

◆Structure : Silicon Monolithic integrated circuit

◆Product name: Voice Synthesis LSI

◆Type : BU6949FV

◆Features

1) Single playback mode, Available bit-rate is 16kbps(High compression) - 128kbps(High Quarity) at 32kHz sampling or 16kHz sampling).

- 2) Voice/audio data is stored in serial Flash ROM which is connected to BU6949FV through SPI-serial Interface. Duration for playback is 32seconds/Mbits(standard) or max 64s/Mbits(Maximum).
- 3) Input system clock: 16.384MHz/8.192MHz/4.096MHz/2.048MHz.
- 4) Audio sampling rate is 32kHz or 16kHz and Built-in 16bits DAC
- 5) Operation by single power supply. Available voltage: 2.7 to 3.6V.
- 6) Max numbers of tunes: 512
- 7) Maximum 10 phrase numbers memory as a ROM-phrase Number, and playback them only one command. (ROM phrase number is available 0-46)
- 8) HOST-I/F is selectable from serial interface with status or direct-pin mode.
- 9) Enable to access(read/write) data stored in serial Flash ROM connected directly to BU6949FV.
- 10) Various play modes are available.

[play modes from serial Interface]

- -decodable 2 channels simultaneously
- -adjustable volume at each track independently
- -enable to playback tunes which are registered in the sequencer list. Order of tunes are randomly selected. Max 16 tunes can be registered.
- -For each track, enable to playback a selected tune or to playback tunes in the sequencer list with/without loop(except ROM_phrase mode).
- -fade-in and fade-out functions are supported.

[Play modes from direct pin control]

- -2ch simultaneously playback available.(phrase0-phrase23 are playback track0, phrase24-31 are playback track1.)
- note) at ROM-phrase mode, phrase number excannge ROM-phrase number.
- -maximum 31 tunes are registered to play.
- -At normal play mode, available loop playback phrase 28-phrase 31 (except ROM-phrase mode).
- ★Radiation resistance design is not arranged.



◆Absolute maximum ratings (Ta = 25°C)

Item	Symbol Ratings		Unit
Power dissipation ^{*)}	Pd	640	mW
Applied voltage	V_{DD}	-0.2 ~ 7.0	V
Input voltage	V_{IN}	-0.2~VDD+0.3	V
Operating temperature range	T_{OPR}	-40 ~+ 85	οຶ
Storage temperature range	TSTG	-50~125	°C

- *) Over Ta = 25°C or more, reducing 6.4mW per °C.
 - ★Radiation resistance design is not arranged.

♦Operation Conditions

(Ta= -40~+85°C unless otherwise specified)

ltom	Cymbol	Specified value			Lloit	Condition	
Item	Symbol	Min	Тур	Max	Unit	Condition	
Operation power-supply voltage	VDD_IN	2.7	-	3.6	V	_	

◆Electric characteristic (DC characteristic)

DC Characteristics

■VDD_IN=3V (Ta=25°C)

100 (10-20 C)								
Item	Symbol	Spe	cified val	ue	Unit	Condition	Circuit form	
nem	Symbol	Min	Тур	Max	Offic	Condition	Circuit ioiiii	
"H" Input Voltage	V_{IH}	0.7VDD	-	_	٧		2	
"L" Input Voltage	V_{IL}	1	-	0.3VDD	٧		2	
"H" Output Voltage	V _{OH}	VDD-0.4	ı	_	V	IO=2.0mA	2	
"L" Output Voltage	V_{OL}	I	ı	0.4	V	IO=2.0mA	2	
"H" Input current	I _{IH}	1	1	10	μΑ	VIH=VDD	1	
"L" Input current	Ι _Ι	1	-	-10	μΑ	VIL=GND	1	
Static consumption current	I _{ST}	-	_	10	μA	$V_i=V_{DD}$ orGND	3	

DAC characteristics

■VDD_IN=3V (Ta=25°C)

ltom	Itam Cumbal		Specified Value			Condition	
Item	Symbol	Min.	Тур.	max.	Unit	Condition	
DACOUToutput load registance	R _{AOUT}	10	ı	ı	ΚΩ	at No signal	
DACOUT Output Voltage	V _{AOUT}	GND	1	VDD	V	at No load	



◆External dimensions • Block diagram

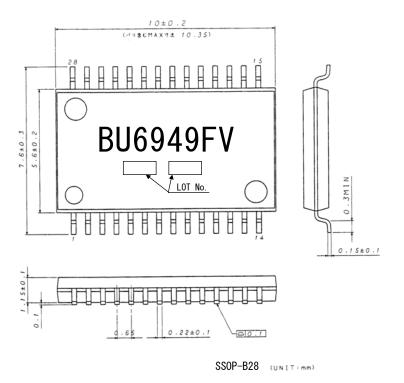


Figure1 External dimention

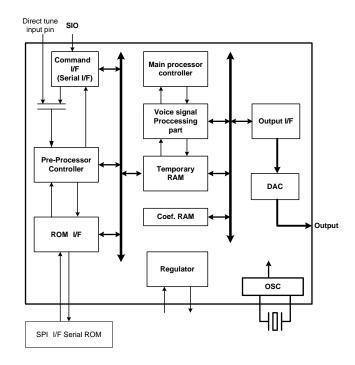


Figure 2. Block diagram



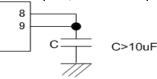
◆Pin name

Table Pin name Detailed table

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PIN NO.	Pin Name	I/O	Function			
1	GND	_	GND			
2	VSEL2/TXD	Ю	tune number pin#2 / Serial Interface output data			
3	VSEL1/RXD	I	tune number pin#1 / Serial Interface input data			
4	VSEL0/RXCB		tune number pin#0 / Serial Interface CLK			
5	TSEVENT/BUSY	0	Playing / ending flag("H":playing "L":stop) accessing Flash ROM ("H": busy "L": not busy)			
6	VSEL3/SYNCREQ	Ю	tune number pin#3 / Synchronous character request ("H" synchronization error)			
7	GND	l	GND			
8	VDD1.8_IN	_	Core power supply input ^{*3}			
9	REG18	0	Core power supply output ^{**3)}			
10	STBY	_	Standby ("H" oscillation stop) normally "L"			
11	TESTEN	I	Test Input("L" fixation)			
12	VDD_IN	_	Power supply input			
13	SPISCK	0	Clock for serial SPI-ROM			
14	SPISO	0	Serial output data to serial SPI-ROM			
15	SPISI	I	Serial Input data from serial SPI-ROM			
16	SPICEB	0	chip enable for serial SPI-ROM			
17	GND	l	GND			
18	VSEL4/BFULLB	0	tune number pin#4 /command buffer Full signal			
19	APOFF		Analog Circuit Power off			
20	CLK16SEL	_	Clock selection "H":16.384Mhz mode "L":4.096MHzmode			
21	REFOUT	0	LSI TEST Pin (attach capacitance(>10uF))			
22	DACOUT	0	DAC Output			
23	GND	_	GND			
24	VDD_IN	_	Power supply input			
25	RESETB	I	Reset pin (low active)			
26	SIO_ENBL	I	Selection of host interface(SIO or direction pin input ^{*1)})			
27	XIN	I	Oscillation cell input ^{*2}			
28	XOUT	0	Oscillation cell Output *2			

^{*1)} At SIO_ENBL ="L", VSEL4, VSEL3, VSEL2, VSEL1, VSEL0 is valid, and SIO is invalid.

^{*3)} pin #8 and pin #9 should be connected in a shortest pass, and attach capacitance(>10uF) as following figure.



[Cautions on use]

Pause Command is available for only 1ch playback. Not Available during 2ch simultaneously playback.

^{*2)} At no setting CLK setting Register, Clock is 16.384MHz at CLK16SEL="H",,4.096MHz at CLK16SEL="L".

Notes

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