Lattice

GAL18V10

High Performance E²CMOS PLD
Generic Array Logic™

FEATURES

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - 15 ns Maximum Propagation Delay
  - Fmax = 62.5 MHz
  - 10ns Maximum from Clock Input to Data Output
  - TTL Compatible 16 mA Outputs
  - UltraMOS® Advanced CMOS Technology

- **LOW POWER CMOS**
  - 75 mA Typical Icc

- **ACTIVE PULL-UPS ON ALL PINS**

- **E² CELL TECHNOLOGY**
  - Reconfigurable Logic
  - Reprogrammable Cells
  - 100% Tested/Guaranteed 100% Yields
  - High Speed Electrical Erasure (50ms)
  - 20 Year Data Retention

- **TEN OUTPUT LOGIC MACROCELLS**
  - Uses Standard 22V10 Macrocells
  - Maximum Flexibility for Complex Logic Designs

- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - 100% Functional Testability

- **APPLICATIONS INCLUDE:**
  - DMA Control
  - State Machine Control
  - High Speed Graphics Processing
  - Standard Logic Speed Upgrade

- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

DESCRIPTION

The GAL18V10, at 15 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest performance 20 pin PLD available on the market. CMOS circuitry allows the GAL18V10 to consume much less power when compared to its bipolar counterparts. The E² technology offers high speed (50ms) erase times, providing the ability to reprogram or reconfigure the device quickly and efficiently.

By building on the popular 22V10 architecture, the GAL18V10 allows the designer to be immediately productive, eliminating the learning curve. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The GAL18V10 OLMC is fully compatible with the OLMC in standard bipolar and CMOS 22V10 devices.

Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products. LATTICE also guarantees 100 erase/rewrite cycles and data retention in excess of 20 years.

FUNCTIONAL BLOCK DIAGRAM
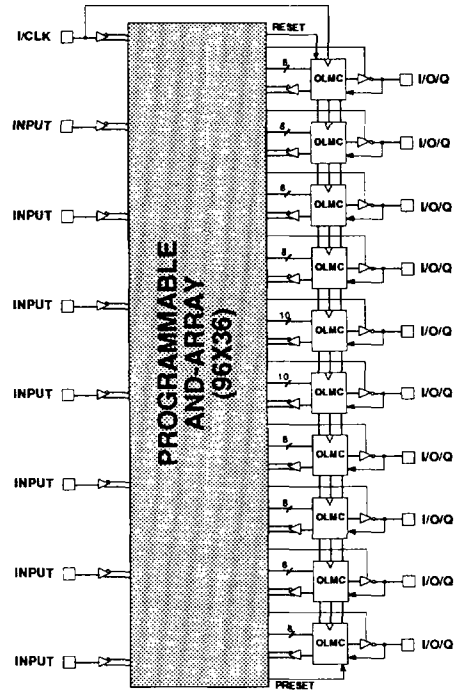
PACKAGE DIAGRAMS
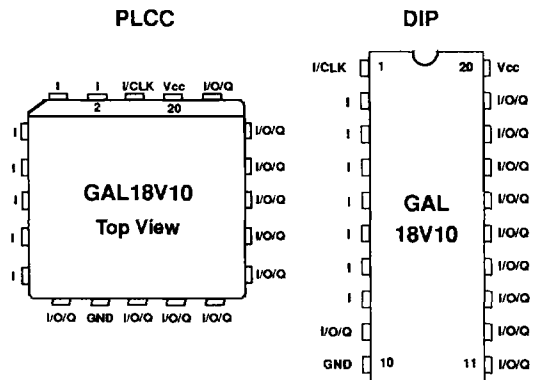
December 1991

ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage V_{cc} ....-0.5 to +7V
Input voltage applied............................-2.5 to V_{cc} +1.0V
Off-state output voltage applied ....-2.5 to V_{cc} +1.0V
Storage Temperature ....-65 to 150°C
Ambient Temperature with
 Power Applied ....-55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

RECOMMENDED OPERATING COND.

Commercial Devices:
Ambient Temperature (T_A) ....0 to +75°C
Supply voltage (V_{cc})
 with Respect to Ground ....+4.75 to +5.25V

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[3]	MAX.	UNITS
V_{IL}	Input Low Voltage		$V_{SS}-0.5$	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	$V_{cc}+1$	V
I_{IL}'	Input or I/O Low Leakage Current	$0V \leq V_{IN} \leq V_{IL}$ (MAX.)	—	—	−100	µA
I_{IH}	Input or I/O High Leakage Current	$3.5V \leq V_{IN} \leq V_{cc}$	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. V_{in} = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. V_{in} = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	16	mA
I_{OH}	High Level Output Current		—	—	−3.2	mA
I_{OS}[2]	Output Short Circuit Current	V_{cc} = 5V V_{OUT} = 0.5V T_A = 25°C	−50	—	−135	mA
I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15Mhz Outputs Open	—	75	115	mA

1) The leakage current is due to the internal pull-up on all pins. See **Input Buffer** section for more information.
2) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
3) Typical values are at Vcc = 5V and TA = 25 °C

CAPACITANCE (T_A = 25 C, f = 1.0 MHz)

SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_i	Input Capacitance	8	pF	V_{cc} = 5.0V, V_i = 2.0V
$C_{I/O}$	I/O Capacitance	10	pF	V_{cc} = 5.0V, $V_{I/O}$ = 2.0V

*Guaranteed but not 100% tested.

AC SWITCHING CHARACTERISTICS

Over Recommended Operating Conditions

PARAMETER	TEST COND.[1]	DESCRIPTION	-15 MIN.	-15 MAX.	-20 MIN.	-20 MAX.	UNITS
t_{pd}	1	Input or I/O to Combinatorial Output	—	15	—	20	ns
t_{co}	1	Clock to Output Delay	—	10	—	12	ns
t_{cf}[2]	—	Clock to Feedback Delay	—	7	—	10	ns
t_{su}	—	Setup Time, Input or Feedback before Clock↑	10	—	12	—	ns
t_h	—	Hold Time, Input or Feedback after Clock↑	0	—	0	—	ns
f_{max}[3]	1	Maximum Clock Frequency with External Feedback, 1/(tsu +tco)	50	—	41.6	—	MHz
	1	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	58.8	—	45.4	—	MHz
	1	Maximum Clock Frequency with No Feedback	62.5	—	62.5	—	MHz
t_{wh}[4]	—	Clock Pulse Duration, High	8	—	8	—	ns
t_{wl}[4]	—	Clock Pulse Duration, Low	8	—	8	—	ns
t_{en}	2	Input or I/O to Output Enabled	—	15	—	20	ns
t_{dis}	3	Input or I/O to Output Disabled	—	15	—	20	ns
t_{ar}	1	Input or I/O to Asynchronous Reset of Register	—	20	—	20	ns
t_{arw}	—	Asynchronous Reset Pulse Duration	10	—	15	—	ns
t_{arr}	—	Asynchronous Reset to Clock↑ Recovery Time	15	—	15	—	ns
t_{spr}	—	Synchronous Preset to Clock↑ Recovery Time	10	—	12	—	ns

1) Refer to **Switching Test Conditions** section.
2) Calculated from fmax with internal feedback. Refer to **fmax Description** section.
3) Refer to **fmax Description** section.
4) Clock pulses of widths less than the specification may be detected as valid clock signals.

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GAL18V10 ORDERING INFORMATION

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	10	10	115	GAL18V10-15LP	20-Pin Plastic DIP
			115	GAL18V10-15LJ	20-Lead PLCC
20	12	12	115	GAL18V10-20LP	20-Pin Plastic DIP
			115	GAL18V10-20LJ	20-Lead PLCC

Industrial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
20	12	12	125	GAL18V10-20LPI	20-Pin Plastic DIP
			125	GAL18V10-20LJI	20-Lead PLCC

PART NUMBER DESCRIPTION

XXXXXXXX – XX X X X

GAL18V10 **Device Name**

Speed (ns)

L = Low Power **Power**

Grade Blank = Commercial
I = Industrial

Package P = Plastic DIP
J = PLCC