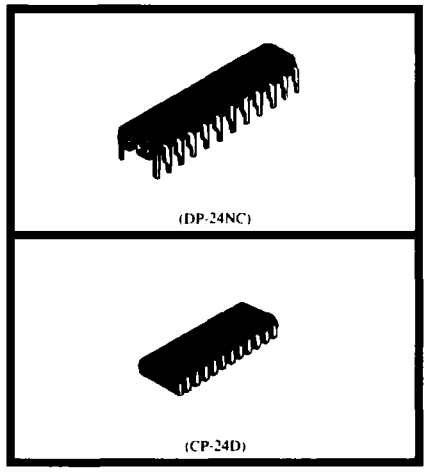
HM6208/HM6208H Series
4-Bit CMOS Static RAM

65536-Word × 4-Bit High Speed CMOS Static RAM

The Hitachi HM6208 and HM6208H are high speed 256k static RAMS organized as 64k-word × 4 bit. They realize high speed access time (25/35/45 ns) and low power consumption, employing CMOS process technology and high speed circuit designing technology. It is most advantageous wherever high speed and high density memory is required, such as the cache memory for main frame or 32-bit MPU.

The HM6208 and HM6208H are packaged in the industry standard 300-mil, 24 pin, plastic DIP. The HM6208H is also available in a 300-mil, 24 pin, plastic SOJ package for high density mounting. The low power versions are ideal for battery backed systems.



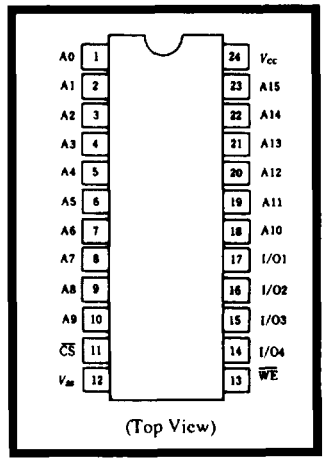
Features

- Single 5 V supply and high density 24-pin package
- High speed: Access time 25/35/45 ns (max.)
- Low power
  - Active: 300 mW (typ.)
  - Standby: 100 μW (typ.)
  - 30 μW (typ.) (L-version)
- Completely static operation requires
  - No clock or timing strobe
- Access and cycle times are equivalent
- All inputs and outputs TTL compatible
- Capability of battery back up operation (L-version)

Ordering Information

Type No.	Access Time	Package
HM6208P-35	35 ns	300-mil 24-pin plastic DIP (DP-24NC)
HM6208P-45	45 ns	
HM6208LP-35	35 ns	
HM6208LP-45	45 ns	
HM6208HP-25	25 ns	
HM6208HP-35	35 ns	
HM6208HLP-25	25 ns	
HM6208HLP-35	35 ns	
HM6208HJP-25	25 ns	300-mil 24-pin plastic SOJ (CP-24D)
HM6208HJP-35	35 ns	
HM6208HLJP-25	25 ns	
HM6208HLJP-35	35 ns	

Pin Arrangement

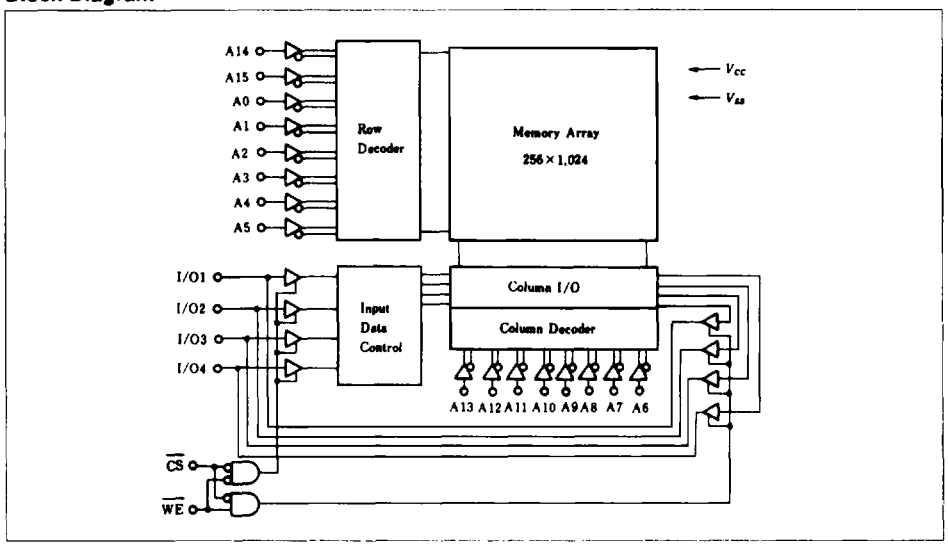


(Top View)

Pin Description

Pin Name	Function
A0 – A15	Address
I/O1 – I/O4	Input/Output
$\overline{CS}$	Chip select
$\overline{WE}$	Write enable
Vcc	Power supply
Vss	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{WE}$	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	—
L	H	Read	Icc	Dout	Read cycle
L	L	Write	Icc	Din	Write cycle

Note: × means don't care.

Absolute Maximum Ratings

Item	Symbol	Value	Unit
Voltage on any pin relative to Vss	Vin	−0.5*1 to +7.0	V
Power dissipation	P_T	1.0	W
Operating temperature range	T_{opr}	0 to +70	°C
Storage temperature range	Tstg	−55 to +125	°C
Storage temperature range under bias	Tbias	−10 to +85	°C

Note: *1. Vin min = −2.5 V for pulse width ≤ 10 ns.

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high (logic 1) voltage	V_{IH}	2.2	—	6.0	V
Input low (logic 0) voltage	V_{IL}	-0.5*1	—	0.8	V

Note: *1. V_{IL} min = -2.0 V for pulse width ≤ 10 ns.

■ DC Characteristics (T_a = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Item	Symbol	Min.	Typ.*1	Max.	Unit	Test Conditions
Input Leakage Current	I_{LI}	—	—	2.0	μA	V_{CC} = Max. V_{in} = V_{SS} to V_{CC}
Output Leakage Current	I_{LO}	—	—	10.0	μA	$\overline{CS}$ = V_{IH} $V_{I/O}$ = V_{SS} to V_{CC}
Operating Power Supply Current	I_{CC}	—	60	100	mA	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0 mA, Min. Cycle, Duty = 100%
Standby Power Supply Current	I_{SB}	—	15	30	mA	$\overline{CS}$ = V_{IH}, Min. Cycle
Standby Power Supply Current "H" Version	I_{SB}	—	20	40	mA	
Standby Power Supply Current	I_{SB1}	—	20	2000	μA	$\overline{CS}$ ≥ V_{CC} - 0.2 V 0 V ≤ V_{in} ≤ 0.2 V or V_{in} ≥ V_{CC} - 0.2V
Standby Power Supply Current L-Version	I_{SB1}	—	6	100	μA	
Output Low Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 8 mA
Output High Voltage	V_{OH}	2.4	—	—	V	I_{OH} = -4.0 mA

Note: *1. Typical limits are at V_{CC} = 5.0 V, T_a = +25°C and specified loading.

Capacitance (Ta = 25°C, f = 1MHz)*1

Item	Symbol	Min	Max	Unit	Test Conditions
Input capacitance	Cin	—	6	pF	Vin = 0 V
Input/output capacitance	Cvo	—	10	pF	Vvo = 0 V

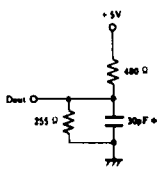
Note: *1. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to +70°C, Vcc = 5 V ± 10%, unless otherwise noted.)

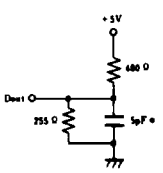
Test Conditions

- Input pulse levels: Vss to 3.0 V
- Input rise and fall times: 5 ns
- Input and output timing reference levels : 1.5 V
- Output load: See Figures

Output Load (A)



Output Load (B)
(for tHZ, tLZ, tWZ & tOW)



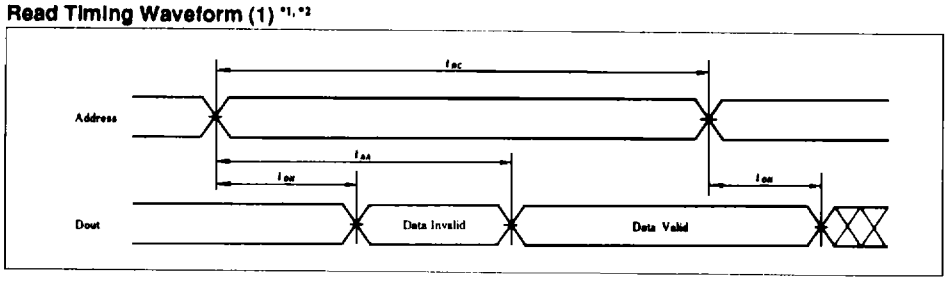
Note: * Including scope & jig.

Read Cycle

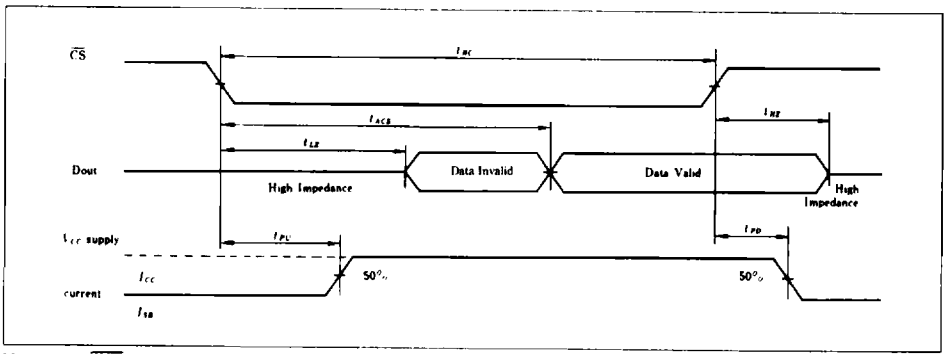
Item	Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	25	—	35	—	45	—	ns
Address Access Time	t_{AA}	—	25	—	35	—	45	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	—	45	ns
Output Hold From Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low-Z	t_{LZ}*1	5	—	5	—	5	—	ns
Chip Deselection to Output in High-Z	t_{HZ}*1	0	12	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	15	—	25	—	30	ns

Note: *1 Transition is measured ±200 mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

Read Timing Waveform (1) *1, *2



Read Timing Waveform (2) *1, *3



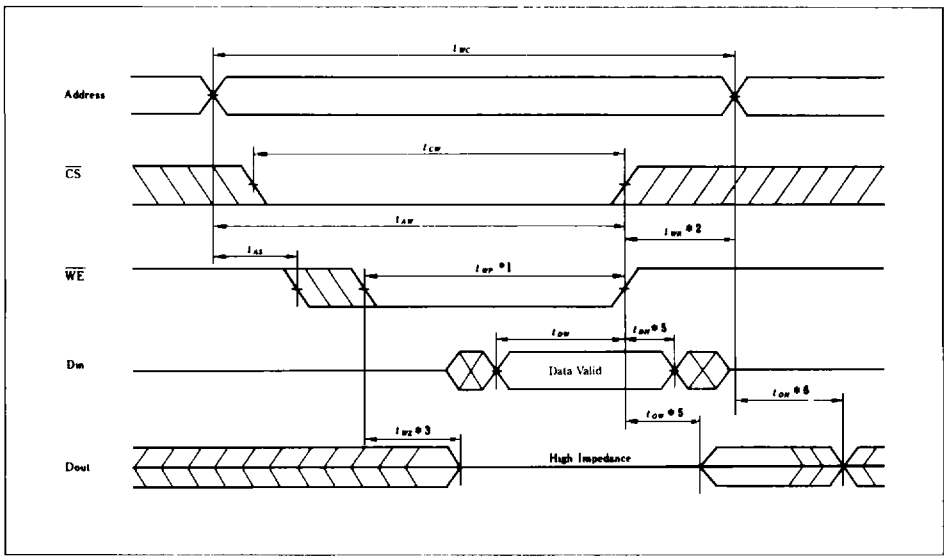
Notes: *1. $\overline{WE}$ is high for read cycle.
*2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
*3. Address valid prior to or coincident with $\overline{CS}$ transition low.

Write Cycle

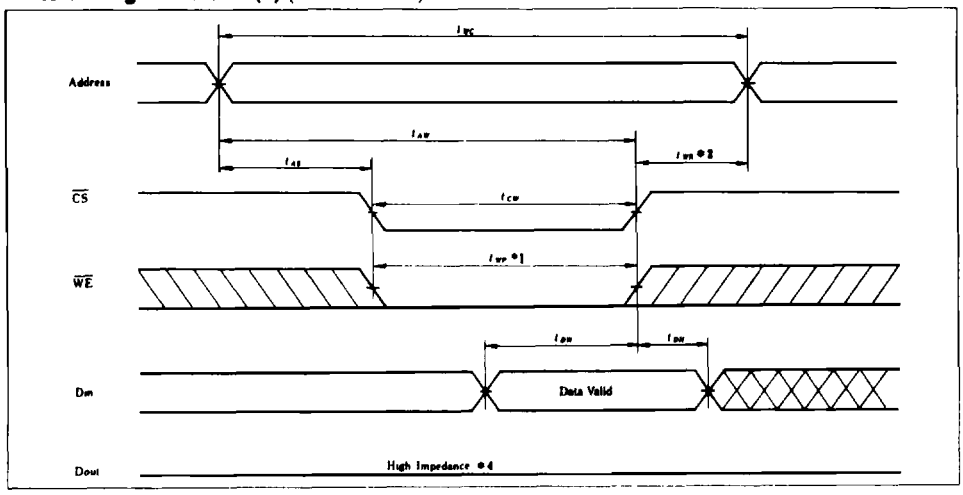
Item		Symbol	HM6208H-25		HM6208-35 HM6208H-35		HM6208-45		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time		t_{WC}	25	—	35	—	45	—	ns
Chip Selection to End of Write		t_{CW}	20	—	30	—	40	—	ns
Address Valid to End of Write		t_{AW}	20	—	30	—	40	—	ns
Address Setup Time		t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width		t_{WP}	20	—	30	—	35	—	ns
	"H" Version				25				
Write Recovery Time		t_{WR}	3	—	3	—	3	—	ns
Data Valid to End of Write		t_{DW}	15	—	20	—	20	—	ns
Data Hold Time		t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High-Z		t_{WZ}*1	0	8	0	10	0	15	ns
Output Active From End of Write		t_{OW}*1	0	—	0	—	0	—	ns

Note: *1 Transition is measured ±200 mV from high impedance voltage with Load (B). This parameter is sampled and not 100% tested.

Write Timing Waveform (1) ($\overline{WE}$ Controlled)



Write Timing Waveform (2) ($\overline{CS}$ Controlled)



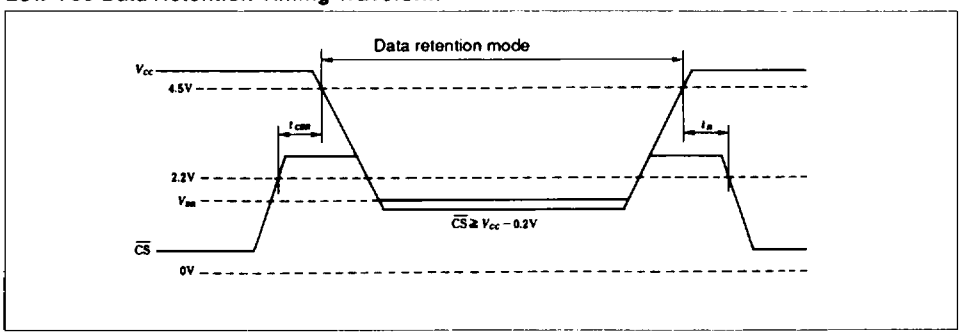
Low V_{CC} Data Retention Characteristics (T_a = 0 to +70°C)

These characteristics are guaranteed only for L-version.

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Vcc for data retention	V_{DR}	2.0	—	—	V	$\overline{CS}$ ≥ Vcc – 0.2 V, Vin ≥ Vcc – 0.2 V or 0 V ≤ Vin ≤ 0.2 V
Data retention current	I_{CCDR}	—	1	50*2	µA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	t_{RC}*1	—	—	ns	

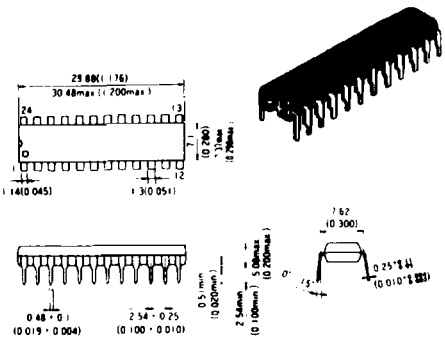
Notes: *1. t_{RC} = read cycle time.
*2. Vcc = 3.0 V.

Low Vcc Data Retention Timing Waveform



■ PACKAGE DIMENSIONS Unit: mm (inch)

HM6208/HM6208HP Series
(DP-24NC)



HM6208HJP Series
(CP-24D)