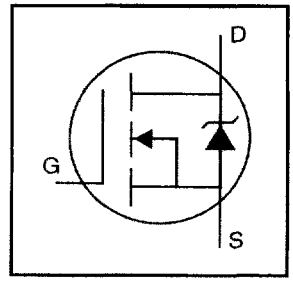
International
IOR Rectifier

PD - 9.1409A

IRFP048N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 55V

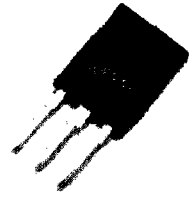
$R_{DS(on)}$ = 0.016Ω

I_D = 64A

Description

Fifth Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design for which HEXFET Power MOSFETs are well known, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



TO-247

Absolute Maximum Ratings

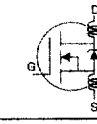
	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	64	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	45	
I_{DM}	Pulsed Drain Current ①⑤	210	
P_D @T_C = 25°C	Power Dissipation	140	W
	Linear Derating Factor	0.90	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	270	mJ
I_{AR}	Avalanche Current ①⑤	32	A
E_{AR}	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

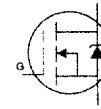
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.052	—	V/°C	Reference to 25°C, I_D = 1mA ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.016	Ω	V_{GS} = 10V, I_D = 37A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	22	—	—	S	V_{DS} = 25V, I_D = 32A ⑤
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V_{DS} = 55V, V_{GS} = 0V
		—	—	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	89	nC	I_D = 32A
Q_{gs}	Gate-to-Source Charge	—	—	20		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	39		V_{GS} = 10V, see figure 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	V_{DD} = 28V
t_r	Rise Time	—	78	—		I_D = 32A
$t_{d(off)}$	Turn-Off Delay Time	—	32	—		R_G = 5.1Ω
t_f	Fall Time	—	48	—		R_D = 0.85Ω, see figure 10 ④⑤
L_D	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	13	—		
C_{iss}	Input Capacitance	—	1900	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	620	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	270	—		f = 1.0MHz, see figure 5⑤



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	64	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①⑤	—	—	210		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 37A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	94	140	ns	T_J = 25°C, I_F = 32A
Q_{rr}	Reverse Recovery Charge	—	360	540	nC	di/dt = 100A/μs ④⑤



Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (see figure 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 530μH, R_G = 25Ω, I_{AS} = 32A. (see figure 12)

③ I_{SD} ≤ 32A, di/dt ≤ 250A/μs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRFZ48N data and test conditions

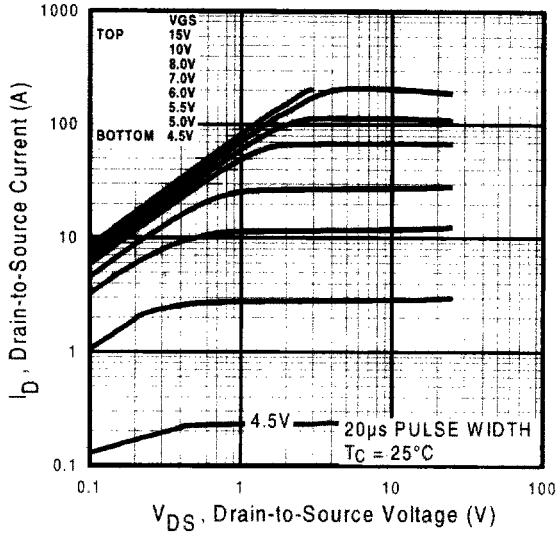


Fig 1. Typical Output Characteristics

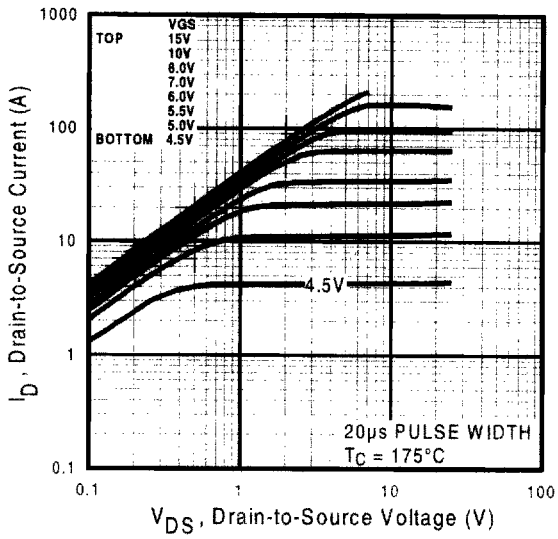


Fig 2. Typical Output Characteristics

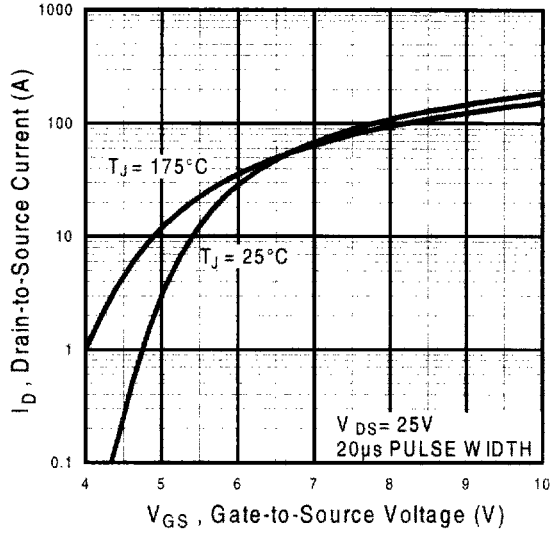


Fig 3. Typical Transfer Characteristics

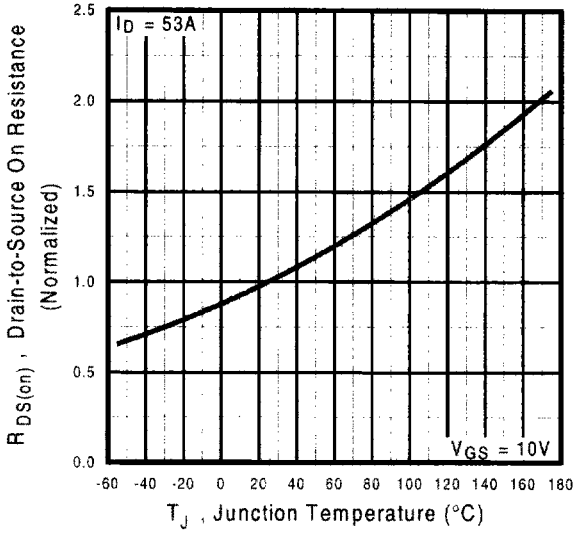


Fig 4. Normalized On-Resistance Vs. Temperature

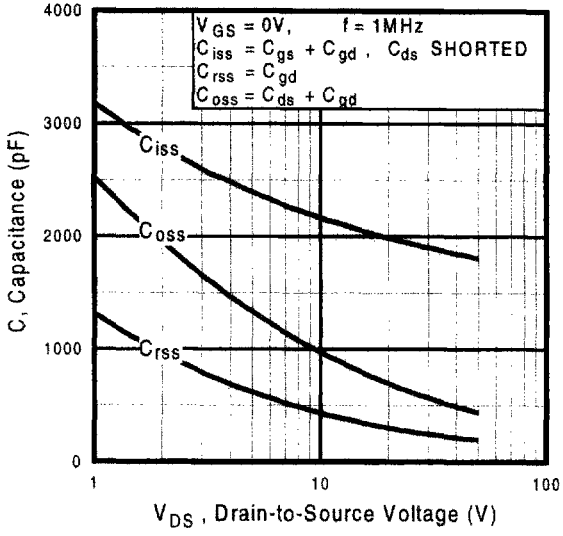


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

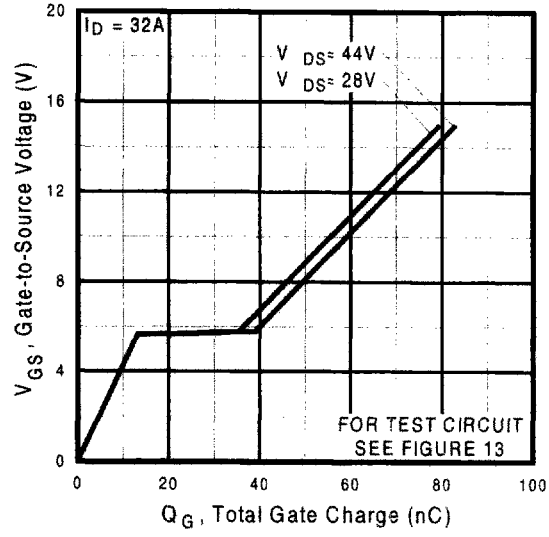


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

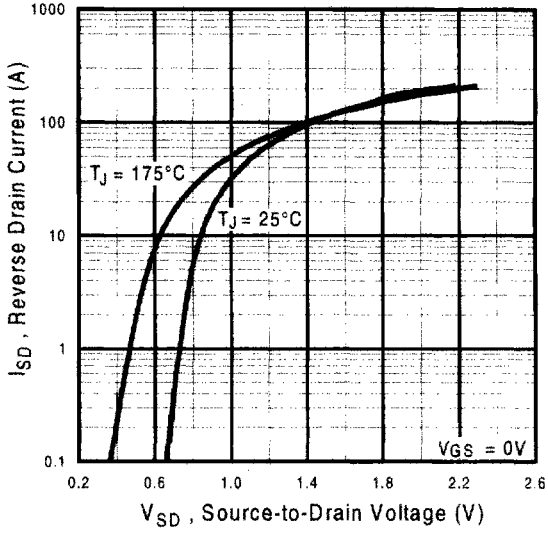


Fig 7. Typical Source-Drain Diode Forward Voltage

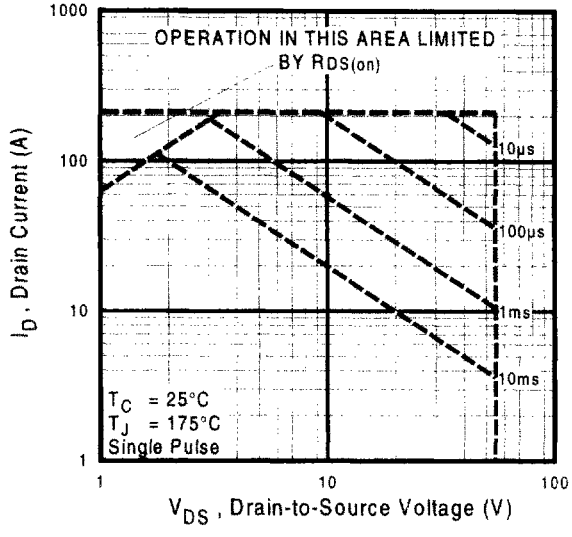


Fig 8. Maximum Safe Operating Area

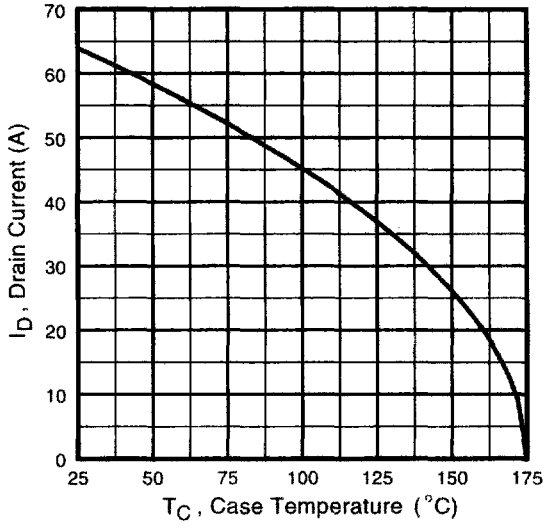


Fig 9. Maximum Drain Current Vs. Case Temperature

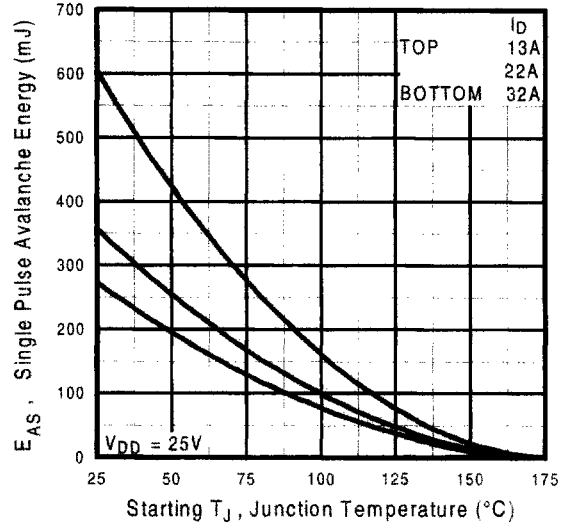


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

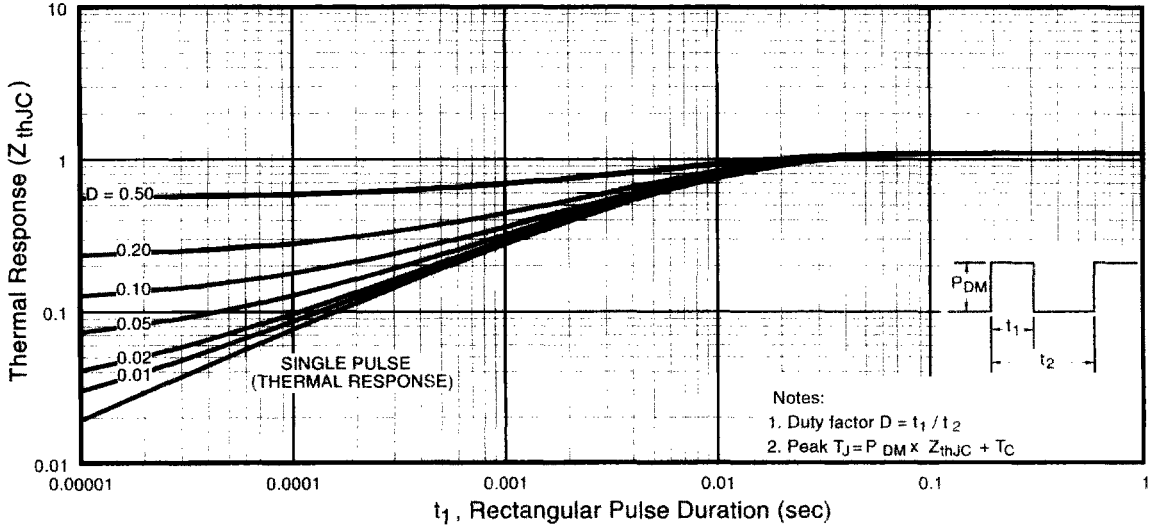


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical drawings, Appendix A
Part marking information, Appendix B
Test Circuit diagrams, Appendix C