

SPEC No. MR96307
ISSUE: Mar. 29 1996

To: _____

PRELIMINARY

SPECIFICATIONS

Product Type 8M bit MASK ROM

LH5G8P××

(LH58FV8P00T-X)

*This specifications contains 9 pages including the cover.
If you have any objections, please contact us before issuing purchasing order.

PRESENTED

BY: M. Okada
M. OKADA
Dept. General Manager

REVIEWED BY: PREPARED BY:
Y. Hotta M. Hayasaki

Engineering Dept. 1
Memory Engineering Center
Tenri Integrated Circuits Group
SHARP CORPORATION



LH53FV8POOT-X

●Handle this document carefully for it contains material protected by international copyright law. Any reproduction, full or in part, of this material is prohibited without the express written permission of the company.

●When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

(1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

- Office electronics
- Instrumentation and measuring equipment
- Machine tools
- Audiovisual equipment
- Home appliances
- Communication equipment other than for trunk lines

(2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-safe operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

- Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
- Mainframe computers
- Traffic control systems
- Gas leak detectors and automatic cutoff devices
- Rescue and security equipment
- Other safety devices and safety equipment, etc.

(3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

- Aerospace equipment
- Communications equipment for trunk lines
- Control equipment for the nuclear power industry
- Medical equipment related to life support, etc.

(4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

●Please direct all queries regarding the products covered herein to a sales representative of the company.

C O N T E N T S

1. General Description	P.2
2. Features	P.2
3. Block Diagram	P.3
4. Pin Connections	P.4
5. Pin Description	P.4
6. Absolute Maximum Ratings	P.5
7. Operating Ranges	P.5
8. D.C. Electrical Characteristics	P.5
9. A.C. Electrical Characteristics	P.6
10. Timing Chart	P.7
11. Note	P.7
12. Package and packing specification	P.8

1. General Description

The Sharp LH568Pxx(LH53FY8P00T) is an 8Mbit CMOS mask ROM (mask-programmable read-only memory), produced by the silicon gate CMOS process.

2. Features

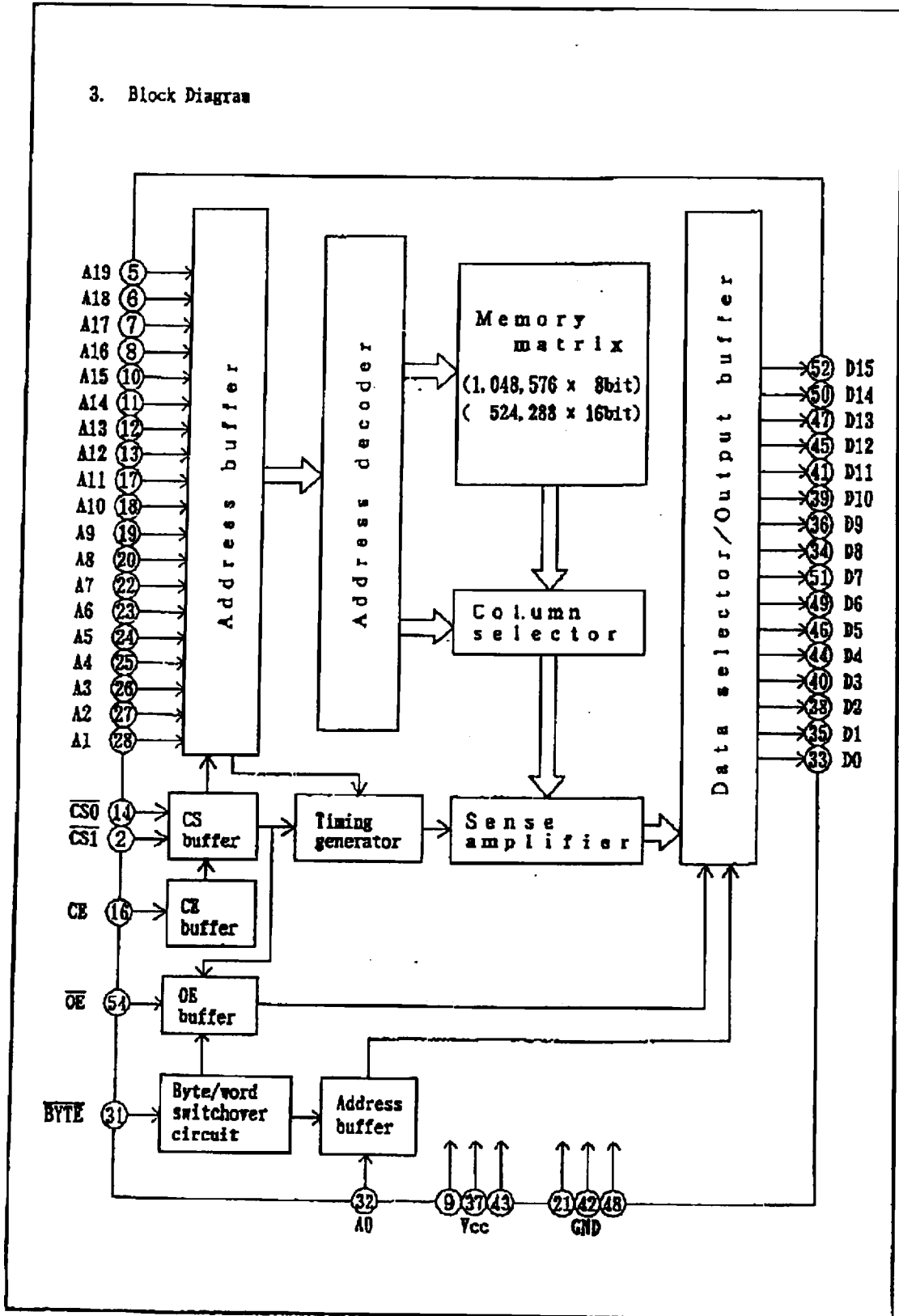
- Memory organization selection
 - 1,048,576 x 8-bit (Byte mode : $\overline{\text{BYTE}}=\text{V}_{12}$)
 - 524,288 x 16-bit (Word mode : $\overline{\text{BYTE}}=\text{V}_{12}$)
- Supply voltage:
3.3V \pm 0.3V
- Static operation
- 3-state output
- Access time:
120ns (Max.)
- 56Pin-TSOP(TYPE-I)
- Supply current
 - Operating: 35mA (Max.)
 - Standby : 30 μ A (Max.)
- Others
 - Non programmable
 - Not designed or rated as radiation hardened
 - CMOS process(P type silicon substrate)

SHARP

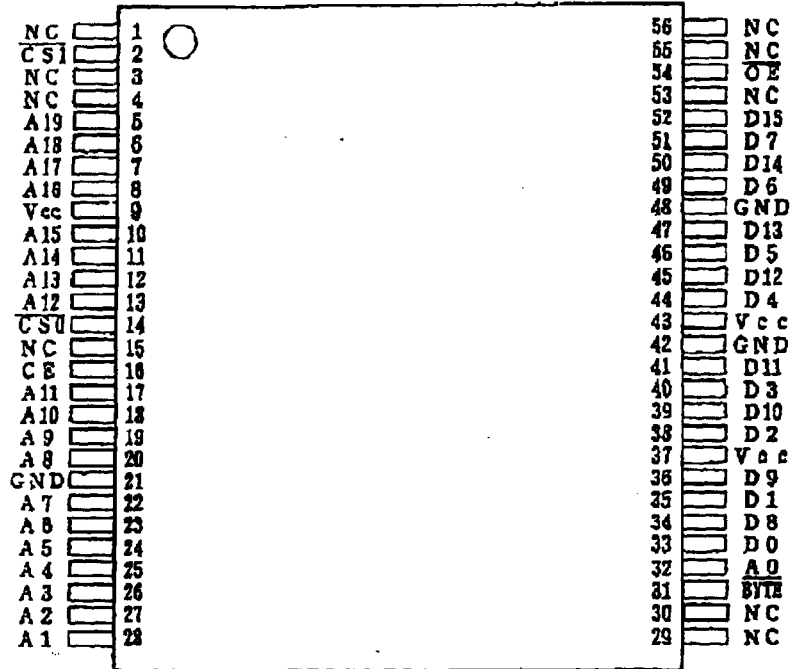
LH53FV8P00T-X

3 ⁶/₁₉

3. Block Diagram



4. Pin Connections



(56Pin-ISO P TYPE-1)

5. Pin Description

A0 ~ A19	Address input
D0 ~ D15	Data output
BYTE	x8bit/x16bit(byte/word) mode select input (Note)
CE	Chip enable input (Note)
CS0, CS1	Chip select input (Note)
OE	Output enable input (Note)
Vcc	Power pin
GND	Ground
NC	Non connection (Non wire bonding)

(Note)

CE	CS0	CS1	OE	BYTE	A0	Data output		Address input		Supply current
						D0-D7-Pin	D8-D15-Pin	LSB	MSB	
L	X	X	X	X	X	High impedance	High impedance	-	-	Standby
H	H	H	X	X	X	High impedance	High impedance	-	-	Power down
H	H	L	X	X	X	High impedance	High impedance	-	-	Power down
H	L	H	X	X	X	High impedance	High impedance	-	-	Power down
H	L	L	H	X	X	High impedance	High impedance	-	-	Operating
H	L	L	L	H	-	D0-D7	D8-D15	A1	A19	Operating
H	L	L	L	L	L	D0-D7	High impedance	A0	A19	Operating
H	L	L	L	L	H	D8-D15	High impedance	A0	A19	Operating

X: Don't Care

SHARP

LH53FV8P00T-X

5

8/19

6. Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage	V _{CC}	-0.3 ~ +4.6	V
Input Voltage	V _{IN}	-0.3 ~ V _{CC} +0.3	V
Output Voltage	V _{OUT}	-0.3 ~ V _{CC} +0.3	V
Operating Temperature	T _{OPS}	0 ~ +70	°C
Storage Temperature	T _{STG}	-85 ~ +150	°C

7. Operating Ranges

Ta=0-70°C

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V

8. D.C. Electrical Characteristics

V_{CC}=3.3V±0.3V, Ta=0-70°C

Item	Symbol	Test conditions	Min.	Max.	Unit	Note
Input high voltage	V _{IH}		2.0	V _{CC} +0.3	V	
Input low voltage	V _{IL}		-0.3	0.8	V	
Output high voltage	V _{OH}	I _{OH} =-400μA	2.4		V	
Output low voltage	V _{OL}	I _{OL} =2.0mA		0.4	V	
Input leakage current	I _{IH}	V _{IN} =0V~V _{CC}		5	μA	
Output leakage current	I _{LO}	V _{OUT} =0V~V _{CC}		5	μA	1
Supply current(Operating)	I _{CC1}	t _{nc} =120ms		35	mA	2
Supply current (Power down)	I _{PD1}	CS0, CS1, CE=V _{IH}		1	mA	
	I _{PD2}	CS0, CS1, CE=V _{CC} -0.2V		50	μA	
Supply current (standby)	I _{SS1}	CE=V _{IL}		1	mA	
	I _{SS2}	CE=0.2V		30	μA	
Input capacitance	C _{IN}	f=1MHz		10	pF	
Output capacitance	C _{OUT}	Ta=25°C		10	pF	

Note 1: CE = V_{IL}OE = V_{IH}Note 2: V_{IH} = V_{IH}, V_{IL}CE = V_{IL}CS0, CS1 = V_{IL}

(Output is open)

9. A.C. Electrical Characteristics

V_{CC}=3.3V±0.3V, T_a=0~70°C

Item	symbol	Min.	Max.	Unit
Read cycle time	t _{RC}	120		ns
Address access time	t _{AA}		120	
Chip enable access time	t _{ACE}		130	
Chip select access time	t _{ACS}		120	
Output enable delay time	t _{OE}		50	
Output hold time	t _{OH}	5		
Output floating time	t _{CSZ}		50 (Note)	
	t _{CSU}			
	t _{OSZ}			

Test Condition

Input voltage amplitude : 0.6V ~ 2.2V
 Input signal rise time : 10ns
 Input signal fall time : 10ns
 Input reference level : 1.4V
 Output reference level : 1.4V
 Output load condition : 1TTL + 100pF

(Note) Determined by the time for the output to be opened.
 (irrespective of output voltage)

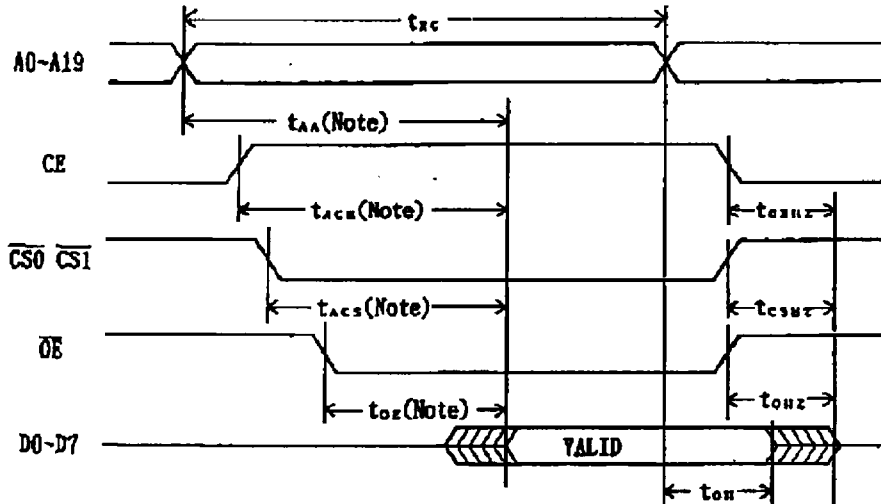
SHARP

LH53FV8POOT-X

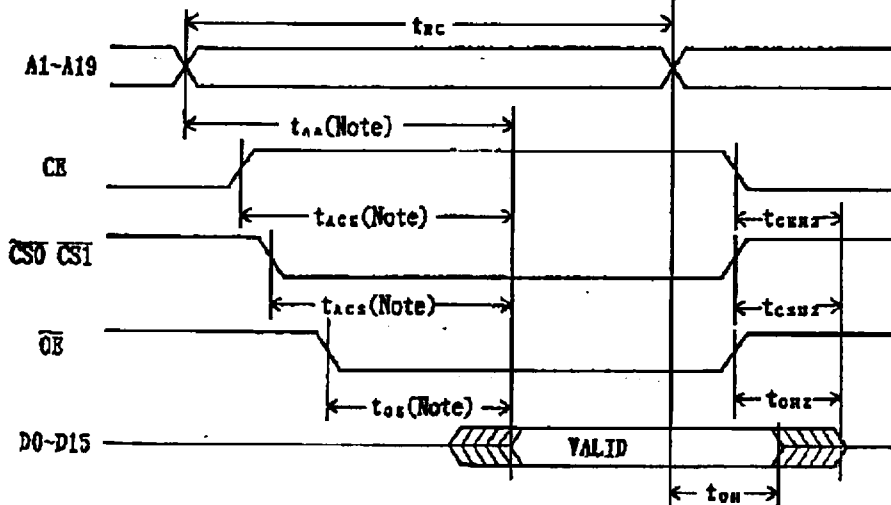
7 10/19

10. Timing Chart

i) Byte mode ($\overline{\text{BYTE}} = V_{IL}$)



ii) Word mode ($\overline{\text{BYTE}} = V_{IH}$)



Note : The output data becomes valid when the last interval, t_{AA} , t_{ACC} , t_{ACS} or t_{OS} have concluded.

11. Note

It is recommended that a decoupling capacitor be connected between Vcc and Gnd-Pin.