M5M5258P,J-35,-45,-45L

262144-BIT(65536-WORD BY 4-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5258P is a family of 65536 word by 4-bit static RAMs, fabricated with the high-performance CMOS silicon-gate MOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

● Fast access time   M5M5258P, J-35 . . . 35 ns (max)
                       M5M5258P, J-45 . . . 45 ns (max)
                       M5M5258P, J-45L . . 45 ns (max)
● Low power dissipation Active . . . . 300 mW (typ)
                       Stand by . . . . . . 0.5 mW (typ)
                       Stand by(-45L) . . . 50 μW (typ)
● Power down by $\overline{S}$
● Single 5V power supply
● Fully static operation
   Requires neither external clock nor refreshing
● All inputs and output are directly TTL compatible
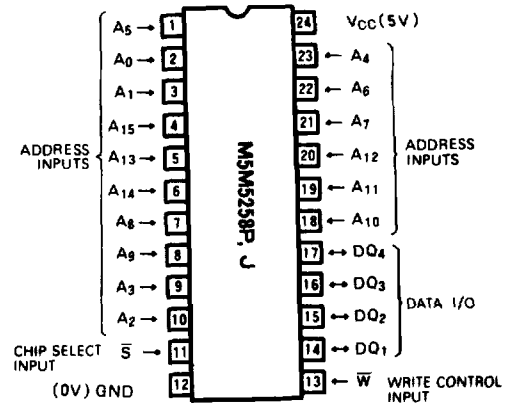● Easy memory expansion by chip-select ($\overline{S}$) input

APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

In a read operation, after setting $\overline{W}$ to high, and $\overline{S}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Signal $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

PIN CONFIGURATION (TOP VIEW)

Outline 24P4Y (DIP)
24P0J (SOJ)

BLOCK DIAGRAM

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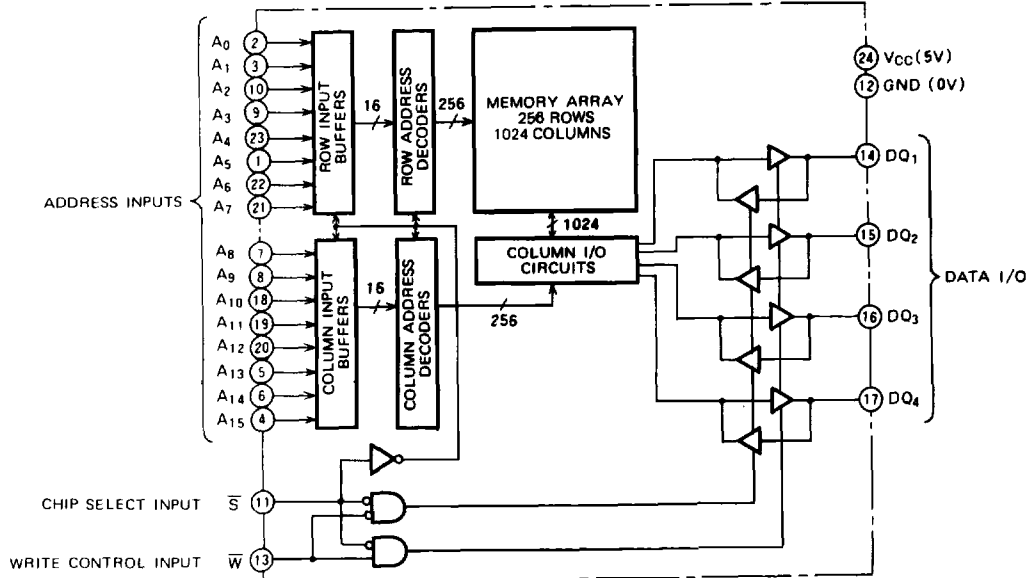
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MODE SELECTION

$\overline{S}$	$\overline{W}$	Mode	Data I/O	I_{CC}
H	X	Non selection	High-impedance	Standby
L	L	Write	D_{IN}	Active
L	H	Read	D_{OUT}	Active

H : V_{IH} L : V_{IL} X : V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Units
V_{CC}	Supply voltage	With respect to GND	-3.5^{*} 7	V
V_I	Input voltage		-3.5^{*} 7	V
V_O	Output voltage		-3.5^{*} 7	V
P_d	Maximum power dissipation		1	W
T_{opr}	Operating temperature		-10 85	°C
T_{stg}	Storage temperature		-65 150	°C

* Pulse width = 20 ns, In case of DC: -0.5V

DC ELECTRICAL CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage			2.4		$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage			-0.5 *		0.6	V
V_{OH}	High-level output voltage	$I_{OH} = -4$ mA		2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA				0.4	V
I_I	Input current	$V_I = 0 \sim 5.5V$				2	μA
$|I_{OZ}|$	Off-state output current	$V_I(\overline{S}) = V_{IH}$, $V_O = 0 \sim V_{CC}$				10	μA
I_{CC1}	Supply current from V_{CC}	$V_I(\overline{S}) = V_{IL}$ Output open				120	mA
I_{CC2}	Stand by current	$V_I(\overline{S}) = V_{IH}$				3	mA
I_{CC3}	Stand by current	$V_I(\overline{S}) \geq V_{CC} - 0.2V$	-35, -45		0.1	2	mA
			$-45L$		10	100	μA

Note 1. Current flow into an IC is positive, out is negative.
* In case of AC: -3.0V (Pulse width $\leq$ 20 ns)

CAPACITANCE ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	$V_I = GND$, $V_I = 25mVrms$, $f = 1MHz$			5	pF
C_O	Output capacitance	$V_O = GND$, $V_O = 25mVrms$, $f = 1MHz$			6	pF

AC ELECTRICAL CHARACTERISTICS ($Ta = 0 \sim 70°C$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels . . . . $V_{IH} = 3V$, $V_{IL} = 0V$
Input rise and fall time . . . . 3 ns
Input timing reference level . . . . $V_{IH} = 2.4V$, $V_{IL} = 0.6V$
Output timing reference leve . . . . $V_{OH} = 2V$, $V_{OL} = 0.8V$
Output loads . . . . Fig. 1, Fig. 2
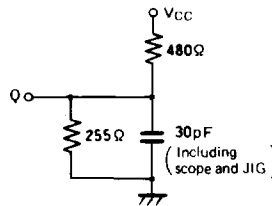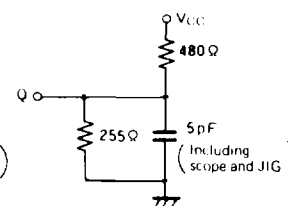
Fig. 1 Output load   Fig. 2 Output load for t_{en}, t_{dis}
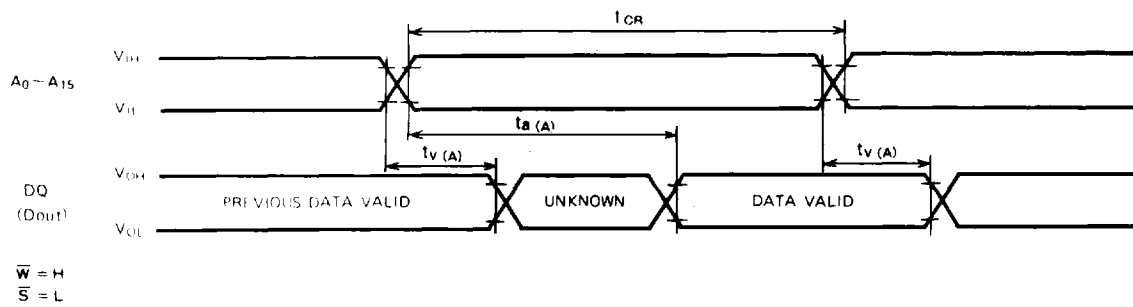
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(2) READ CYCLE

Symbol	Parameter	M5M5258P, J-35			M5M5258P, J-45, -45L			Unit
		Min	Typ	Max	Min	Typ	Max	
$t_{c(R)}$	Read cycle time	35			45			ns
$t_{a(A)}$	Address access time			35			45	ns
$t_{a(S)}$	Chip select access time			35			45	ns
$t_{v(A)}$	Data valid time after address	5			5			ns
$t_{en(S)}$	Chip selection to output active	5			5			ns
$t_{dis(S)}$	Output disable time from CS	0		20	0		20	ns
t_{PU}	Power-up time after chip selection	0			0			ns
t_{PD}	Power down time after chip deselection			35			45	ns

(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1

$\overline{W} = H$
$\overline{S} = L$

Read cycle 2 (Note 2)
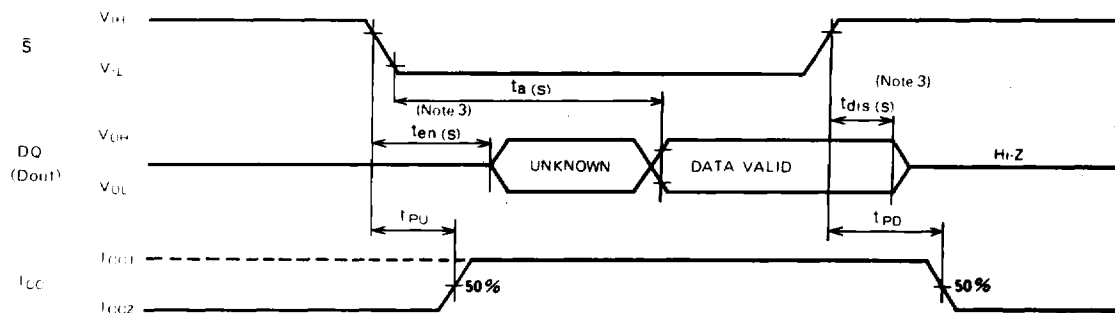
$\overline{W} = H$

Note 2 Addresses valid prior to or coincident with $\overline{S}$ transition low.
3 Transition is measured ±500mV from steady state voltage with specified loading in Figure 2.

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(4) WRITE CYCLE (Ta=0~70°C, V$_{CC}$=5V±10%, unless otherwise noted)

| Symbol	Parameter	M5M5258P, J-35			M5M5258P, J-45, -45L			Unit
		Min	Typ	Max	Min	Typ	Max	
t$_{c(W)}$	Write cycle time	35			45			ns
t$_{su(S)}$	Chip select setup time	30			35			ns
t$_{su(A)1}$	Address setup time (W)	0			0			ns
t$_{su(A)2}$	Address setup time (S)	0			0			ns
t$_{w(W)}$	Write pulse width	30			35			ns
t$_{rec(W)}$	Write recovery time	5			5			ns
t$_{su(D)}$	Data setup time	15			20			ns
t$_{h(D)}$	Data hold time	0			0			ns
t$_{dis(W)}$	Output disable time from W			15			15	ns
t$_{en(W)}$	Output enable time from W	0			0			ns
t$_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	30			35			ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)
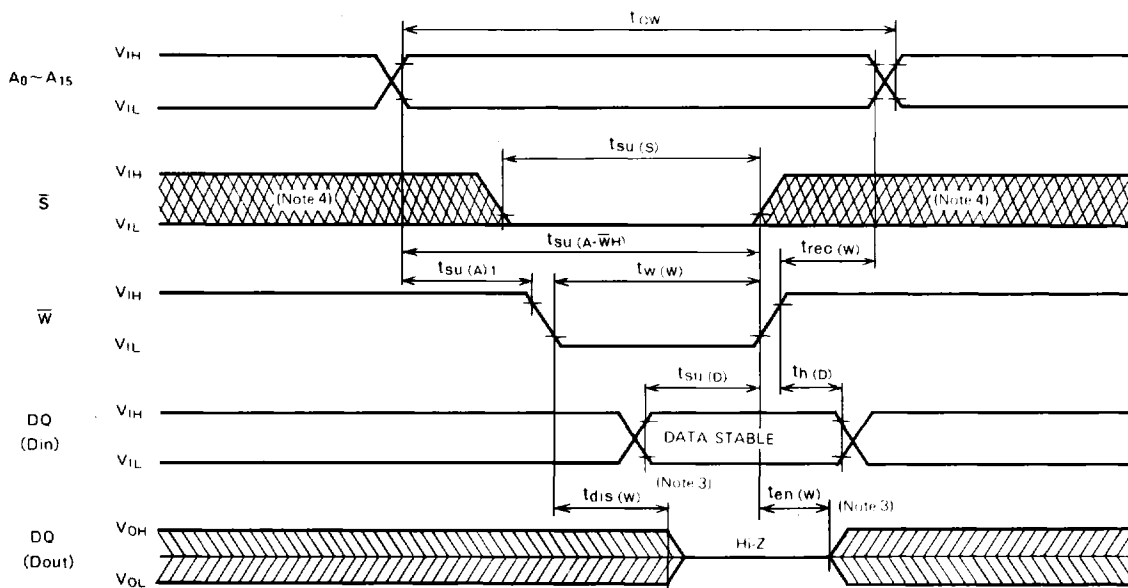
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Write cycle 2 (S̄ control mode)
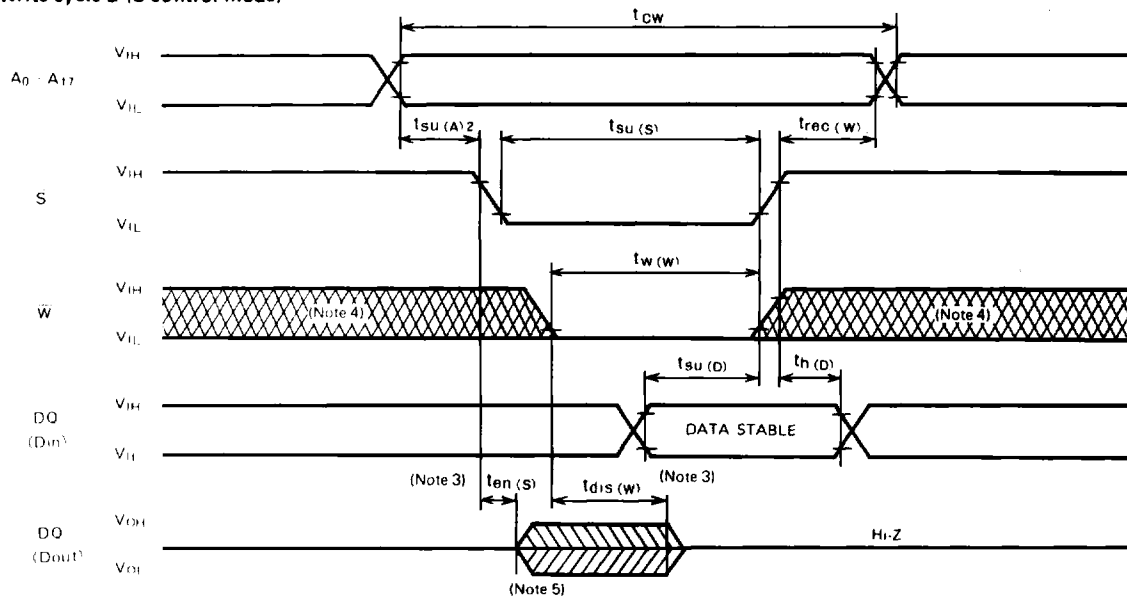
Note 4 Hatching indicates the state is don't care.
5 When the falling edge of W̄ is simultaneous or prior to the falling edge of S̄, the output is maintained in the high impedance.

DATA RETENTION CHARACTERISTICS (Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Characteristics	Test condition	Limits			Units
			Min	Typ	Max	
$V_{CC(PD)}$	Power down supply voltage	$V_I(\bar{S}) \geqq V_{CC} - 0.2V$	2			V
$V_{I(\bar{S})}$	Chip select input voltage		$V_{CC}-0.2$			V
$t_{su(PD)}$	Power down setup time	$V_I \geqq V_{CC} - 0.2V$ or $0V \leqq V_I \leqq 0.2V$	0			ns
$t_{rec(PD)}$	Power down recovery time		45			ns
$I_{CC(PD)}$	Power down supply current	$V_{CC} = 3.0V$			50	μA
		$V_{CC} = 5.5V$			100	μA

Note 6. This is only M5M5258P, J-45L

TIMING WAVEFORM FOR POWER DOWN

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