8/16-bit Data Bus Flash Memory Card

MF82M1-G7DATXX
MF84M1-G7DATXX
MF88M1-G7DATXX
MF810M-G7DATXX
MF816M-G7DATXX
MF820M-G7DATXX

Connector Type

Two- piece 68-pin

DESCRIPTION

The MF8XXX-G7DATXXX is a flash memory card which uses eight-megabit flash electrically erasable and programmable read only memory IC's as common memory and a 64-kilobit electrically erasable and programmable read only memory as attribute memory.

FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level
- Program/erase operation by software command control
- Program/erase voltage 12V (common memory)
- 100,000 program/erase cycles
- Write protect switch

APPLICATIONS

- Notebook computers Printers
- Industrial machines

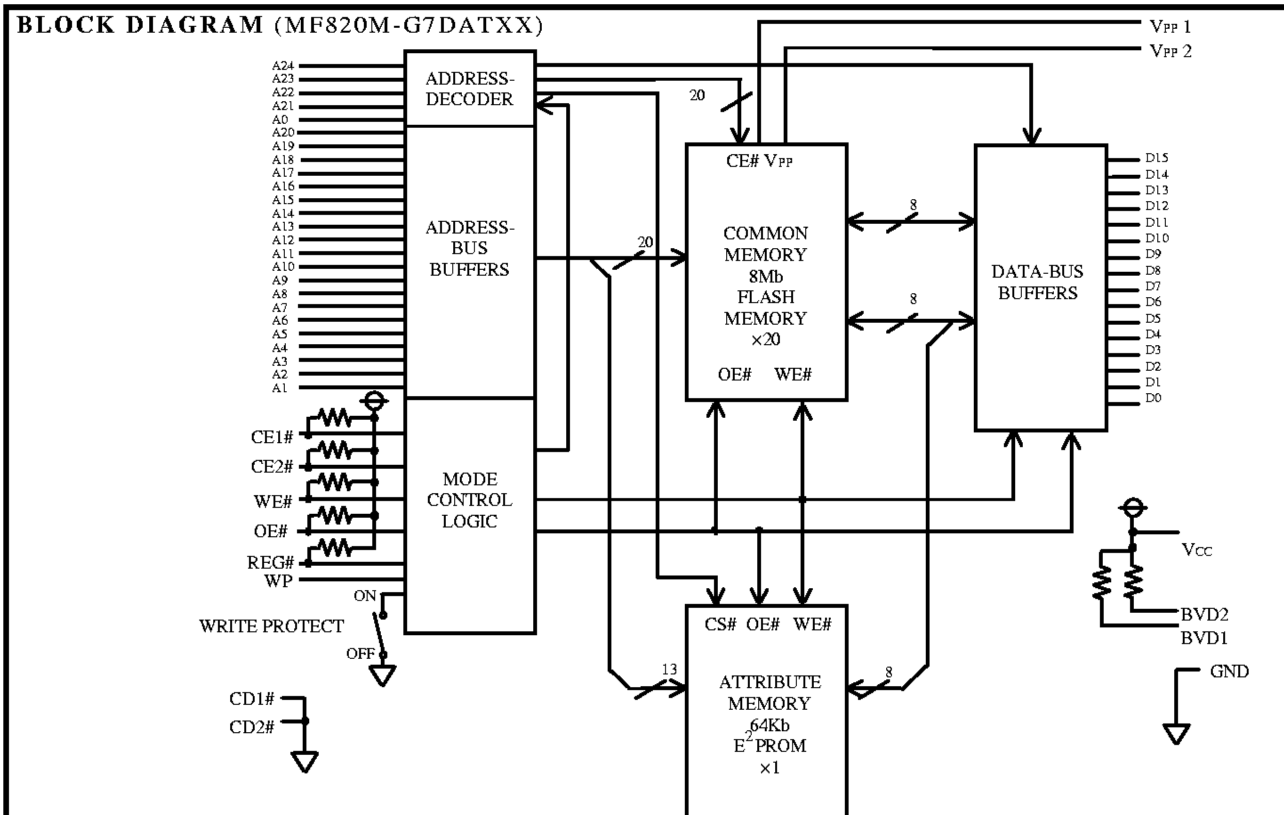
PRODUCT LIST

Type name \ Item	Memory capacity	Data bus width (bits)	Access time (ns)	Number of pins	Outline drawing
MF82M1-G7DATXX	2MB	8/16	200	68	68P-002
MF84M1-G7DATXX	4MB				
MF88M1-G7DATXX	8MB				
MF810M-G7DATXX	10MB				
MF816M-G7DATXX	16MB				
MF820M-G7DATXX	20MB				

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D3		36	CD1#	Card detect 1
3	D4		37	D11	
4	D5	Data I/O	38	D12	
5	D6		39	D13	Data I/O
6	D7		40	D14	
7	CE1#	Card enable 1	41	D15	
8	A10	Address input	42	CE2#	Card enable 2
9	OE#	Output enable	43	NC	
10	A11		44	NC	No connection
11	A9		45	NC	
12	A8	Address input	46	A17	
13	A13		47	A18	Address
14	A14		48	A19	input
15	WE#	Write enable	49	A20	
16	NC	No connection	50	A21	A21 (NC for ⇔ 2 MB types)
17	V_{CC}	Power supply voltage	51	V_{CC}	Power supply voltage
18	V_{PP} 1	Programming supply voltage 1	52	V_{PP} 2	Programming supply voltage 2
19	A16		53	A22	A22 (NC for ⇔ 4 MB types) Address
20	A15		54	A23	A23 (NC for ⇔ 8 MB types) input
21	A12		55	A24	
22	A7		56	NC	
23	A6		57	NC	
24	A5	Address input	58	NC	No connection
25	A4		59	NC	
26	A3		60	NC	
27	A2		61	REG#	Attribute memory select
28	A1		62	BVD 2	Battery voltage detect 2
29	A0		63	BVD 1	Battery voltage detect 1
30	D0		64	D8	
31	D1	Data I/O	65	D9	Data I/O
32	D2		66	D10	
33	WP	Write protect	67	CD2#	Card detect 2
34	GND	Ground	68	GND	Ground

BLOCK DIAGRAM (MF820M-G7DATXX)



FUNCTIONAL DESCRIPTION

The operating mode of the card is determined by five active low control signals (REG#, CE1#, CE2#, OE#, WE#), three supply voltages (VCC, VPP1, VPP2) and control registers located in each memory IC.

Common memory function

When the REG# signal is set to a high level common memory is selected.

Read only mode

When the voltages applied to both VPP1 and VPP2 are less than the voltage applied to VCC (i.e. VPP=0Vto VCC), the control registers of each memory IC are set to read only mode. Operation of the card then depends on the four possible combinations of CE1# and CE2# (note WE# should be set to a high level when the device is in read only mode except during combination (4) where it's condition is unimportant) :

(1) If CE1# is set to a low level and CE2# is set to a high level, the card will work as an eight bit data bus width card. Data can be accessed via the lower half of the data bus (D0 to D7).

(2) If both CE1# and CE2# are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.

(3) If CE1# is set to a high level and CE2# is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.

(4) If CE1# and CE2# are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When OE# is set to a low level data can be read from the card, depending on the address applied and the setting of CE1# and CE2# as mentioned above, except under combination (4)

When OE# is set to a high level and WE# is set to a high level the card is in an output disable mode and the data bus will be in a high impedance state regardless of the condition of CE1# and CE2#.

Read/write mode
When a programming voltage (VPPH) is applied to either or both of VPP1 and VPP2, read/write mode is enabled for the corresponding banks of memory IC's inside the card. VPP1 enables the Even Byte bank and VPP2 enables the Odd Byte bank.

By using the 4 combinations of CE1# and CE2#as described under Read only mode above the appropriate Data Out and Command/Data In bus selection can be made.

If OE# is set to a high level and WE# set to a low level, the control register will latch command data applied at the rising edge of the WE# signal. Note that more than one bus cycle may be required to latch the command and/or the related data-please refer to the Command Definition table.

If OE# is set to a low level and WE# is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details plese refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

Attribute memory
When the REG# signal is set to a low level attribute memory is selected.

The card includes a byte wide attribute memory consisting of 8K bytes of E^2PROM located at the even addresses when the card is in the 8 bit operating mode. It is located at sequential addresses on the lower half of the data bus when the card is in 16 bit operating mode i.e. A0 is ignored.

To access the attribute memory, first set CE1# and CE2#. Set CE1# to low level and CE2# to high level for 8 bit mode or CE1# and CE2# to low level for 16 bit mode. Then select the required address.Note please take care that in 8 bit mode A0 must be set low for attribute memory access i.e. an even address is applied. In 16 bit mode it is not important whether A0 is high or low. Data can then be read by setting OE# to a low level with WE set to a high level.

Writing to the attribute memory can be achieved in one of two ways, in byte mode or in page mode. The page mode write is a function which allows up to 32 bytes of data to be written in a single cycle. A page is defined as a block of 32 even bytes selected by addresses A6 through A13.

To write to attribute memory set OE# to high level and WE# to low level. The data to be written will be latched at the rising edge of WE#. Then, unless WE# changes back from high level to low level within 30 μs an automatic erase/program operation starts which will complete within 10ms.

If WE# makes a transition back from high to low level within 30μs of the first data being latched then further bytes from a page of up to 32 bytes can be latched with further WE# low to high transitions. The latching operation is repeated until all bytes are loaded at which point holding WE# high for greater than 30μs will initiate execution of a page erase/program operation which will complete within 10ms.

During page write data loading operations all data must be addressed within one 32 byte page i.e. the page address which is selected by A6 through A13 and must remain constant throughout the data load. Please also remember that for attribute memory A0 is not applicable and it should be set to low, even addressing only, in 8 bit mode or ignored for 16 bit mode.

Write protect mode
The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and VCC is applied. When the card is not in write protect mode the WP output pin is set to a low level when VCC is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.

FUNCTION TABLE (COMMON MEMORY)

Mode	REG#	CE2#	CE1#	OE#	WE#	A0	VPP2	VPP1	I/O (D15 to D8)	I/O (D7 to D0)
Standby	H	H	H	X	X	X	VPPX	VPPH	High-Z	High-Z
	H	H	H	X	X	X	VPPH	VPPX	High-Z	High-Z
Read A (16-bit)	H	L	L	L	H	X	VPPH	VPPH	Odd byte data out	Even byte data out
Read B (8-bit)	H	H	L	L	H	L	VPPX	VPPH	High-Z	Even byte data out
	H	H	L	L	H	H	VPPH	VPPX	High-Z	odd byte data out
Read C (8-bit)	H	L	H	L	H	X	VPPH	VPPX	Odd byte data out	High-Z
Write A (16-bit)	H	L	L	H	L	X	VPPH	VPPH	Command or odd byte data in	Command or even byte data in
Write B (8-bit)	H	H	L	H	L	L	VPPX	VPPH	High-Z	Command or even byte data in
	H	H	L	H	L	H	VPPH	VPPX	High-Z	Command or odd byte data in
Write C (8-bit)	H	L	H	H	L	X	VPPH	VPPX	Command or odd byte data in	High-Z
Output disable	H	X	X	H	H	X	VPPH	VPPX	High-Z	High-Z
	H	X	X	H	H	X	VPPX	VPPH	High-Z	High-Z

Note 2 : H=VIH, L=VIL, X=VIH or VIL, VPPX=VPPL or VPPH, High-Z= High-impedance
To operate refer to the command definition, algorithms and so on.

FUNCTION TABLE (ATTRIBUTE MEMORY)

Mode	REG#	CE2#	CE1#	OE#	WE#	A0	VPP2	VPP1	I/O (D15 to D8)	I/O (D7 to D0)
Standby	L	H	H	X	X	X	Vcc	Vcc	High-Z	High-Z
Read A (16-bit)	L	L	L	L	H	X	Vcc	Vcc	Data out (not valid)	Even byte data out
Read B (8-bit)	L	H	L	L	H	L	Vcc	Vcc	High-Z	Even byte data out
	L	H	L	L	H	H	Vcc	Vcc	High-Z	Data out (not valid)
Read C (8-bit)	L	L	H	L	H	X	Vcc	Vcc	Data out (not valid)	High-Z
WriteA (16-bit)	L	L	L	H	L	X	Vcc	Vcc	Odd byte data in (not valid)	Even byte data in
Write B (8-bit)	L	H	L	H	L	L	Vcc	Vcc	High-Z	Even byte data in
	L	H	L	H	L	H	Vcc	Vcc	High-Z	Odd byte data in (not valid)
Write C (8-bit)	L	L	H	H	L	X	Vcc	Vcc	Odd byte data in (not valid)	High-Z
Output disable	L	X	X	H	H	X	Vcc	Vcc	High-Z	High-Z

COMMAND DEFINITION

When either or both $V_{PP}1$ and $V_{PP}2$ are applied the programming voltage ($V_{PP}H$) the corresponding memories of the card are set to read/write mode and the operation is controled by the software command written in the control register.

COMMAND DEFINITION TABLE

Command	Bus cycles	First bus cycle			Second bus cycle			
		Mode	Address	Data in	Mode	Address	Data in	Data out
Read/Reset	1	Write	ZA	FFh(FFFFh)	↳	↳	↳	↳
Programme Setup/ Programme	2	Write	PA	40h(4040h)	Write	PA	PD	↳
Erase Setup/ Erase Confirm	2	Write	BA	20h(2020h)	Write	BA	D0h(DD00h)	↳
Erase Suspend/ Erase Resume	2	Write	BA	B0h(B0B0h)	Write	BA	D0h(D0D0h)	↳
Read Status Register	2	Write	ZA	70h(7070h)	Read	↳	↳	RD
Clear Status Register	1	Write	ZA	50h(5050h)	↳	↳	↳	↳
Read Device Identifier Code	2	Write	ZA	90h(9090h)	Read	DIA	↳	DID

Note 3. Indicates the basic functions of commands. Refer to the algorithms to operate.
Signal status is defined in function table and bus status.
Parenthesized data shows the data for 16 bit mode operation.
ZA=an address of a memory zone (Please reser to the memory zone)
PA=Programming address
PD=Programming data
BA=An address of a memory block (Please refer to the memory block)
RD=Data of status Register
DIA=Device identifier address
000000h for manufacturer code 000002h for device code
DID=Device identifier data
manufacturer code : 89h (8989h) device code : A2h (A2A2h)

Read/Reset
The memory in the card is switched to read mode by writing FFh (FFFFh for 16 bit operation) into the control resister. This mode is maintained until the contents of register are changed. This mode have nothing to do with the voltage of VPP. This mode needs to be written to every memory zone to which access is required.

Programme Setup/Programme
The setup programme command sets up the card for programming. It is applied when 40h (4040h for 16 bit operation) is written to control register. Programming will take place automatically after latching the address and data which are applied at the rising edge of WE#.
The completion of programme can be confirmed by reading status register. after writing Read status register command 70h (7070h for 16 bit operation) to control register.
(For details please refer to the algorithm)

Erase Setup/Erase confirm
The erase setup is a command to set up the memory block for erasure. Writing setup erase command 20h (2020h for 16 bit operation) in the control register followed by erase confirm command D0h (D0D0h for 16 bit operation) will initiate a erasure operation. Eraseing will take place automaticaly after the rising edge of WE# controlled by a internal timer.
Thecompletion of erase can be confirmed by reading status register, after writing read status register command 70h (7070h for 16 bit operation) to control register.
(For details please refer to the algorithm)
These commands will not erase all the data of a memory card and should be repeated for all the required memory blocks. At an eight bit access mode it should be noticed that the erasure of a memory block will result in odd byte or even byte erasure.

Erase Suspend/Erase Resume
The erase suspend command B0h (B0B0h for 16 bit operation) is a command to generate erase interruption and to read data from another block of selected memory zone.
By writing in the control register erase resume command D0h (D0D0h for 16 bit operation), the memory block will continue the eraseoperation.
These commands must be executed in erase algorithm.
(For details please refer to the algorithm)

Read Status Register
The Read status register is a command to read the status register's data and to make sure programme or earse operations complete successfully. The data of status register can be read after writing 70h (7070h for 16 bit operation) in the control register. The register's read data is latched on the falling edge of OE#. At programme or erase, the status register's data must be read to verify the results.

Clear Status Register
The clear status register command will clear data of status ragister. It is applied when 50h (5050h for 16 bit operation) is written to the control register.
If an error occured during programme or erase, the status register must be cleared before retrying programme or erase.

Read Device Identifier Codes
The read device identifier codes command is implemented by writing 90h (9090h for 16 bit operation) to the command register. After writing the command, manufacturer code can be read at the address of 000000h of the zone and device code can be read at the address 000002h of the zone. Each card uses the same type of memory throughout and each memory zone will respond the same code.
(Do not apply high voltage to A10 pin in order to try and read the device identifier codes as this will result in the card being destroyed.)

STATUS REGISTER

When operating programme or erase, it is necessary to read status register data and to transact these bit. Each memory IC used in this card has internal status register to make sure programme or erase operations complete successfully.

7 (15) BIT	6 (14) BIT	5 (13) BIT	4 (12) BIT	3 (11) BIT	2 to 0 (10 to 8) BIT
Programme/ Erase Status Bit	Erase Suspend Bit	Erase Error Bit	Programme Error Bit	V_{PP} Error Bit	Reserved

Note 4. ( ) ; for 16 bit operation

Bit ; Field name

7(15) BIT ; Programme/Erase Status Bit
0=Busy (in programming/erasing)
1=Ready

6(14) BIT ; Erase Suspend Bit
1=Erase Suspended

5(13) BIT ; Erase Error Bit
1=Erase Error

Bit ; Field name

4(12) BIT ; Programme Error Bit
1=Programme Error

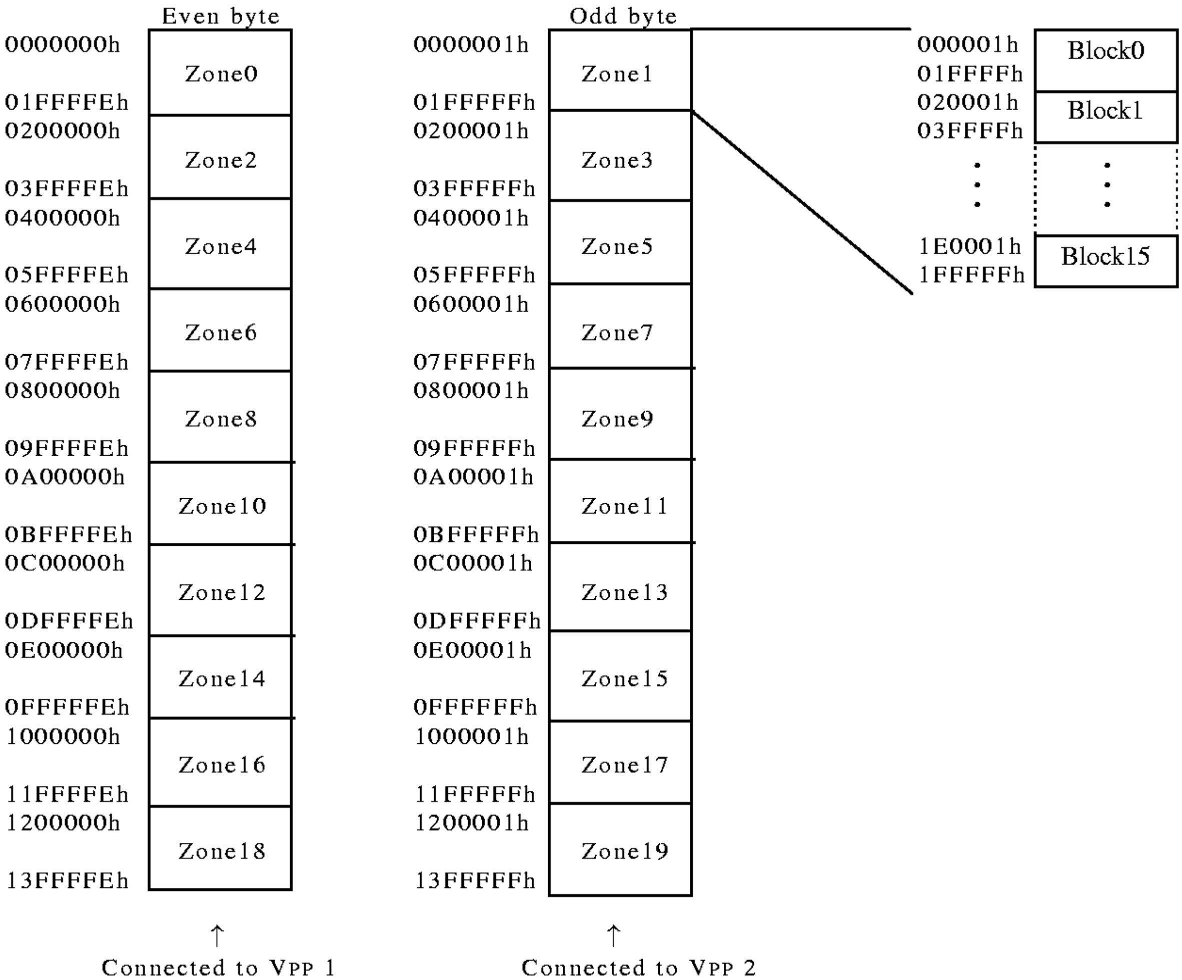
3(11) BIT ; V_{PP} Error
1=Error of voltage at V_{PP}

2 to 0
(10 to 8) BIT ; Reserved for future

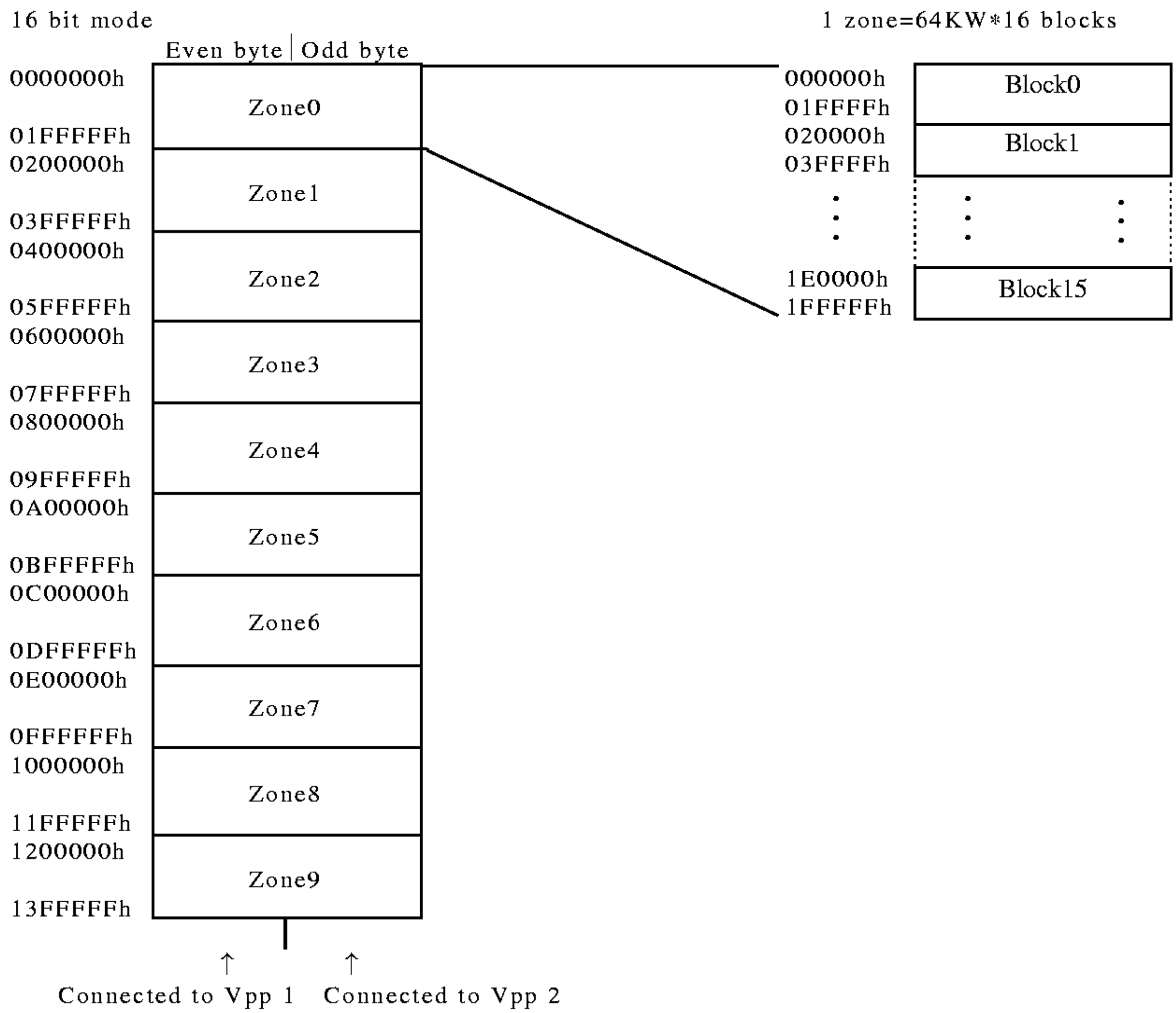
MEMORY ZONE AND BLOCK

8 bit mode

1 zone=64KB*16 blocks



Zone 2 to 19 do not exist in 2MB
Zone 4 to 19 do not exist in 4MB
Zone 8 to 19 do not exist in 8MB
Zone 10 to 19 do not exist in 10MB
Zone 16 to 19 do not exist in 16MB



Zone 1 to 9 do not exist in 2MB
Zone 2 to 9 do not exist in 4MB
Zone 4 to 9 do not exist in 8MB
Zone 5 to 9 do not exist in 10MB
Zone 8 to 9 do not exist in 16MB

PROGRAMME SEQUENCE

8 bit Operation
First apply VPPH to VPP1 and/or VPP2. Then the write programme setup command (40h) to the address to be programmed. The next write sequence will initiate the programming operation which will end automatically as this period being controlled by an internal timer and the data will be programmed. To make sure that the data is programmed correctly write a read status register command (70h) and read data. (Reading should be waited more than 6μs after the programme setup command)
If the data is programed step address and program me data according to the above sequence.
The next address to be programmed should be written with in a memory zone whose VPP voltage is set to VPPH. If not write the reset command (FFh) and then drop the VPP voltage to VPPL.
Then apply VPP for the desired memory zone and proceed with programming.
In applications where VPP1 and VPP2 are shorted together all addresses can be programmed without there being any need for the programming algorithm to take account of the cards memory zone architecture.

16 bit operation
The algorithm of 16 bit programming is almost same as the 8 bit programming. (Please refer to the algorithm and the status of bus at programming)

ERASE SEQUENCE

ERASE

8 bit Operation
First apply VPPH to VPP1 and/or VPP2. Then write the erase setup command (20h) and erase cofirm command (D0h) for the applicable block address.
An erasure operation will then commence which will be finished in 1.6s typical or less this being automatically controlled by an internal timer.
To make sure that the data is erased correctly write the read status register command (70h) and read data (Reading should be waited more than 300ms after the erase confirm command).
After erasure has been completed write the reset command (FFh) to the control register,

set VPP1 and /or VPP2 to VPP L as applicable and proceed

with the erase operation for the next memory block.

16 bit Operation
Most of the algorithm of 16 bit erasure is same as the one of the 8 bit erasure.
(Please refer to the algorithm and the state of bus at erasure.)

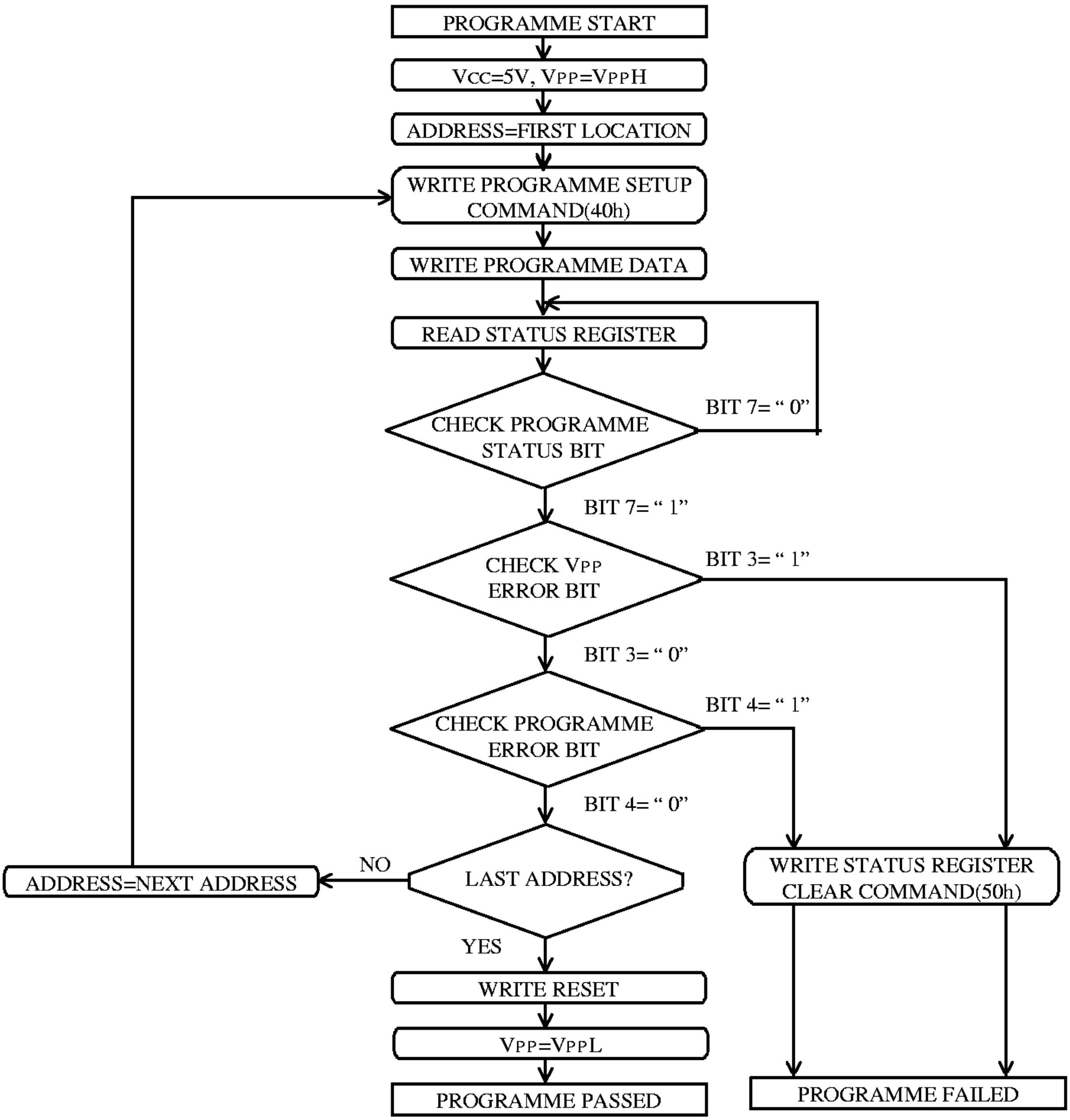
ERASE SUSPEND

8 bit Operation
The erase suspend is a command to generate block erase interruption in order to read data from another block of the selected memory zone. It is necessary to write the erase suspend command (B0h) in the erase algorithm. The excecution of the erase suspend can be confirmed by reading data of the status register, after writing the read status register command (70h).
Then it is necessary to write the read command (FFh) in control register in order to read data, after reading the status register's data.
After the erase resume command (D0h) is written in the control register, the memory block will continue erase operation.

16 bit Operation
Most of the algorithm of 16 bit erase suspending is same as the one of the 8 bit erase suspending.
(Please refer to the algorithm and the state of bus at erase suspending.)

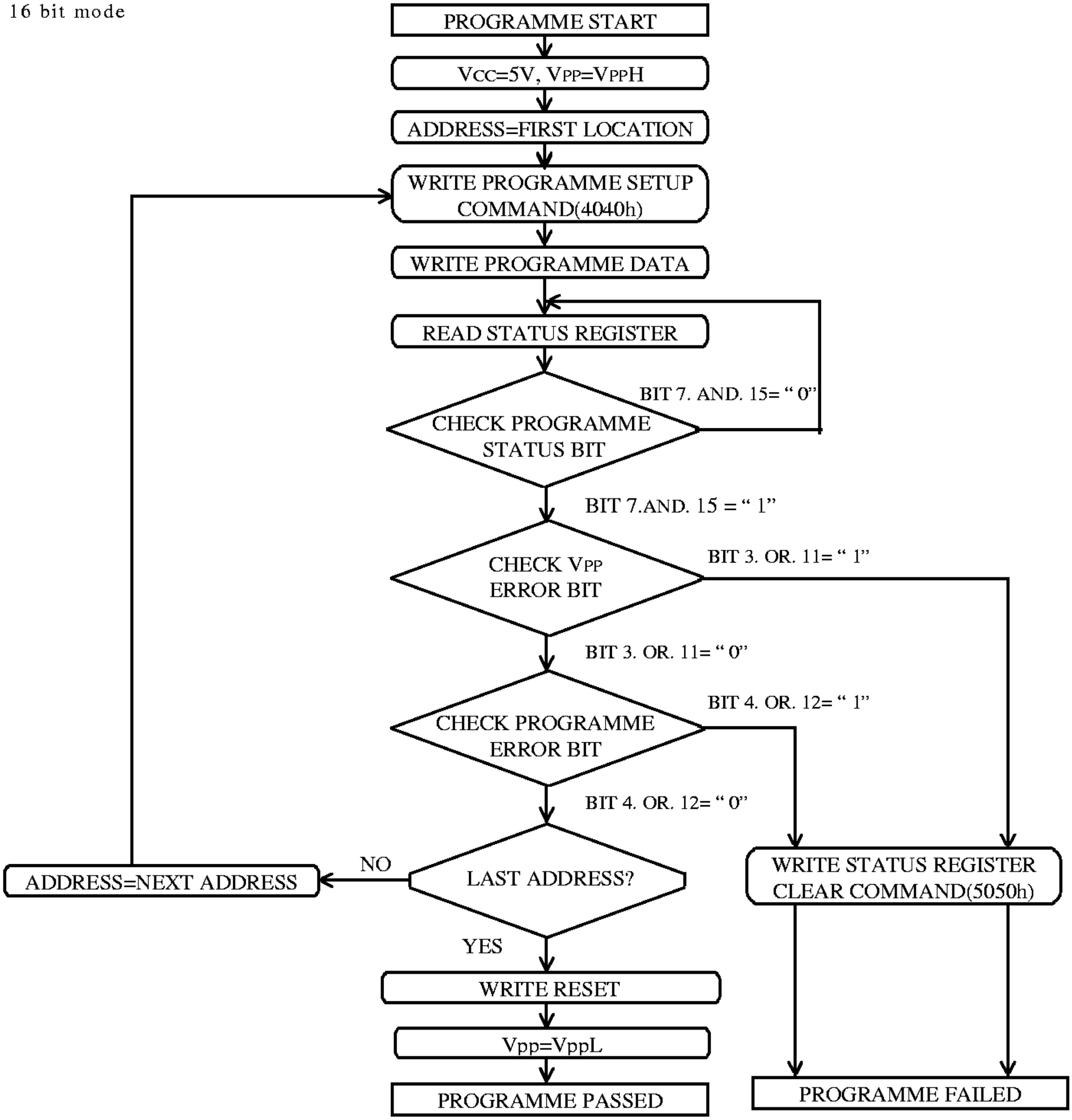
PROGRAMME ALGORITHM

8 bit mode



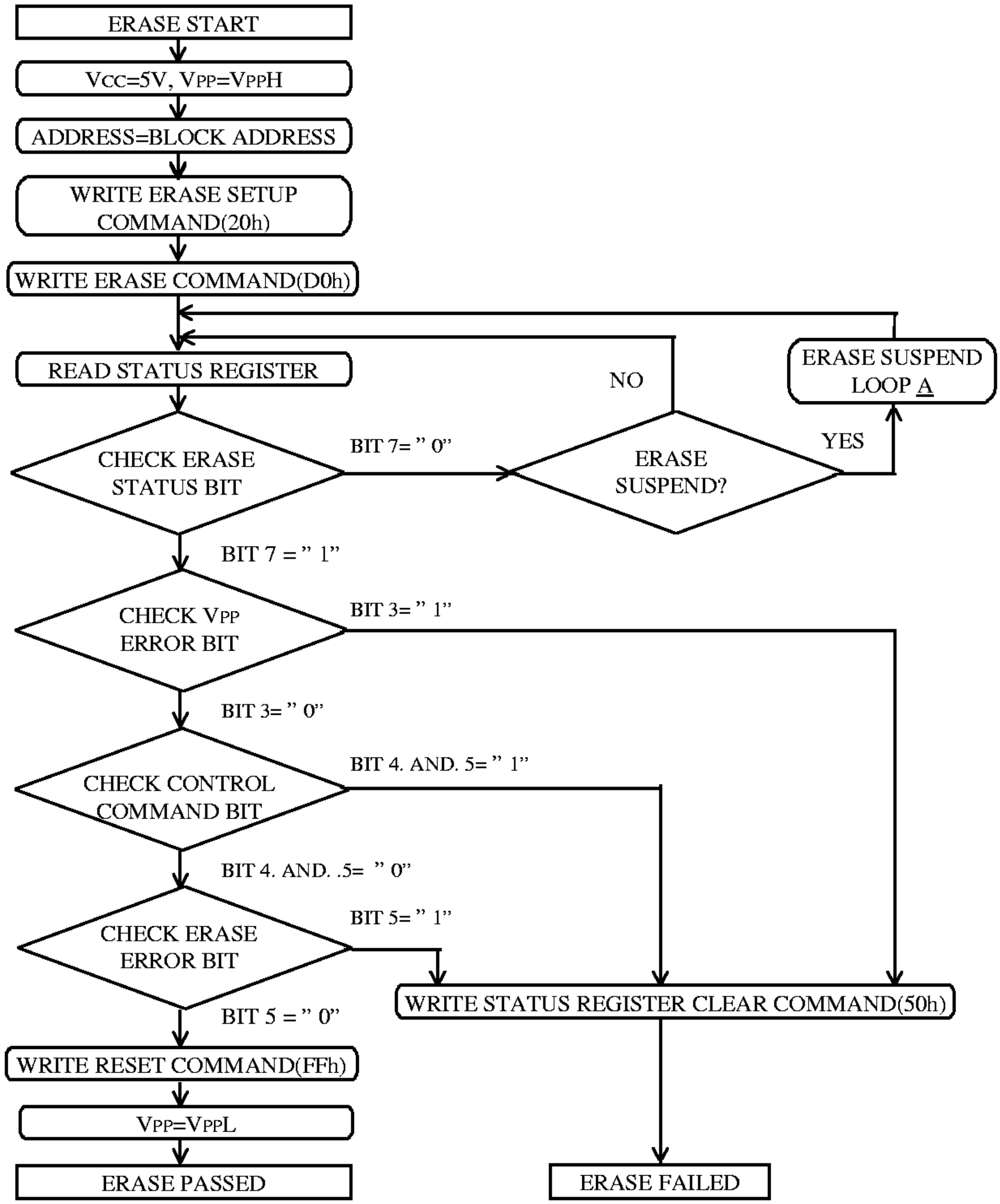
Note 5. . This is programme algorithm for a memory zone and not for a card.
. If VPP error bit is detected, try to programme again at VPPH level.

PROGRAMME ALGORITHM
16 bit mode

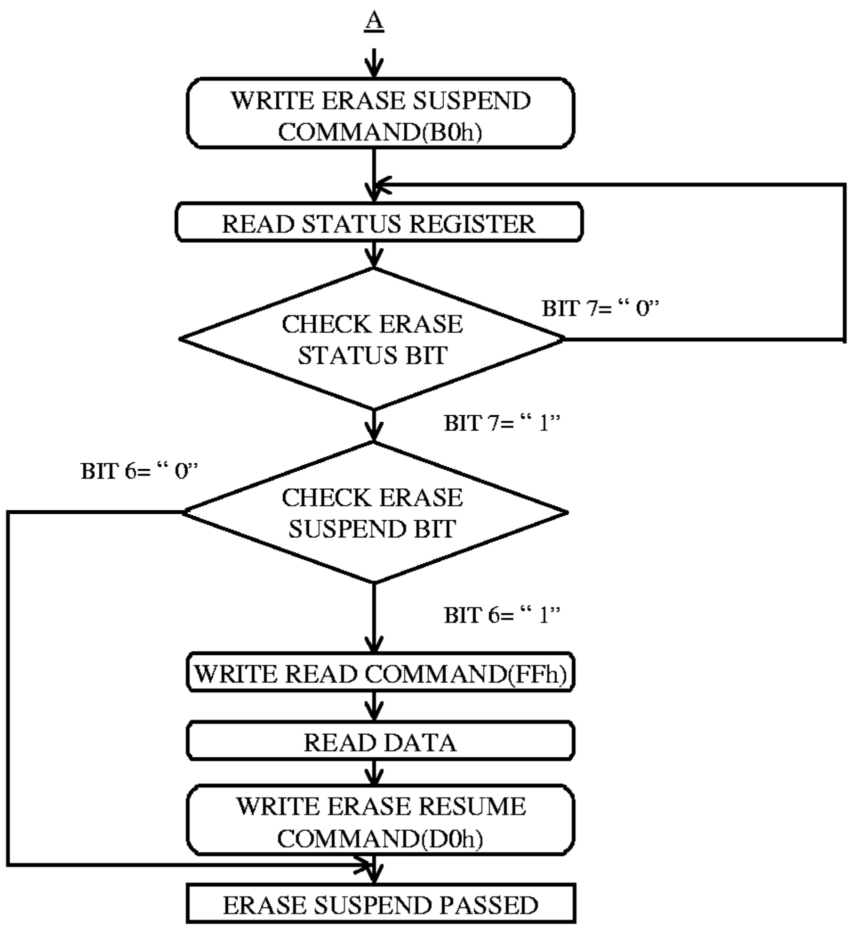


Note 6. If VPP error bit is detected, try to programme again at VPPH level.
. This is programme algorithm for a memory zone and not for a card.
. . OR. : =Logical or ; . AND. : =Logical and

ERASE ALGORITHM
8 bit mode



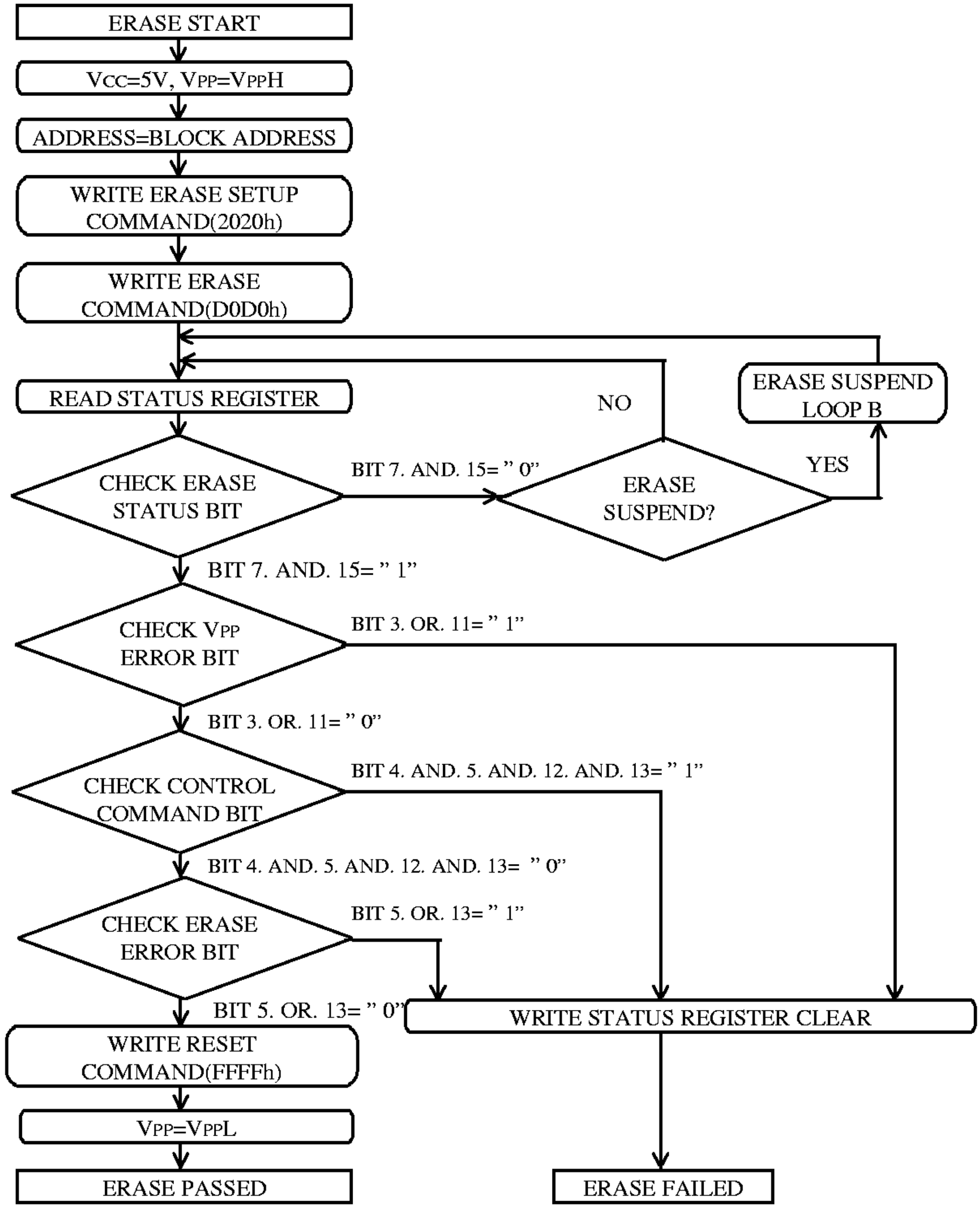
Note 7. If VPP error bit is detected, try to programme again at VPPH level.
. This is an erase algorithm for a memory block and not for a card.
. . OR. : = Logical or



Note 8. Reading data from block other than the suspended block the in zone generating erase suspend.

ERASE ALGORITHM

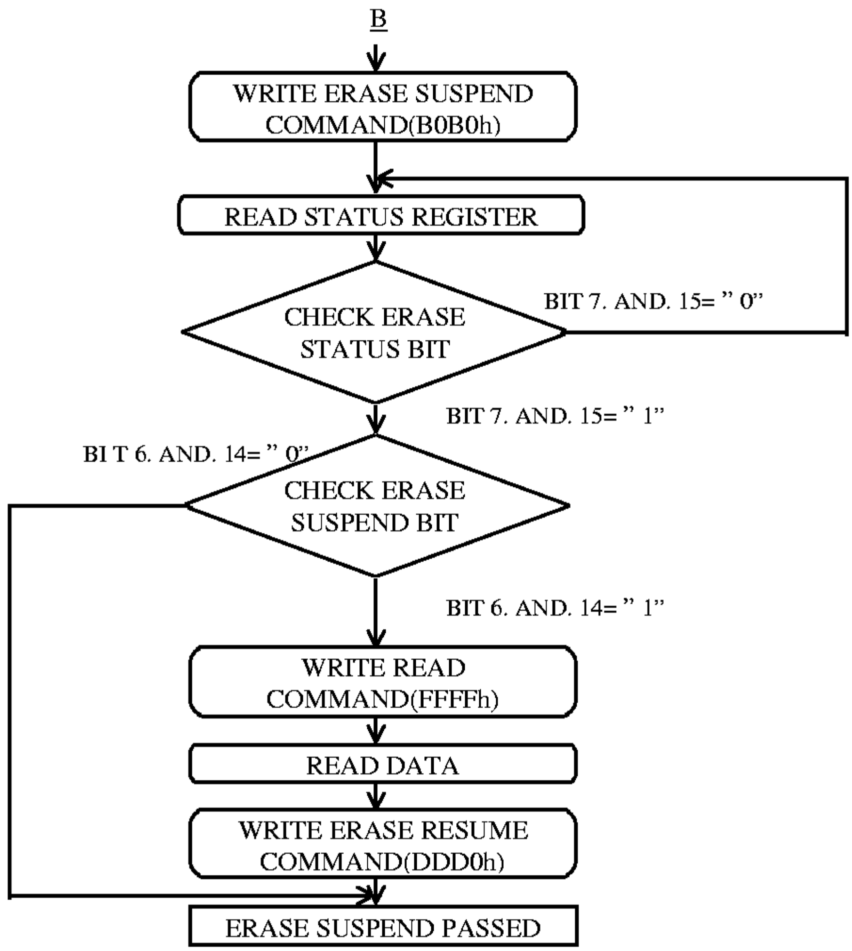
16 bit mode



Note 9. If VPP error bit is detected, try to programme again at VPPH level.

. This is an erase algorithm for a memory block and not for a card.

. . OR. : =Logical or ; . AND. : =Logical and



Note 10. Reading data from block other than the suspended block the in zone generating erase suspend.
. AND. : =Logical and

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	V_{CC} Supply voltage	With respect to GND	-0.5 to 6.0	V
V_{PP}	V_{PP} Supply voltage		-0.5 to 14.0	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		0 toV_{CC}	V
T_{opr}	Operating temperature	Read/Write Operation	0 to70	°C
T_{stg}	Storage temperature		-40 to 80	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0 to 55°C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	V_{CC} Supply voltage		4.75	5.0	5.25	V
V_{PPL}	V_{PP} Supply voltage during READ only mode		0	V_{CC}	V_{CC}+1.0	V
V_{PPH}	V_{PP} Supply voltage during READ WRITE mode		11.4	12.0	12.6	V
V_{IH}	High input voltage		2.4		V_{CC}	V
V_{IL}	Low input voltage		0		0.8	V
N_{ACT}	Number of simultaneous activated memory zones/blocks	Programme			1	Zone
		Erase			1	Block

ELECTRICAL CHARACTERISTICS

Ta=0 to 55°C, V_{CC}=5V+/-5%, V_{PP}=V_{PPL} or V_{PPH}, unless otherwise noted)

Symbol	Parameter	Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High output voltage	I_{OH}=-0.1mA, BVDn		2.4			V
		I_{OH}=-1.0mA, Other outputs		2.4			
V_{OL}	Low output voltage	I_{OL}=2mA		0		0.4	V
I_{IH}	High input current	V_I=V_{CC} V				10	μA
I_{IL}	Low input current	V_I=0V	CE1#, CE2#, OE#, WE#, REG#	-10		-70	μA
			Other inputs			-10	
I_{OZH}	High output current in off state	CE1#=CE2#=V_{IH} or OE#=V_{IH},V_O(Dm)=V_{CC}				10	μA
I_{OZL}	Low output current in off state	CE1#=CE2#=V_{IH} or OE#=V_{IH}, V_O(Dm)=0V				-10	μA
I_{CC} 1 • 1	Active V_{CC} supply current 1	CE1#=CE2#=V_{IL}, Other inputs=V_{IH} or V_{IL}, Outputs=open			100	200	mA
I_{CC} 1 • 2	Active V_{CC} supply current 2	CE1#=CE2# ≤ 0.2V, Other inputs ≤ 0.2V or ≥ V_{CC}-0.2V, Outputs=open			90	180	mA
I_{CC} 2 • 1	Standby V_{CC} supply current 1	CE1#=CE2#=V_{IH}, Other inputs=V_{IH} or V_{IL}	2MB			9.0	mA
			4MB			13	
			8MB			21	
			10MB			25	
			16MB			37	
			20MB			45	
I_{CC} 2 • 2	Standby V_{CC} supply current 2	CE1#=CE2# ≥ V_{CC}-0.2V, Other inputs ≤ 0.2V or ≥ V_{CC}-0.2V	2MB		0.1	1.2	mA
			4MB		0.2	1.4	
			8MB		0.4	1.8	
			10MB		0.5	2.0	
			16MB		0.7	2.6	
			20MB		0.8	3.0	
I_{PP} 1	V_{PP} supply current 1 (each V_{PP} pin)	V_{PP}=V_{PPL} ≤ V_{CC}	2MB		10	20	μA
			4MB		20	30	
			8MB		30	50	
			10MB		40	60	
			16MB		50	90	
			20MB		70	110	
I_{PP} 2	V_{PP} supply current 2 (each V_{PP} pin)	V_{PP}=V_{PPH} (standby, read)	2MB			0.3	mA
			4MB			0.5	
			8MB			0.9	
			10MB			1.1	
			16MB			1.7	
			20MB			2.1	
I_{PP} 3	V_{PP} supply current 3 (each V_{PP} pin)	V_{PP}=V_{PPH} (programme, erase)			10	35	mA

Note 11. Currents flowing into the card are taken as positive (unsigned).
Typical values are measured at V_{CC}=5.0V, V_{PPL}=5V, V_{PPH}=12V, Ta=25°C.
The card consumes active current at programming, erasure even if both CE1# and CE2# are high level.

CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_i	Input capacitance	V_I=GND, v_i=25mVrms, f=1 MHz, Ta=25°C			45	pF
C_o	Output capacitance	V_I=GND, v_o=25mVrms, f=1 MHz, Ta=25°C			45	pF

Note 12 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS (COMMON MEMORY)

Read Cycle (Ta=0 to 55°C, V_{CC}=5V+/-5%, V_{PP}=V_{PPL} or V_{PPH}, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{RC}	Read cycle time	200			ns
$t_{a(A)}$	Address access time			200	ns
$t_{a(CE)}$	Card enable access time			200	ns
$t_{a(OE)}$	Output enable accese time			100	ns
$t_{dis(CE)}$	Output disable time (from CE#)			90	ns
$t_{dis(OE)}$	Output disable time (from OE#)			90	ns
$t_{en(CE)}$	Output enable time (from CE#)	5			ns
$t_{en(OE)}$	Output enable time (from OE#)	5			ns
$t_{V(A)}$	Data valid time after address change	0			ns

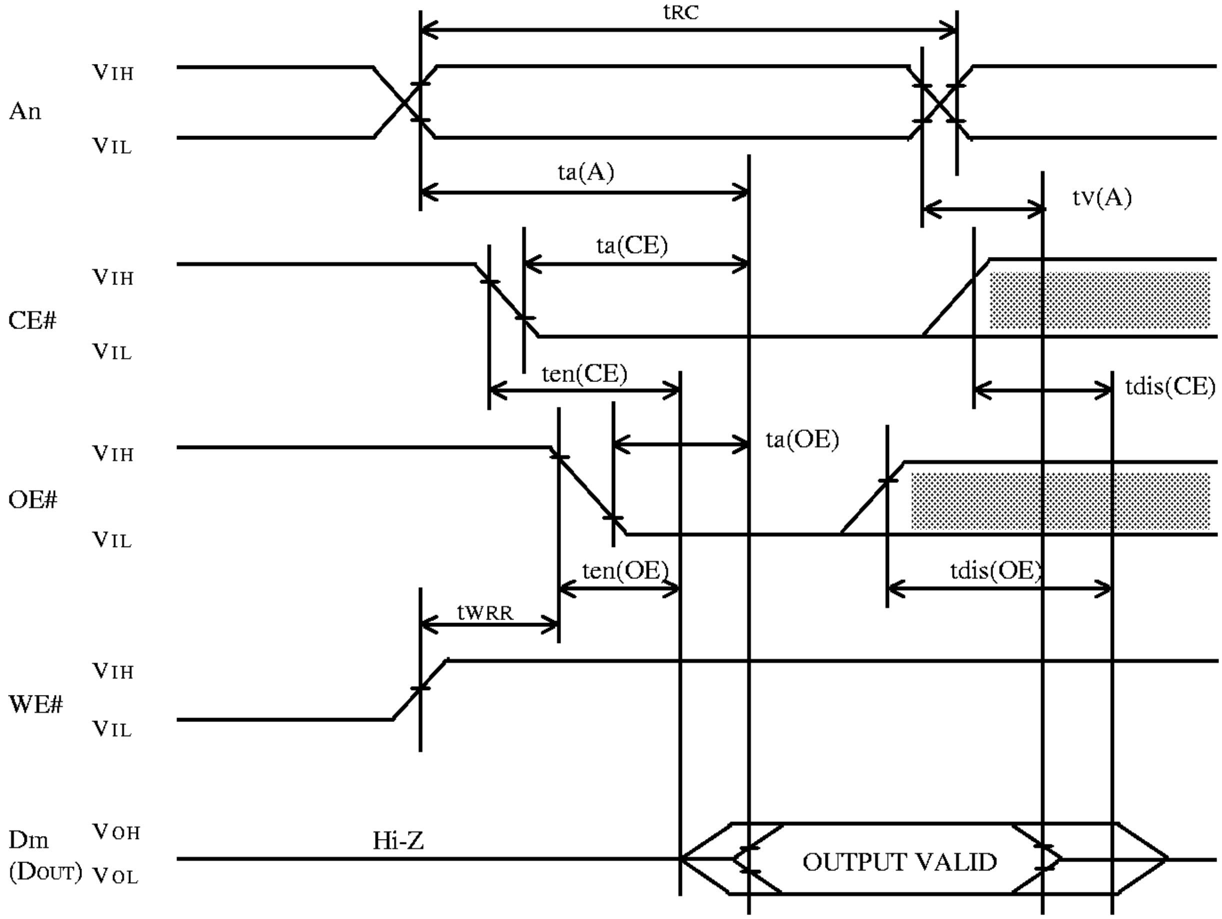
TIMING REQUIREMENTS (COMMON MEMORY)

Write Cycle (Ta=0 to 55°C, V_{CC}=5V+/-5%, V_{PP}=V_{PPH}, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{WC}	Write cycle time	200			ns
t_{AS}	Address setup time	20			ns
t_{AH}	Address hold time	30			ns
t_{DS}	Data setup time	60			ns
t_{DH}	Data hold time	30			ns
t_{WRR}	Write recovery time before read	10			ns
t_{CS}	Card enable setup time before write	20			ns
t_{CH}	Card enable hold time	30			ns
t_{WP}	Write pulse width	120			ns
t_{WPH}	Write pulse width high	40			ns
t_{DP}	Duration of programming operation	6			µs
t_{DE}	Duration of erase operation	300			ms
t_{VSC}	V_{PP} setup time to card enable low	1			µs
t_{VRW}	V_{PP} recovery time to card enable high	150			ns
t_{ASH}	Address setup time to write enable high	140			ns

Note 13 : Refer to switching characteritics for read parameters

TIMING DIAGRAM
Common Memory Read

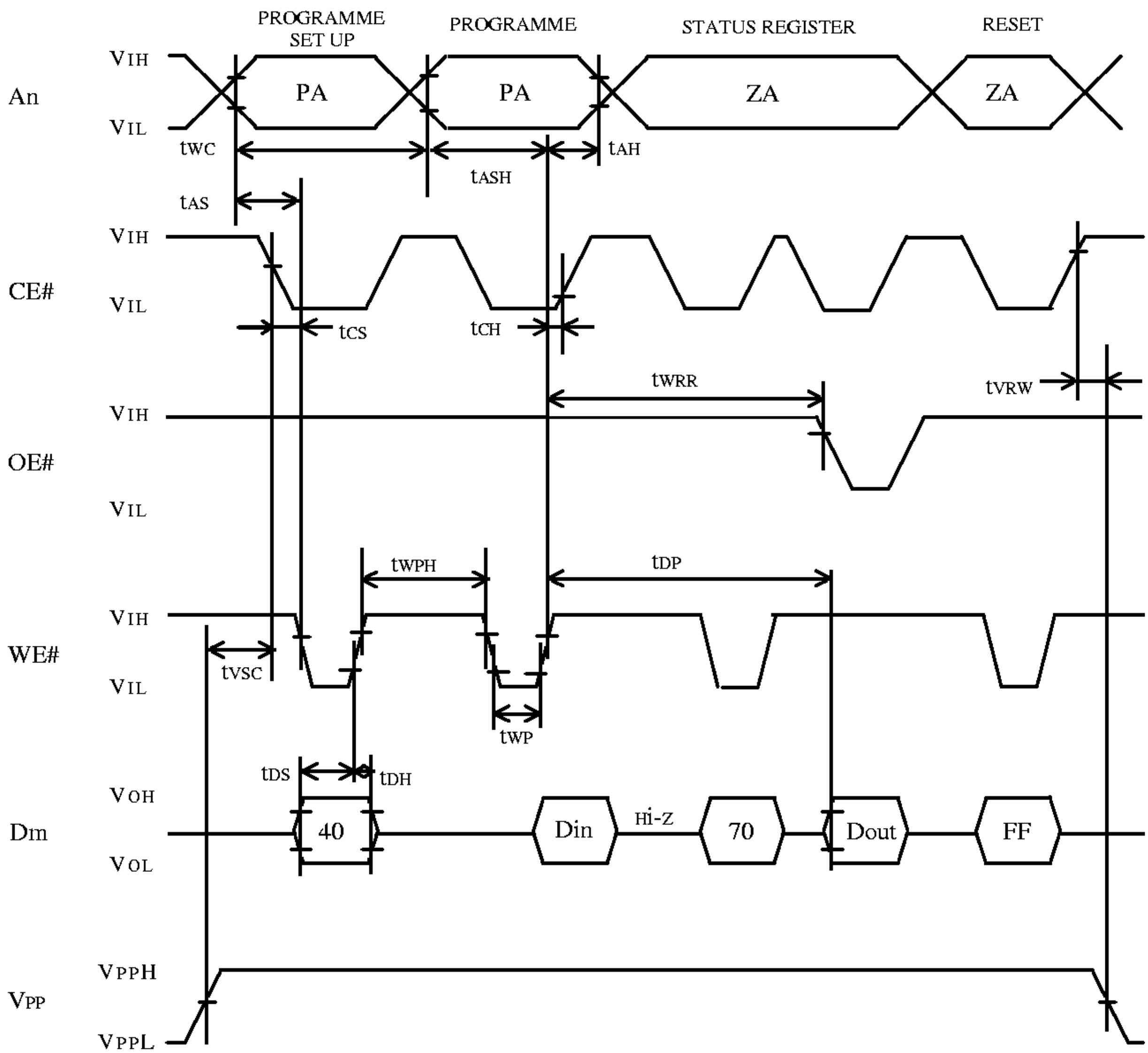


REG# ="H" level

Note 14: [shaded box] Indicates the don't care input.

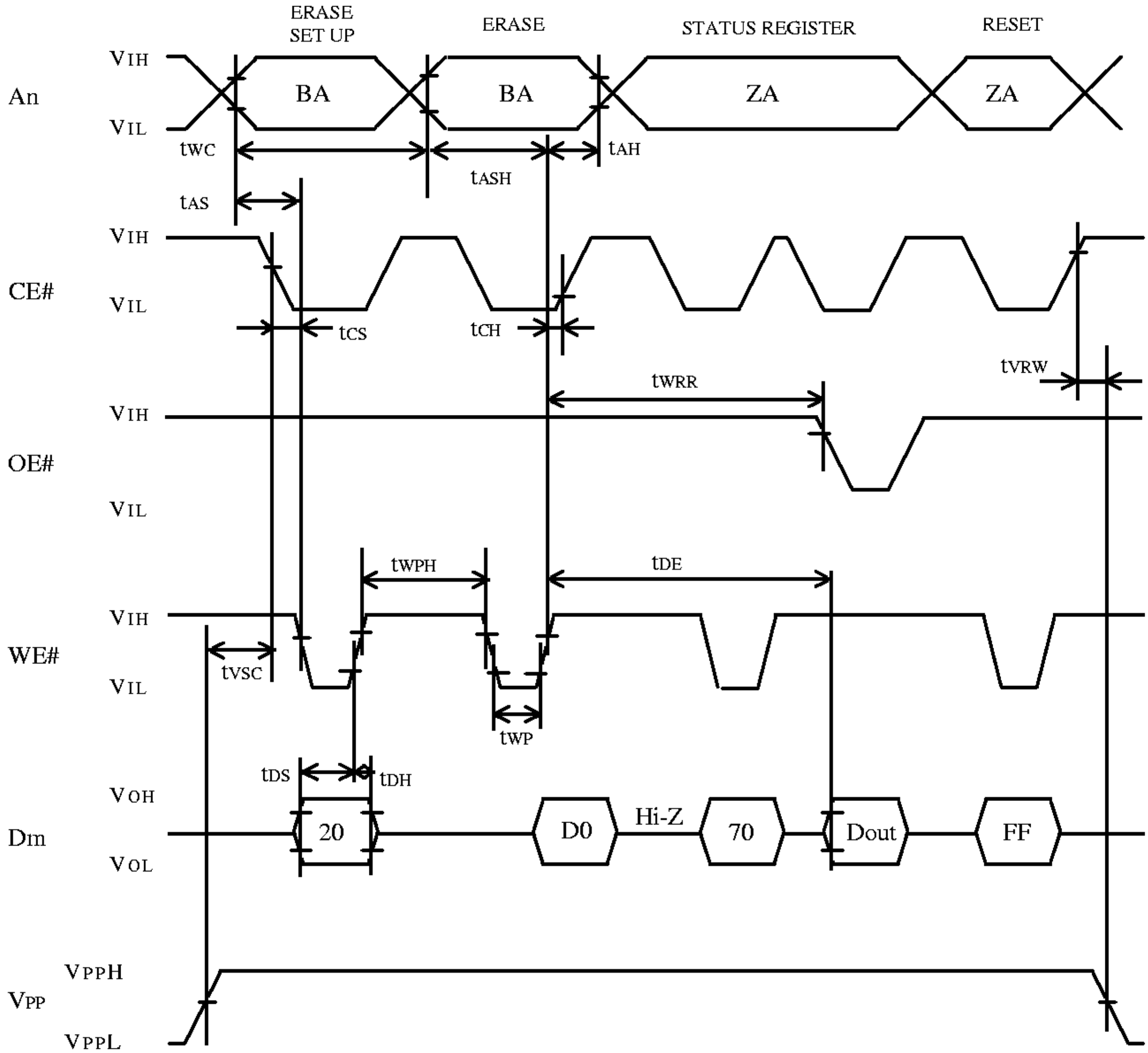
TIMING DIAGRAM (COMMON MEMORY)

Programme Mode



REG# ="H" level

TIMING DIAGRAM (COMMON MEMORY)
Erase Mode



REG# ="H" level

SWITCHING CHARACTERISTICS

Read Cycle (Ta=0 to 55°C, VCC=5V+/-5%, VPP=VCC, unless otherwise noted)

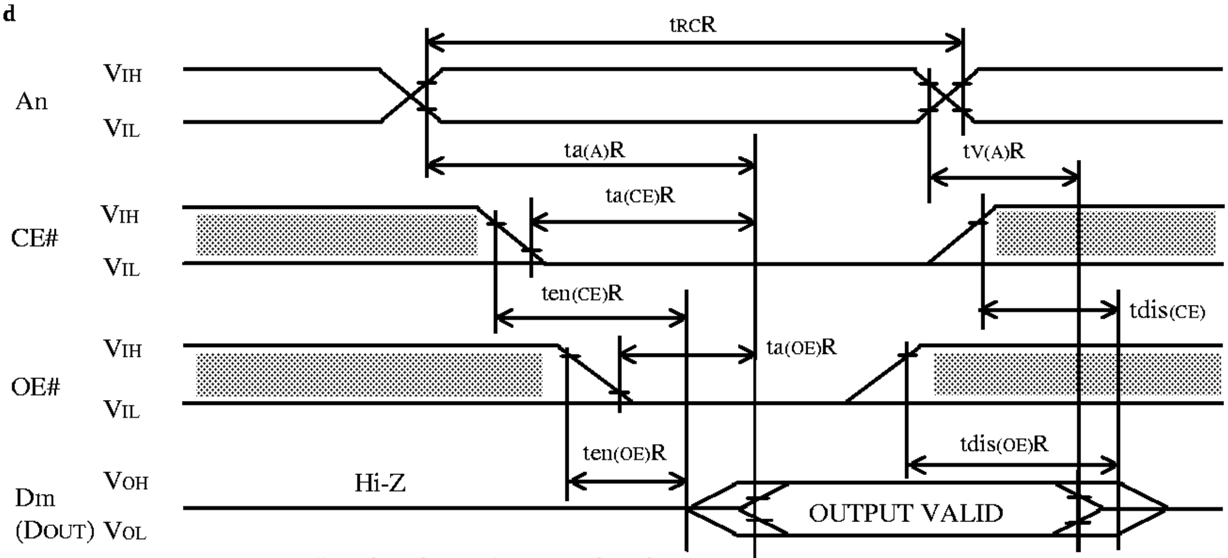
Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tRCR	Read cycle time	300			ns
ta(A)R	Address access time			300	ns
ta(CE)R	Card enable access time			300	ns
ta(OE)R	Output enable access time			150	ns
tdis(CE)R	Output disable time (from CE#)			100	ns
tdis(OE)R	Output disable time (from OE#)			100	ns
ten(CE)R	Output enable time (from CE#)	5			ns
ten(OE)R	Output enable time (from OE#)	5			ns
tv(A)R	Data valid time after address change	0			ns

TIMING REQUIREMENTS (ATTRIBUTE MEMORY)

Write Cycle (Ta=0 to 55°C, VCC=5V+/-5%, VPP=VCC, unless otherwise noted)

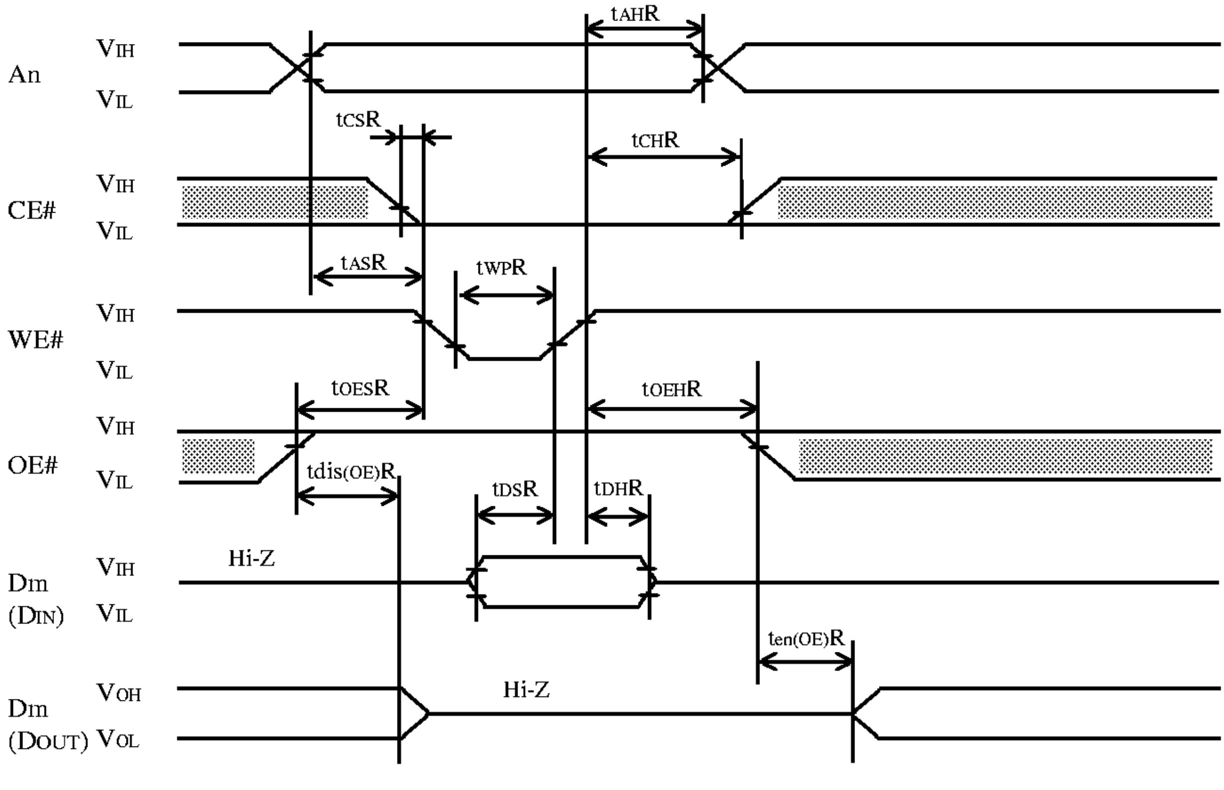
Symbol	Parameter	Limits			
		Min.	Typ.	Max.	
tASR	Address setup time	30			ns
tAHR	Address hold time	30			ns
tCSR	CE setup time	40			ns
tCHR	CE hold time	30			ns
tDSR	Data setup time	120			ns
tDHR	Data hold time	40			ns
tOESR	OE setup time	30			ns
tOEHR	OE hold time	40			ns
tWPR	Write pulse width	170			ns
tDLR	Data latch time	120			ns
tBLR	Byte load cycle time	0.3		30	µs
tWCR	Write cycle time	10			ms
ten(OE)R	Output enable time (from OE#)	5			ns
tdis(OE)R	Output disable time (from OE#)	0		100	ns

TIMING DIAGRAM (Attribute Memory)
Read



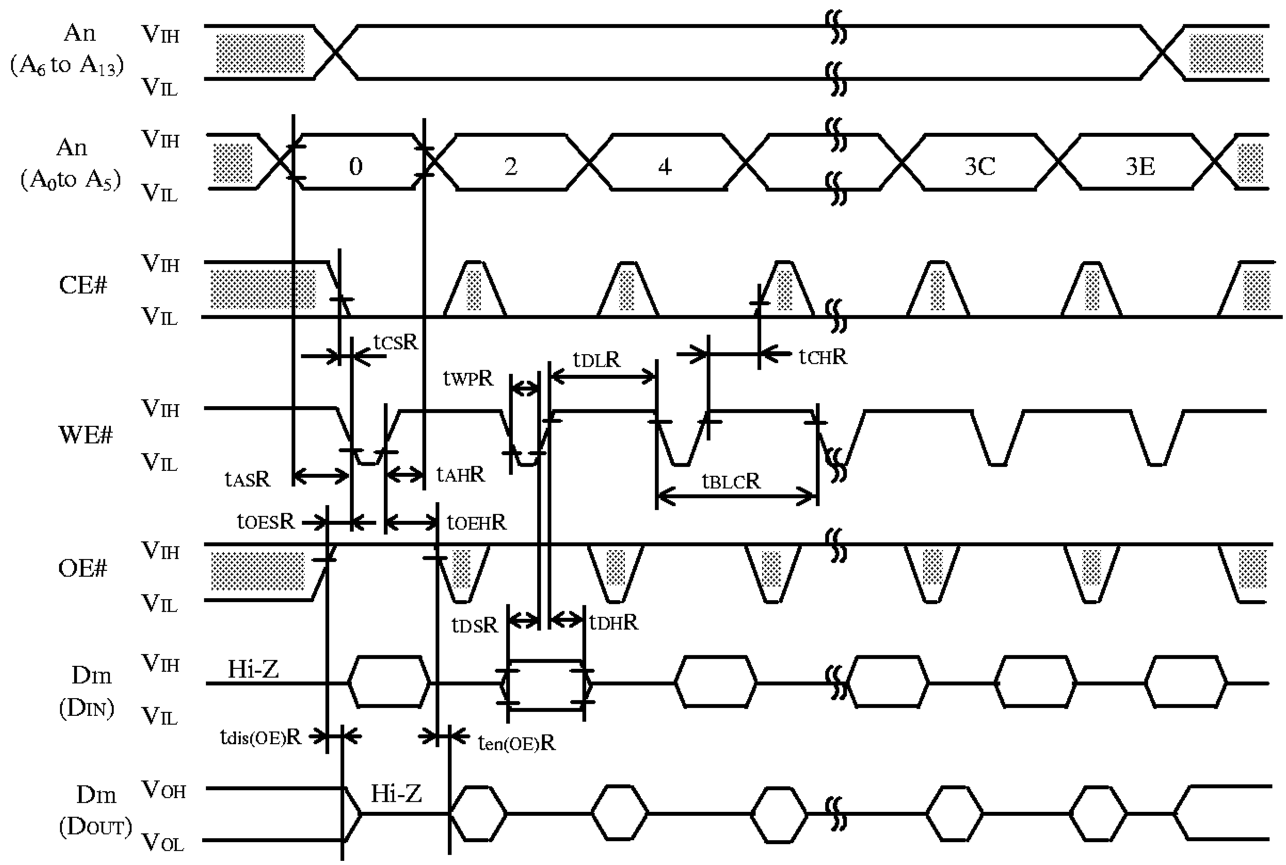
WE# ="H" level, REG# ="L" level

Byte Write



REG# ="L" level

Page Mode Write



REG#="L" level

Note 15 : AC Test Conditions

Input pulse levels : V_{IL}=0.4V, V_{IH}=2.8V

Input pulse rise, fall time : t_r=t_f=10ns

Reference voltage

Input : V_{IL}=0.8V, V_{IH}=2.4V

Output : V_{OL}=0.8V, V_{OH}=2.0V

(t_{en} and t_{dis} are measured when output voltage is± 500mV from steady state.)

Load : 100pF+1 TTL gate

5pF+1 TTL gate (at t_{en} and t_{dis} measuring)

16 : The data write is performed during the interval when both CE# and WE# are "L" level.

17 : Do not apply inverted phase signal externally when Dm pin is in output mode.

18 : CE is indicated as follows:

Read A/Write A : CE#=CE1#=CE2#

Read B/Write B : CE#=CE1#, CE2#="H" level

Read C/Write C : CE#=CE2#, CE1#="H" level

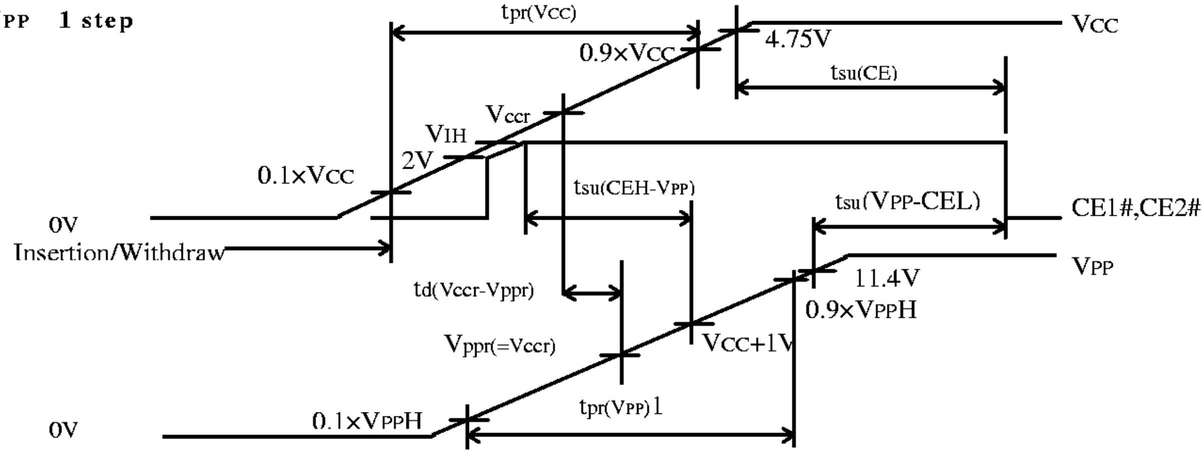
19: ▒ Indicates the don't care input.

RECOMMENDED POWER UP/DOWN CONDITIONS (Ta=0 to 55°C, unless otherwise noted)

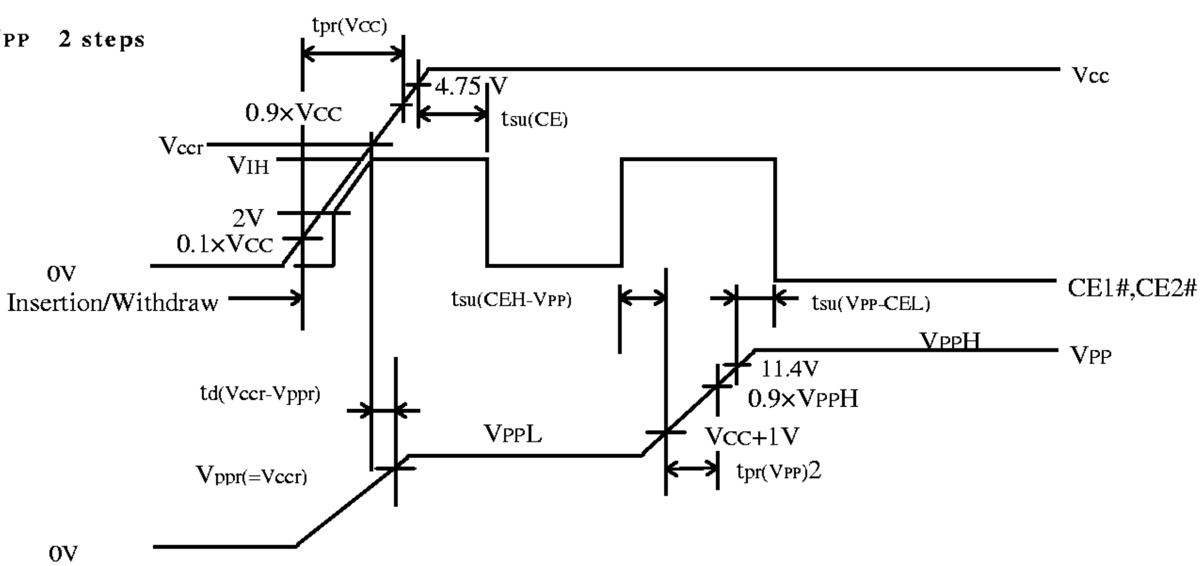
Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vi(CE)	CE input voltage	0V≤ Vcc <2V	0		Vcc	V
		2V≤ Vcc <2.4V	Vcc-0.1	Vcc	Vcc+0.1	V
		2.4V≤ Vcc	2.4		Vcc+0.1	V
t_{su}(CE)	CE# setup time		1			ms
t_{rec}(CE)	CE# recovery time		1			µs
t_{pr}(VCC)	Vcc rise time		0.1		300	ms
t_{pf}(VCC)	Vcc fall time		3		300	ms
t_{su}(CEH-VPP)	Setup time before Vpp rise		0.15			µs
t_{su}(VPP-CEL)	Setup time after Vpp rise		1			µs
t_{rec}(CEH-VPP)	Recovery time before Vpp fall		0.15			µs
t_{rec}(VPP-CEL)	Recovery time after Vpp fall		1			µs
t_{pr}(VPP)1	Vpp rise time 1		0.24		300	ms
t_{pf}(VPP)1	Vpp fall time 1		7.2		300	ms
t_{pr}(VPP)2	Vpp rise time 2		0.1		300	ms
t_{pf}(VPP)2	Vpp fall time 2		3		300	ms
t_d(VCCr-VPPr)	Vppr delay time after Vccr	0V≤Vcc≤4.75V	0			µs
t_d(VPPf-VCCf)	Vccf delay time after Vppf	0V≤Vcc≤4.75V	0			µs

POWER UP TIMING DIAGRAM

VPP 1 step



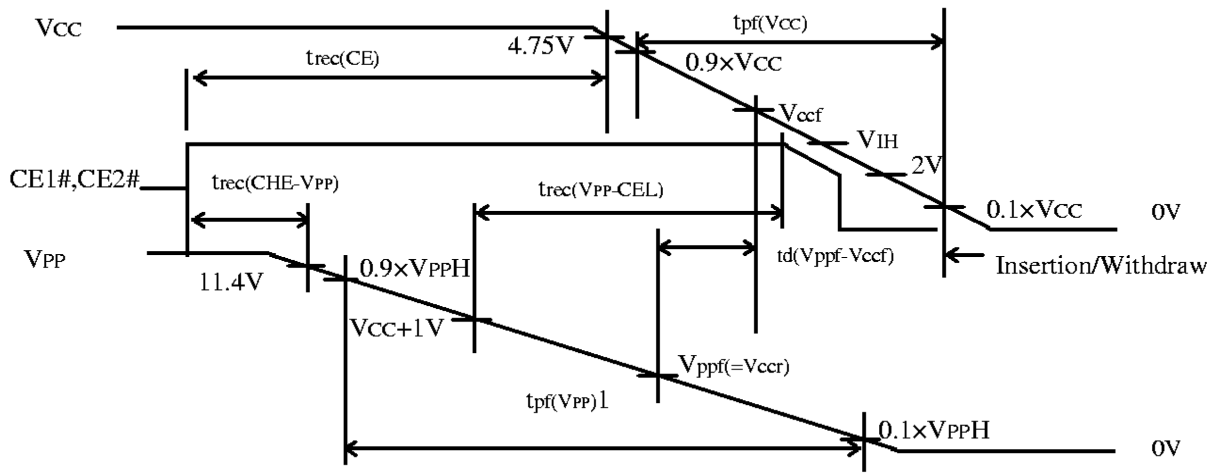
VPP 2 steps



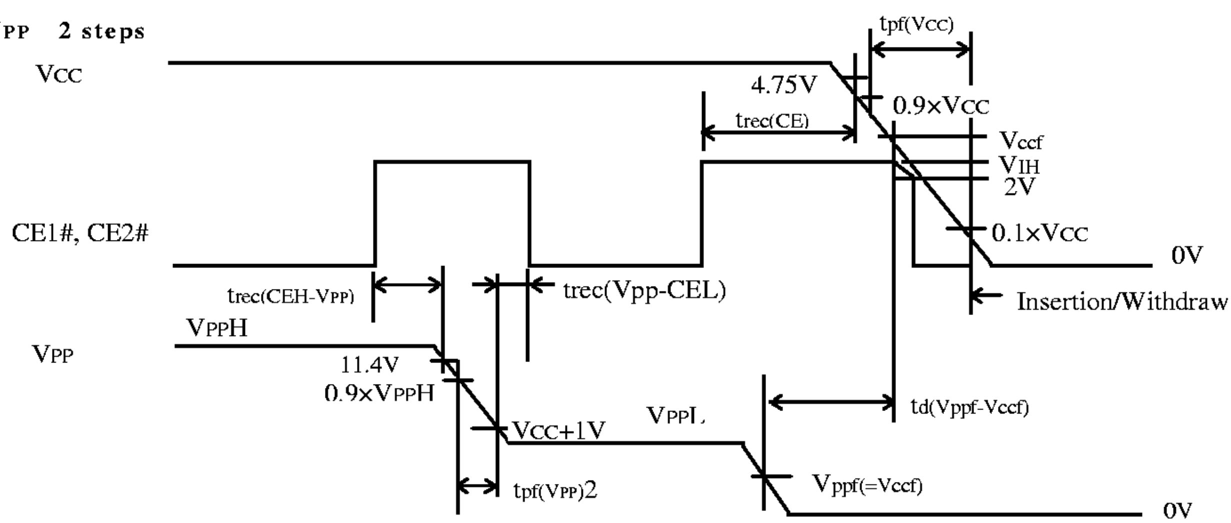
Note 20 : Vccr and Vppr(=Vccr) indicates any voltage when Vcc voltage is in the range of 0V to 4.75V
REG#="H"level

POWER DOWN TIMING DIAGRAM

VPP 1 step



VPP 2 steps



Note 21 : V_{ccr} and V_{ppr}(=V_{ccr}) indicates any voltage when VCC voltage is in the range of 0 V to 4.75V
REG#="H"level

BLOCK PROGRAM/ERASE TIME

Parameters	Limits		Unit
	Typ.	Max.	
Block erase time	1.6	10	s
Block proram time	0.6	2.1	s

Note 22 : At Ta=25°C, V_{pp}=12V
23 : Byte/word program time is about 9μs (typical), but not guaranteed.