4.5Mb LATE WRITE SRAM

MT59L256V18P
MT59L128V36P

NEW LATE WRITE SRAM

FEATURES

- Fast cycle times (4.5ns, 5ns, 6ns and 7ns)
- 256K x 18 or 128K x 36 configurations
- Single +3.3V +0.3V/-0.2V power supply (V_{DD})
- Separate isolated output buffer supply ($V_{DD}Q$)
- JEDEC-standard 2.5V I/O
- PECL differential input clock (2.5V I/O-compatible)
- JTAG boundary scan
- Asynchronous output enable
- Fully static design for reduced-power standby and clock-stop capability
- BYTE WRITE capability and synchronous WRITE
- SNOOZE MODE for reduced-power standby
- Clock-controlled and registered addresses, data I/Os and control signals
- Self-timed LATE WRITE
- 119-bump, 1.27mm (50 mil) pitch, 7 x 17 ball grid array (BGA) package
- JEDEC-standard pinout
- Low capacitive bus loading

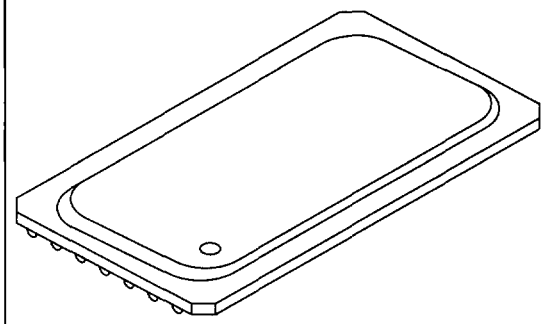
OPTIONS / MARKING

- Clock Cycle Timing
  - 4.5ns (222 MHz) -4.5
  - 5ns (200 MHz) -5
  - 6ns (167 MHz) -6
  - 7ns (143 MHz) -7
- Configurations
  - 256K x 18 MT59L256V18P
  - 128K x 36 MT59L128V36P
- Package
  - 119-bump, 14mm x 22mm BGA B

VALID PART NUMBERS

PART NUMBER	DESCRIPTION
MT59L256V18PB-xx	256K x 18, 2.5V I/O, Pipelined
MT59L128V36PB-xx	128K x 36, 2.5V I/O, Pipelined

119-Bump BGA
(SB-1)



GENERAL DESCRIPTION

The Micron Late Write SRAM family employs high-speed, low-power CMOS designs using an advanced CMOS process.

The MT59L256V18P and MT59L128V36P SRAMs integrate a 256K x 18 or 128K x 36 SRAM core with advanced synchronous peripheral circuitry. All synchronous inputs pass through registers controlled by a differential input clock (CK and CK#) and are latched on the rising edge of CK and the falling edge of CK#. CK and CK# are PECL clock inputs (2.5V I/O-compatible). Synchronous inputs include all addresses, all data inputs, synchronous write (SW#), byte write enables (BWa#, BWb#, BWc# and BWd#) and synchronous select (SS#). Asynchronous inputs are output enable (OE#) and snooze enable (ZZ).

Address and write control are registered on-chip to simplify WRITE cycles. Individual byte enables allow individual bytes to be written. During WRITE cycles on the x36 version, BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins. During WRITE cycles on the x18 version, BWa# controls DQa pins, and BWb# controls DQb pins.

Four pins are used to implement JTAG test capabilities: test mode select (TMS), test data-in (TDI), test clock (TCK) and test data-out (TDO). JTAG circuitry is used to serially shift data to and from the SRAM. JTAG inputs use LVTTL/LVCMOS levels to shift data during this testing mode of operation.

The MT59L256V18P and MT59L128V36P operate from a +3.3V power supply, and all inputs and outputs are 2.5V I/O-compatible. The device is ideally suited for cache, ATM, telecom and other applications that benefit from a very wide, high-speed data bus. The device is also ideal in generic 18-, 36- and 72-bit-wide applications.

NEW LATE WRITE SRAM

GENERAL DESCRIPTION (continued)

Please refer to the Micron Web site (www.micron.com./mti/msp/html/sramprod.html) for the latest data sheet revisions.

LATE WRITE

The pipelined Late Write SRAM allows for high performance with only a single bus turnaround or dead cycle when switching from READ to WRITE. This eliminates an extra dead cycle that was present in the pipelined SyncBurst family during the same operation through the use of an extra address register. A WRITE is performed by registering the write address on a rising CK edge (and falling edge of CK#) and then registering the write data on the next rising CK edge. A DESELECT cycle (SS# = HIGH, see Truth Table) or an "ABORTED" READ cycle must occur when transitioning from a READ cycle to a WRITE cycle. An ABORTED READ cycle is a regular READ cycle whose data is never read out of the SRAM because the WRITE that occurs in the next cycle turns off the output drivers. No DESELECT cycle is necessary when transitioning from WRITE to READ.

If a READ occurs after a WRITE cycle, the address and data for the WRITE are stored in registers. The write information must be stored because the SRAM cannot perform the last WORD WRITE to the array without conflicting with the READ. The data stays in this register until the next WRITE cycle occurs. On the first WRITE cycle after the READ(s), the stored data from the earlier WRITE will be written into the SRAM array. This is called a POSTED WRITE.

A READ can be made immediately to an address even if that address was written in the previous cycle. During this READ cycle, the SRAM array is bypassed, and data is read from the data register storing the recently written data. This is transparent to the user.

For lowest power operating mode, the differential input clock may be stopped. This prevents the internal circuitry from cycling and results in minimal power dissipation.

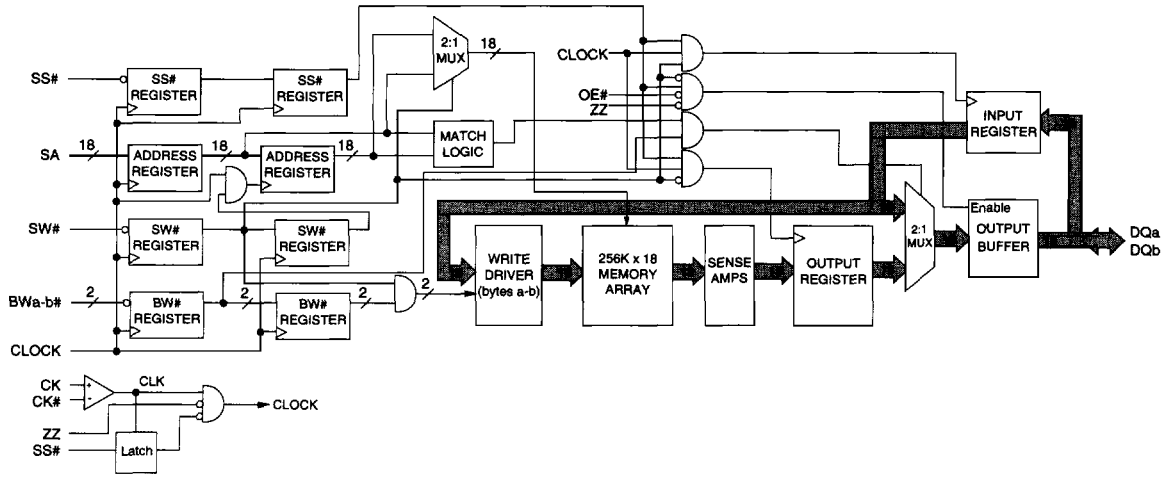
BYTE WRITES

The Late Write SRAM is able to perform BYTE WRITEs using the byte write signals along with the SW# control. These BWx# signals are "Don't Care" during READ cycles. If BYTE WRITEs are not required, these signals can be wired LOW (Vss), and WRITEs can be exclusively controlled through the SW# pin. Only word-wide WRITEs are possible using this method.

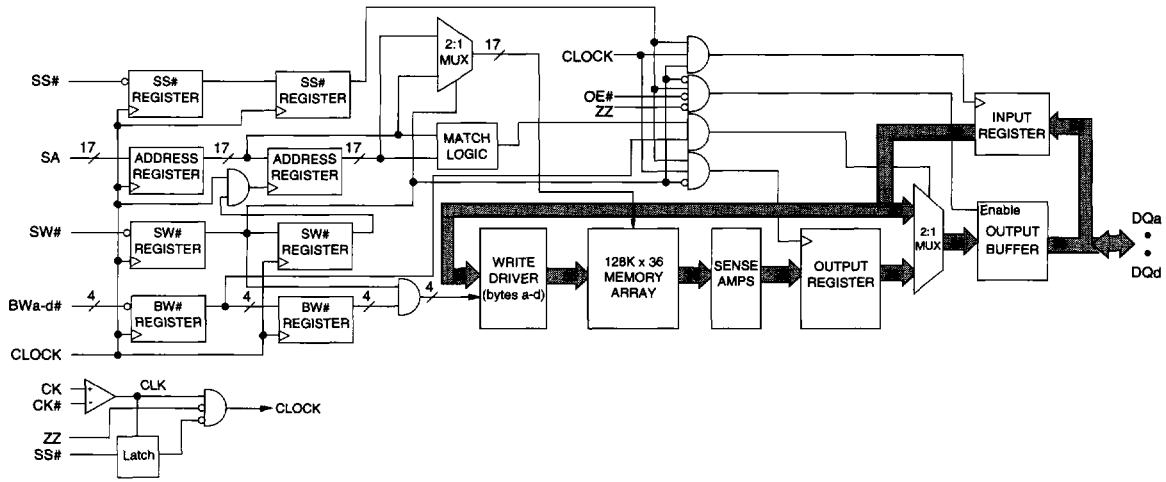
During a BYTE WRITE command, one or more BWx# pins are LOW. This means that one or more bytes are written. The other bytes (with the corresponding BWx# HIGH) are not written or read during a BYTE WRITE cycle. Only a WRITE or READ can be performed within a cycle, not both.

NEW LATE WRITE SRAM

FUNCTIONAL BLOCK DIAGRAM
256K x 18



FUNCTIONAL BLOCK DIAGRAM
128K x 36



NOTE: Functional Block Diagrams illustrate simplified device operation. See Truth Table, Pin Descriptions and timing diagrams for detailed information.

NEW LATE WRITE SRAM

x18 BGA BUMP LAYOUT
(Top View)

	1	2	3	4	5	6	7
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC[2]	SA	NC	SA	NC[1]	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	DQb	NC	Vss	NC	Vss	DQa	NC
E	NC	DQb	Vss	SS#	Vss	NC	DQa
F	VDDQ	NC	Vss	OE#	Vss	DQa	VDDQ
G	NC	DQb	BWb#	NC	Vss	NC	DQa
H	DQb	NC	Vss	NC	Vss	DQa	NC
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	NC	DQb	Vss	CK	Vss	NC	DQa
L	DQb	NC	Vss	CK#	BWa#	DQa	NC
M	VDDQ	DQb	Vss	SW#	Vss	NC	VDDQ
N	DQb	NC	Vss	SA	Vss	DQa	NC
P	NC	DQb	Vss	SA	Vss	NC	DQa
R	NC	SA	Vss	VDD	VDD	SA	NC
T	NC	SA	SA	NC	SA	SA	ZZ
U	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ

x18 BGA BUMP LAYOUT
(Bottom View)

	7	6	5	4	3	2	1
A	VDDQ	SA	SA	NC	SA	SA	VDDQ
B	NC	NC[1]	SA	NC	SA	NC[2]	NC
C	NC	SA	SA	VDD	SA	SA	NC
D	NC	DQa	Vss	NC	Vss	NC	DQb
E	Da	NC	Vss	SS#	Vss	DQb	NC
F	VDDQ	DQa	Vss	OE#	Vss	NC	VDDQ
G	DQa	NC	Vss	NC	BWb#	DQb	NC
H	NC	DQa	Vss	NC	Vss	NC	DQb
J	VDDQ	VDD	NC	VDD	NC	VDD	VDDQ
K	DQa	NC	Vss	CK	Vss	DQb	NC
L	NC	DQa	BWa#	CK#	Vss	NC	DQb
M	VDDQ	NC	Vss	SW#	Vss	DQb	VDDQ
N	NC	DQa	Vss	SA	Vss	NC	DQb
P	DQa	NC	Vss	SA	Vss	DQb	NC
R	NC	SA	VDD	VDD	Vss	SA	NC
T	ZZ	SA	SA	NC	SA	SA	NC
U	VDDQ	NC	TDO	TCK	TDI	TMS	VDDQ

NOTE: 1. Bump 6B is reserved as an address bit for the 9Mb Late Write SRAM.
2. Bump 2B is reserved as an address bit for the 18Mb Late Write SRAM.

x36 BGA BUMP LAYOUT
(Top View)

	1	2	3	4	5	6	7
A	$V_{DD}Q$	SA	SA	NC	SA	SA	$V_{DD}Q$
B	NC	NC[2]	SA	NC	SA	NC[1]	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQc	DQc	Vss	NC	Vss	DQb	DQb
E	DQc	DQc	Vss	SS#	Vss	DQb	DQb
F	$V_{DD}Q$	DQc	Vss	OE#	Vss	DQb	$V_{DD}Q$
G	DQc	DQc	BWc#	NC	BWb#	DQb	DQb
H	DQc	DQc	Vss	NC	Vss	DQb	DQb
J	$V_{DD}Q$	V_{DD}	NC	V_{DD}	NC	V_{DD}	$V_{DD}Q$
K	DQd	DQd	Vss	CK	Vss	DQa	DQa
L	DQd	DQd	BWd#	CK#	BWa#	DQa	DQa
M	$V_{DD}Q$	DQd	Vss	SW#	Vss	DQa	$V_{DD}Q$
N	DQd	DQd	Vss	SA	Vss	DQa	DQa
P	DQd	DQd	Vss	SA	Vss	DQa	DQa
R	NC	SA	Vss	V_{DD}	V_{DD}	SA	NC
T	NC	NC	SA	SA	SA	NC	ZZ
U	$V_{DD}Q$	TMS	TDI	TCK	TDO	NC	$V_{DD}Q$

x36 BGA BUMP LAYOUT
(Bottom View)

	7	6	5	4	3	2	1
A	$V_{DD}Q$	SA	SA	NC	SA	SA	$V_{DD}Q$
B	NC	NC[1]	SA	NC	SA	NC[2]	NC
C	NC	SA	SA	V_{DD}	SA	SA	NC
D	DQb	DQb	Vss	NC	Vss	DQc	DQc
E	DQb	DQb	Vss	SS#	Vss	DQc	DQc
F	$V_{DD}Q$	DQb	Vss	OE#	Vss	DQc	$V_{DD}Q$
G	DQb	DQb	BWb#	NC	BWc#	DQc	DQc
H	DQb	DQb	Vss	NC	Vss	DQc	DQc
J	$V_{DD}Q$	V_{DD}	NC	V_{DD}	NC	V_{DD}	$V_{DD}Q$
K	DQa	DQa	Vss	CK	Vss	DQd	DQd
L	DQa	DQa	BWa#	CK#	BWd#	DQd	DQd
M	$V_{DD}Q$	DQa	Vss	SW#	Vss	DQd	$V_{DD}Q$
N	DQa	DQa	Vss	SA	Vss	DQd	DQd
P	DQa	DQa	Vss	SA	Vss	DQd	DQd
R	NC	SA	V_{DD}	V_{DD}	Vss	SA	NC
T	ZZ	NC	SA	SA	SA	NC	NC
U	$V_{DD}Q$	NC	TDO	TCK	TDI	TMS	$V_{DD}Q$

NOTE: 1. Bump 6B is reserved as an address bit for the 9Mb Late Write SRAM.
2. Bump 2B is reserved as an address bit for the 18Mb Late Write SRAM.

NEW LATE WRITE SRAM

PIN DESCRIPTIONS

BGA BUMPS (x18)	BGA BUMPS (x36)	SYMBOL	TYPE	DESCRIPTION
2A, 2C, 2R, 2T, 3A, 3B, 3C, 3T, 4N, 4P, 5A, 5B, 5C, 5T, 6A, 6C, 6R, 6T	2A, 2C, 2R, 3A, 3B, 3C, 3T, 4N, 4P, 4T, 5A, 5B, 5C, 5T, 6A, 6C, 6R	SA	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of CK. Bump 6B (no connect) is reserved as an address bit for a 9Mb Late Write SRAM, and bump 2B is reserved as an address bit for an 18Mb Late Write SRAM.
4M	4M	SW#	Input	Synchronous Write: This active LOW input enables BYTE WRITE operations and must meet setup and hold times around the rising edge of CK. If SW# is active (LOW), any byte write enables (BWx#) that are LOW will write to the corresponding byte. When SW# is LOW, data I/Os are placed in High-Z. SW# must be inactive (HIGH) for READ operations.
5L 3G – –	5L 5G 3G 3L	BWa# BWb# BWc# BWd#	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written and must meet the setup and hold times around the rising edge of CK. A byte write enable is LOW for a WRITE cycle and "Don't Care" for a READ cycle. BWa# controls DQa pins; BWb# controls DQb pins; BWc# controls DQc pins; and BWd# controls DQd pins.
4K 4L	4K 4L	CK CK#	Input	PECL Differential Clock: This differential input clock registers data, address and control inputs on the rising edge of CK (falling edge of CK#). All synchronous inputs must meet setup and hold times around the rising edge of CK. Input data is registered at the rising edge of CK during a WRITE cycle. These inputs are PECL logic levels (2.5V I/O-compatible).
4F	4F	OE# (G#)	Input	Output Enable: This active LOW, asynchronous input enables the data I/O output drivers. G# is the JEDEC-standard term for OE#.
(a) 6D, 6F, 6H, 6L, 6N, 7E, 7G, 7K, 7P (b) 1D, 1H, 1L, 1N, 2E, 2G, 2K, 2M, 2P	(a) 6K, 6L, 6M, 6N, 6P, 7K, 7L, 7N, 7P (b) 6D, 6E, 6F, 6G, 6H, 7D, 7E, 7G, 7H (c) 1D, 1E, 1G, 1H, 2D, 2E, 2F, 2G, 2H (d) 1K, 1L, 1N, 1P, 2K, 2L, 2M, 2N, 2P	DQa DQb DQc DQd	I/O	Synchronous Data I/Os: Byte "a" is DQa; Byte "b" is DQb; Byte "c" is DQc; Byte "d" is DQd. Input data must meet setup and hold times around the rising edge of CK (falling edge of CK#) during WRITE cycles.
4E	4E	SS#	Input	Synchronous Select: This active LOW, synchronous chip select input enables the SRAM for READ or WRITE operations. SS# must meet setup and hold times around the rising edge of CK.

PIN DESCRIPTIONS (continued)

BGA BUMPS (x18)	BGA BUMPS (x36)	SYMBOL	TYPE	DESCRIPTION
7T	7T	ZZ	Input	Snooze Mode: This active HIGH, asynchronous input causes the device to enter a low-power standby mode in which all data in the memory array is retained. When ZZ is active, all other inputs are ignored and outputs go to High-Z. The SNOOZE MODE must not be initiated until all valid pending operations are completed.
2U 3U 4U	2U 3U 4U	TMS TDI TCK	Input	IEEE 1149.1 test inputs. LVTTL-level inputs.
5U	5U	TDO	Output	IEEE 1149.1 test output. LVTTL-level output.
1B, 1C, 1E, 1G, 1K, 1P, 1R, 1T, 2B, 2D, 2F, 2H, 2L, 2N, 3J, 4A, 4B, 4D, 4G, 4H, 4T, 5J, 6B, 6E, 6G, 6K, 6M, 6P, 6U, 7B, 7C, 7D, 7H, 7L, 7N, 7R	1B, 1C, 1R, 1T, 2B, 2T, 3J, 4A, 4B, 4D, 4G, 4H, 5J, 6B, 6T, 6U, 7B, 7C, 7R	NC	–	No Connect: These signals are not internally connected and may be connected to ground to improve package heat dissipation. For upgrade to higher-density Late Write SRAMs, bump 6B is reserved as an address bit for the 9Mb and bump 2B for the 18Mb.
2J, 4C, 4J, 4R, 5R, 6J	2J, 4C, 4J, 4R, 5R, 6J	V_{DD}	Supply	Power Supply: See DC Electrical Characteristics and Operating Conditions for range.
1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	1A, 1F, 1J, 1M, 1U, 7A, 7F, 7J, 7M, 7U	V_{DDQ}	Supply	Power Supply: Isolated Output Buffer Supply. See DC Electrical Characteristics and Operating Conditions for range.
3D, 3E, 3F, 3H, 3K, 3L, 3M, 3N, 3P, 3R, 5D, 5E, 5F, 5G, 5H, 5K, 5M, 5N, 5P	3D, 3E, 3F, 3H, 3K, 3M, 3N, 3P, 3R, 5D, 5E, 5F, 5H, 5K, 5M, 5N, 5P	V_{SS}	Supply	Power Supply: GND.

TRUTH TABLE

OPERATION	ADDRESS	ZZ	SS#	SW#	BWa#	BWb#	BWc#	BWd#	DQ(t)	DQ(t + 1)	CLK	NOTES
READ CYCLE	A1	L	L	H	X	X	X	X	X	DOUT (A1)	L → H	1
READ CYCLE	A1	L	L	H	X	X	X	X	X	High-Z	L → H	2
WRITE CYCLE, BYTE A	A1	L	L	L	L	H	H	H	High-Z	DIN (A1)	L → H	3
WRITE CYCLE, BYTE B	A1	L	L	L	H	L	H	H	High-Z	DIN (A1)	L → H	3
WRITE CYCLE, BYTE C	A1	L	L	L	H	H	L	H	High-Z	DIN (A1)	L → H	3
WRITE CYCLE, BYTE D	A1	L	L	L	H	H	H	L	High-Z	DIN (A1)	L → H	3
WRITE CYCLE, ALL BYTES	A1	L	L	L	L	L	L	L	High-Z	DIN (A1)	L → H	
WRITE ABORT	X	L	L	L	H	H	H	H	High-Z	High-Z	L → H	
DESELECT CYCLE	X	L	H	X	X	X	X	X	X	High-Z	L → H	
SNOOZE MODE	X	H	X	X	X	X	X	X	High-Z	High-Z	X	

NOTE: 1. OE# LOW.
2. OE# HIGH.
3. For WRITE cycle: For Byte "a," only DQa pins are written; for Byte "b," only DQb pins are written; for Byte "c," only DQc pins are written; for Byte "d," only DQd pins are written. Bytes "c" and "d" are only available on the x36 version.

OUTPUT ENABLE TRUTH TABLE

OPERATION	OE# (G#)	DQ
READ	L	DOUT (A)
READ	H	High-Z
Sleep (ZZ = HIGH)	X	High-Z
WRITE (SW# = LOW)	X	High-Z
DESELECT (SS# = HIGH)	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD} Supply Relative to V_{SS} ..... -0.5V to +4.6V
Voltage on V_{DDQ} Supply Relative to V_{SS} ..... -0.5V to V_{DD}
V_{IN} ..... -0.5V to V_{DD} + 0.5V
Storage Temperature ..... -55°C to +125°C
Junction Temperature** ..... +125°C
Short Circuit Output Current 100mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See Micron Technical Note TN-05-14 for more information.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(20°C ≤ T_J ≤ 110°C; +3.1V ≤ V_{DD} ≤ +3.6V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	1.7	V_{DD} + 0.3	V	1, 2
	PECL clock inputs	V_{IHP}	2.135	2.420	V	1, 2, 3
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.7	V	1, 2
	PECL clock inputs	V_{ILP}	1.490	1.825	V	1, 2, 3
Clock Input Signal Voltage		V_{IN}	-0.3	V_{DDQ} + 0.3	V	1
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-1.0	1.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ V_{DDQ} (DQx)	I_{LO}	-1.0	1.0	µA	
Output High Voltage	I_{OH} ≤ 8mA	V_{OH}	1.7	-	V	1, 4
Output Low Voltage	I_{OL} ≤ 8mA	V_{OL}	-	0.7	V	1, 4
Supply Voltage		V_{DD}	3.1	3.6	V	1
Isolated Output Buffer Supply		V_{DDQ}	2.3	2.7	V	1
Differential Clock Input Signal		V_{DIFF}	0.2	V_{DDQ} + 0.6	V	1
Differential Clock Common Mode Voltage		V_{CM}	1.1	2.1	V	1

NOTE:
1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} (AC) ≤ V_{DD} + 1.5V for t ≤ $^tKHKH/2$
   Undershoot: V_{IL} (AC) -0.5V for t ≤ $^tKHKH/2$
   Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V and V_{DDQ} ≤ V_{DD} for t ≤ 200ms
   During normal operation, V_{DDQ} must not exceed V_{DD}. Control input signals (such as SS#, SW#, etc.) may not have pulse widths less than ^tKHKL (MIN) or operate at frequencies exceeding ^fKF (MAX).
3. PECL clock inputs are also 2.5V I/O-compatible.
4. AC load current is higher than the shown DC values. AC I/O curves are available upon request.

NEW LATE WRITE SRAM

I_{DD} OPERATING CONDITIONS AND MAXIMUM LIMITS

(20°C ≤ T_J ≤ 110°C; V_{DD} = MAX)

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	TYP	-4.5	-5	-6	-7	UNITS	NOTES
Power Supply Current: Operating (x36)	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKHKH (MIN); SS# is registered active; Outputs open	I_{DD}	TBD	525	500	440	390	mA	1, 2, 3, 4
Power Supply Current: Operating (x18)	Device selected; All inputs ≤ V_{IL} or ≥ V_{IH}; Cycle time ≥ ^tKHKH (MIN); SS# is registered active; Outputs open	I_{DD}	TBD	475	450	400	360	mA	1, 2, 3, 4
Active Standby	Device selected; All inputs ≤ V_{SS} + 0.2 or ≥ V_{DD} - 0.2; SS# is registered active; Outputs open; All inputs static; CLK frequency = 0	I_{DD1}	TBD	170	170	170	170	mA	2, 3, 4
Standby: Clock Active	Device deselected; All inputs ≤ V_{IL} or ≥ V_{IH}; SS# is registered inactive; All inputs static; CLK frequency = MAX	I_{SB1}	TBD	105	105	105	105	mA	2, 3
Standby: Clock Static	Device deselected; All inputs ≤ V_{IL} or ≥ V_{IH}; SS# is registered inactive; All inputs static; CLK frequency = 0	I_{SB2}	TBD	105	105	105	105	mA	2, 3
Standby: Z	ZZ ≥ V_{IH}	I_{SB2Z}	TBD	25	25	25	25	mA	3

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Address/Control Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	4	5	pF	5
Input/Output Capacitance (DQ)		C_O	6	7	pF	5
Clock Capacitance		C_{CK}	5	6	pF	5

THERMAL RESISTANCE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	UNITS	NOTES
Junction to Ambient (Airflow of 1m/s)	Soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board	θ_{JA}	25	°C/W	5
Junction to Case (Top)		θ_{JC}	10	°C/W	5
Junction to Bumps (Bottom)		θ_{JB}	12	°C/W	5

NOTE:
1. I_{DD} is specified with no output current and increases with faster cycle times. I_{DDQ} increases with faster cycle times and greater output loading.
2. "Device deselected" means device is in deselect mode as defined in the truth table. "Device selected" means device is active (not in deselect mode).
3. Typical values are measured at V_{DD} = 3.3V, 25°C and 7ns cycle time.
4. I_{DDS} are calculated with 50 percent READ cycles and 50 percent WRITE cycles.
5. This parameter is sampled.

AC ELECTRICAL CHARACTERISTICS

(Note 4) (20°C ≤ T_J ≤ 110°C; +3.1V ≤ V_{DD} ≤ +3.6V)

DESCRIPTION	SYMBOL	-4.5		-5		-6		-7		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock											
Clock cycle time	^tKHKH	4.5		5.0		6.0		7.0		ns	
Clock frequency	^fKF		222		200		166		143	MHz	
Clock HIGH time	^tKHKL	1.8		2.0		2.4		2.8		ns	
Clock LOW time	^tKLKH	1.8		2.0		2.4		2.8		ns	
Output Times											
Clock to output in Low-Z	$^tKHQX1$	0.5		1.0		1.0		1.0		ns	1
Clock to output valid	^tKHQV		2.25		2.5		3.0		3.5	ns	
Clock to output invalid	^tKHQX	0.5		1.0		1.0		1.0		ns	
Clock to output in High-Z	^tKHQZ		2.5		2.5		3.0		3.25	ns	1
OE# to output in Low-Z	^tGLQX	0.5		0.5		0.5		0.5		ns	
OE# to output valid	^tGLQV		2.5		2.5		3.0		3.5	ns	2
OE# to output invalid	^tGHQX	0.5		0.5		0.5		0.5		ns	1
OE# to output in High-Z	^tGHQZ		2.5		2.5		3.0		3.5	ns	1
Setup Times											
Address	^tAVKH	0.5		0.5		0.5		0.5		ns	3
Data-in	^tDVKH	0.5		0.5		0.5		0.5		ns	3
Synchronous select (SS#)	^tSVKH	0.5		0.5		0.5		0.5		ns	3
Write enable	^tWVKH	0.5		0.5		0.5		0.5		ns	3
Hold Times											
Address	^tKHAX	0.9		1.0		1.0		1.0		ns	3
Data-in	^tKHDX	0.9		1.0		1.0		1.0		ns	3
Synchronous select (SS#)	^tKHSX	1.0		1.0		1.0		1.0		ns	3
Write enable	^tKHWX	1.0		1.0		1.0		1.0		ns	3

NOTE:
1. Output loading is specified with Figure 2. Transition is measured ±200mV from steady state voltage.
2. OE# is a "Don't Care" when SW# is LOW.
3. This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CK when SS# is enabled. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of clock (CK) when the chip is enabled. Synchronous select (SS#) must be valid at each rising edge of CK to remain enabled.
4. Test conditions as specified with the output loading as shown in Figure 1 unless otherwise noted.

AC TEST CONDITIONS

Input pulse levels	0.25V to 2.25V
2.5V input rise and fall times	1ns
PECL clock rise and fall times	0.5ns
Input timing reference levels	0.75V
Output reference levels	0.75V
PECL clock input high voltage	2.4V
PECL clock input low voltage	1.5V
Clock input timing reference level	Differential Cross Point
Output load	See Figures 1 and 2

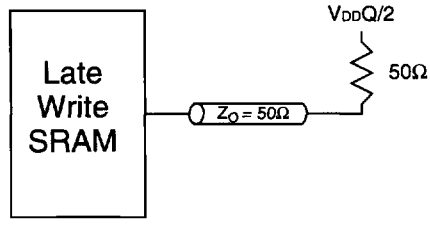


Figure 1
OUTPUT LOAD EQUIVALENT

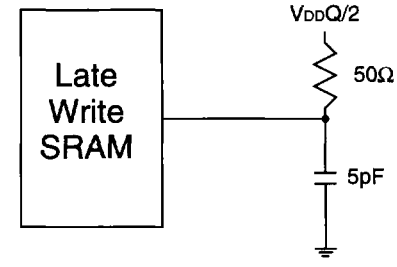


Figure 2
OUTPUT LOAD EQUIVALENT

SNOOZE MODE

SNOOZE MODE is a low-current, "power-down" mode in which the device is deselected and current is reduced to I_{SB2Z}. The duration of SNOOZE MODE is dictated by the length of time the ZZ bump is in a HIGH state. After the device enters SNOOZE MODE, all inputs except ZZ become gated inputs and are ignored, and all outputs go to High-Z.

The ZZ pin (bump 7T) is an asynchronous, active HIGH input that causes the device to enter SNOOZE MODE. When the ZZ pin becomes a logic HIGH, I_{SB2Z} is guaranteed after the time ^tZZI is met. Any READ or WRITE operation pending when the device enters SNOOZE MODE is not guaranteed to complete successfully. Therefore, SNOOZE MODE must not be initiated until valid pending operations are completed. Similarly, when exiting SNOOZE MODE during ^tRZZ, only a DESELECT or READ cycle should be given.

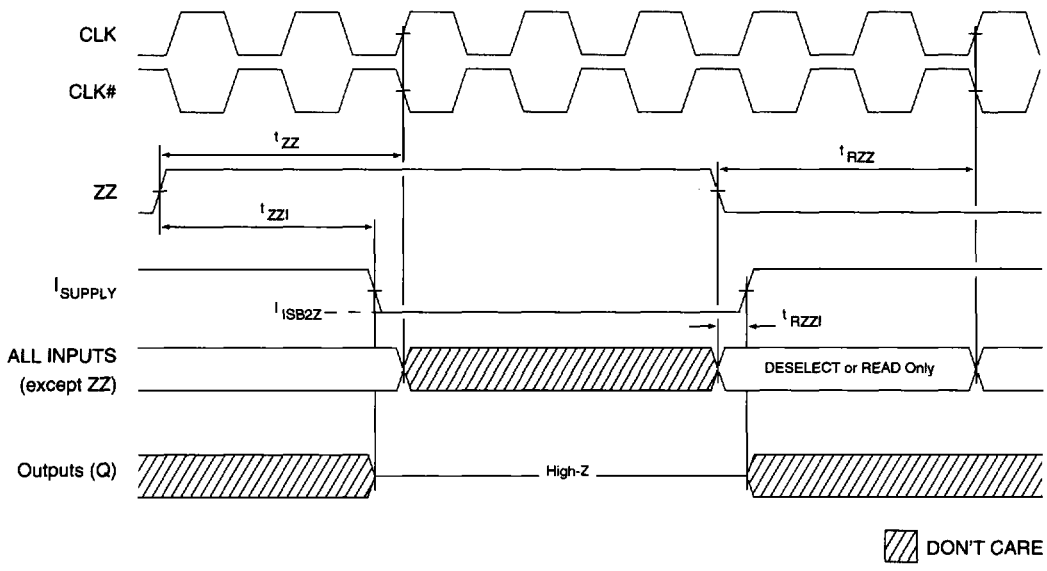
SNOOZE MODE ELECTRICAL CHARACTERISTICS

($20°C \le T_J \le 110°C$; $+3.1V \le V_{DD} \le +3.6V$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Current during SNOOZE MODE	ZZ ≥ V_{IH}	I_{SB2Z}		25	mA	
ZZ active to input ignored		^tZZ		2(^tKHKH)	ns	1
ZZ inactive to input sampled		^tRZZ	2(^tKHKH)		ns	1
ZZ active to snooze current		^tZZI		2(^tKHKH)	ns	1
ZZ inactive to exit snooze current		^tRZZI	0		ns	1

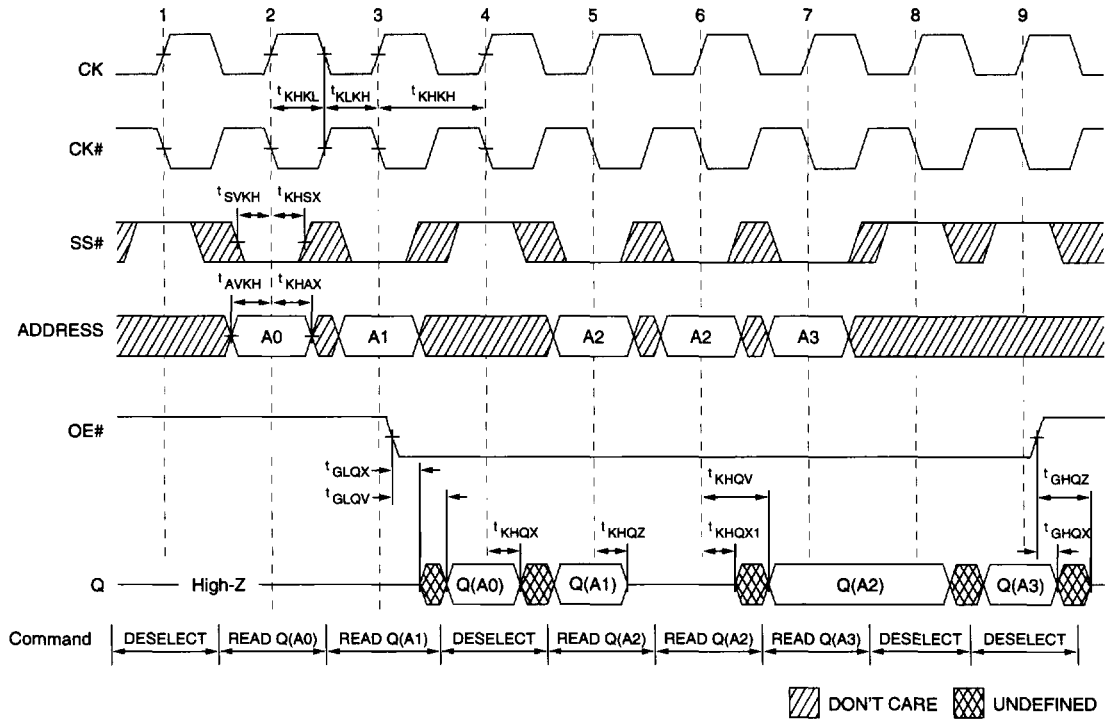
NOTE: 1. This parameter is sampled.

SNOOZE MODE WAVEFORM



NEW LATE WRITE SRAM

READ TIMING



READ TIMING PARAMETERS

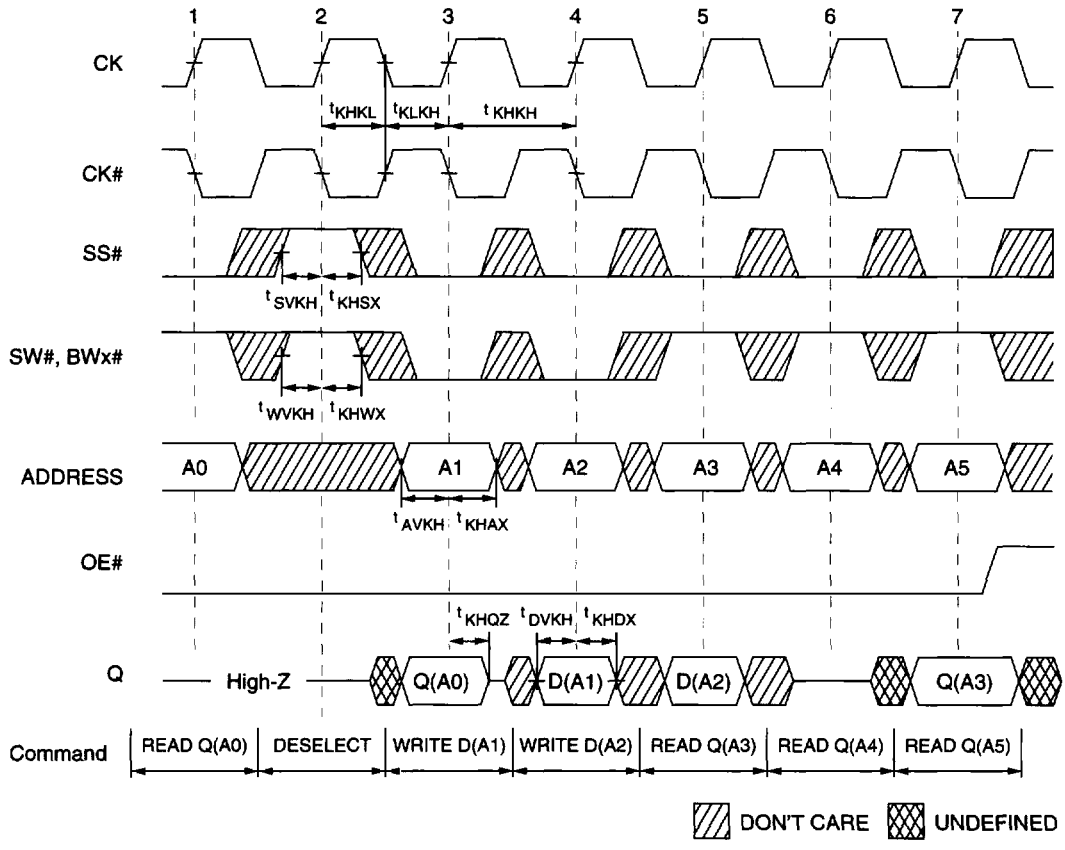
SYMBOL	-4.5 MIN	-4.5 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tKHKH	4.5		5.0		6.0		7.0		ns
tKF		222		200		166		143	MHz
tKHKL	1.8		2.0		2.4		2.8		ns
tKLKH	1.8		2.0		2.4		2.8		ns
tKHQX1	0.5		1.0		1.0		1.0		ns
tKHQV		2.25		2.5		3.0		3.5	ns
tKHQX	0.5		1.0		1.0		1.0		ns
tKHQZ		2.5		2.5		3.0		3.25	ns

SYMBOL	-4.5 MIN	-4.5 MAX	-5 MIN	-5 MAX	-6 MIN	-6 MAX	-7 MIN	-7 MAX	UNITS
tGLQX	0.5		0.5		0.5		0.5		ns
tGLQV		2.5		2.5		3.0		3.5	ns
tGHQX	0.5		0.5		0.5		0.5		ns
tGHQZ		2.5		2.5		3.0		3.5	ns
tAVKH	0.5		0.5		0.5		0.5		ns
tSVKH	0.5		0.5		0.5		0.5		ns
tKHAX	0.9		1.0		1.0		1.0		ns
tKHSX	1.0		1.0		1.0		1.0		ns

NOTE: SW# is inactive (HIGH).

NEW LATE WRITE SRAM

READ/WRITE TIMING



READ/WRITE TIMING PARAMETERS

	-4.5		-5		-6		-7		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tKHKH	4.5		5.0		6.0		7.0		ns
tKF		222		200		166		143	MHz
tKHKL	1.8		2.0		2.4		2.8		ns
tKLKH	1.8		2.0		2.4		2.8		ns
tKHQZ		2.5		2.5		3.0		3.25	ns
tAVKH	0.5		0.5		0.5		0.5		ns
tDVKH	0.5		0.5		0.5		0.5		ns

	-4.5		-5		-6		-7		
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tSVKH	0.5		0.5		0.5		0.5		ns
tWVKH	0.5		0.5		0.5		0.5		ns
tKHAX	0.9		1.0		1.0		1.0		ns
tKHDX	0.9		1.0		1.0		1.0		ns
tKHSX	1.0		1.0		1.0		1.0		ns
tKHWX	1.0		1.0		1.0		1.0		ns

NEW LATE WRITE SRAM

IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The Late Write SRAM incorporates a serial boundary scan test access port (TAP). This port operates in accordance with IEEE Standard 1149.1-1990 but does not have the set of functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because their inclusion places an added delay in the critical speed path of the SRAM. Note that the TAP controller functions in a manner that does not conflict with the operation of other devices using 1149.1 fully compliant TAPs. The TAP operates using LVTTL/LVCMOS logic level signaling.

The SRAM contains a TAP controller, instruction register, boundary scan register, bypass register and ID register. TRST#, an optional reset signal, is not required for JTAG because the TAP controller resets internally upon power-up.

DISABLING THE JTAG FEATURE

The SRAM can be operated without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (Vss) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternately be connected to VDD through a pull-up resistor. TDO should be left unconnected. Upon power-up, the device will come up in a reset state which will not interfere with the operation of the device.

TEST ACCESS PORT (TAP)

TEST CLOCK (TCK)

The TCK is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

TEST MODE SELECT (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. It is allowable to leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

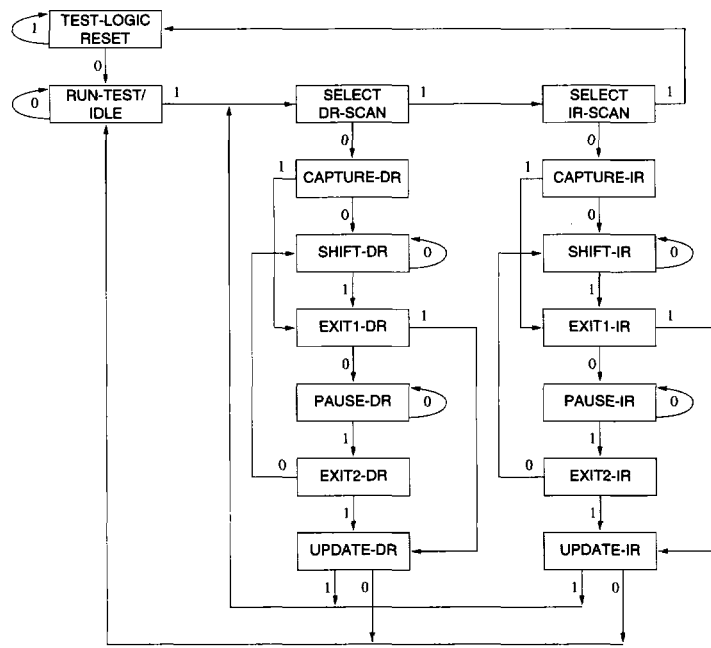


Figure 3
TAP CONTROLLER STATE DIAGRAM

NOTE: The 0/1 next to each state represents the value of TMS at the rising edge of TCK.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information into the registers and can be connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see Figure 3. TDI is internally pulled up and can be unconnected if the TAP is not used in an application. TDI is connected to the most significant bit (MSB) of any register. (See Figure 4.)

TEST DATA-OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending upon the current state of the TAP state machine. (See Figure 3.) The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register. (See Figure 4.)

PERFORMING A TAP RESET

The TAP circuitry does not have a reset pin (TRST#, which is optional in the IEEE 1149.1 specification). A RESET can be performed for the TAP controller by forcing TMS HIGH (V_{DD}) for five rising edges of TCK. This RESET does not affect the operation of the SRAM and may be performed while the SRAM is operating.

At power-up, the TAP is reset internally to ensure that TDO comes up in a High-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction register. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

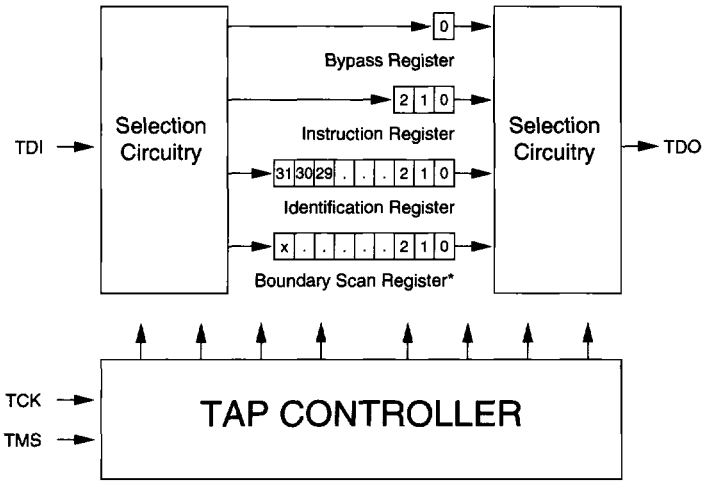
INSTRUCTION REGISTER

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins as shown in Figure 3. Upon power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary "01" pattern to allow for fault isolation of the board-level serial test data path.

BYPASS REGISTER

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between the TDI and TDO pins to allow data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (V_{SS}) when the BYPASS instruction is executed.



*x = 50 for the x18 configuration, and x = 69 for the x36 configuration.

Figure 4
TAP CONTROLLER BLOCK DIAGRAM

BOUNDARY SCAN REGISTER

The boundary scan register is connected to all the input and bidirectional pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve address bits for 9Mb and 18Mb Late Write SRAMs. The x36 configuration has a 70-bit-long register, and the x18 configuration has a 51-bit-long register.

The boundary scan register is loaded with the contents of the RAM I/O ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the I/O ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

IDENTIFICATION (ID) REGISTER

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in the Identification Register Definitions table.

TAP INSTRUCTION SET

OVERVIEW

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in the Instruction Codes table. Three of these instructions are listed as RESERVED and should not be used. The other five instructions are described in detail below.

The TAP controller used in this SRAM is not fully compliant to the 1149.1 convention because some of the mandatory 1149.1 instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals into the SRAM and cannot preload the I/O buffers. The SRAM does not implement the 1149.1 commands EXTEST, INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead, it performs a capture of the I/O ring when these instructions are executed.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction once it is shifted in, the TAP controller needs to be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. EXTEST is not implemented in the Late Write SRAM TAP controller, and therefore this device is not fully compliant to 1149.1.

The TAP controller does recognize an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is one difference between the two instructions. Unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state when this instruction is executed.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the device TAP controller is not fully 1149.1-compliant.

When the SAMPLE/PRELOAD instruction is loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and bidirectional pins is captured in the boundary scan register.

The user must be aware that the TAP controller clock can only operate at a frequency up to 10 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state an input or output will undergo a transition. The TAP may then try to capture a signal while in transition (metastable state). This will not harm the SRAM, but there is no guarantee as to the value that will be captured. Repeatable results may not be possible.

To guarantee that the boundary scan register will capture the correct value of a signal, the SRAM signal must be stabilized long enough to meet the TAP controller's capture setup plus hold time (^{t}CS plus ^{t}CH). The SRAM clock input

might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK# captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between TDI and TDO. The advantage of the BYPASS instruction is a shortened boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

TAP AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	1ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Test load termination supply voltage	1.5V

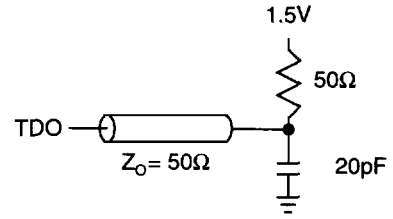


Figure 5
TAP AC OUTPUT LOAD EQUIVALENT

TAP DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

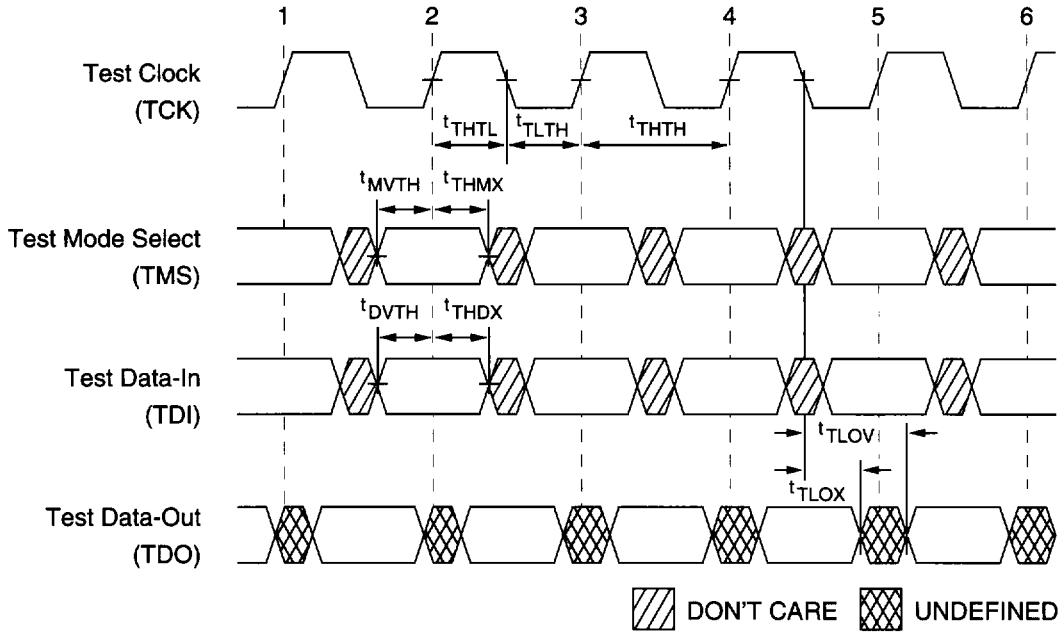
(20°C ≤ T_J ≤ 110°C; +3.1V ≤ V_{DD} ≤ +3.6V unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{DD} + 0.3	V	1, 2
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}	I_{LI}	-5.0	5.0	µA	
Output Leakage Current	Output(s) disabled, 0V ≤ V_{IN} ≤ $V_{DD}Q$ (DQx)	I_{LO}	-5.0	5.0	µA	
LVCMOS Output Low Voltage	I_{OLC} = 100µA	V_{OLC}		0.2	V	1, 3
LVCMOS Output High Voltage	$\|I_{OHC}\|$ = 100µA	V_{OHC}	V_{DD} - 0.2		V	1, 3
LVTTL Output Low Voltage	I_{OLT} = 8mA	V_{OLT}		0.4	V	1
LVTTL Output High Voltage	$\|I_{OHT}\|$ = 8mA	V_{OHT}	2.4		V	1

NOTE: 1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} (AC) ≤ V_{DD} + 1.5V for t ≤ $^tKHKH/2$
Undershoot: V_{IL} (AC) ≥ -0.5V for t ≤ $^tKHKH/2$
Power-up: V_{IH} ≤ +3.6V and V_{DD} ≤ 3.135V and $V_{DD}Q$ ≤ 1.4V for t ≤ 200ms
During normal operation, $V_{DD}Q$ must not exceed V_{DD}. Control input signals (such as SS#, SW#, etc.) may not have pulse widths less than ^tKHKL (MIN) or operate at frequencies exceeding ^fKF (MAX).
3. This parameter is sampled.

NEW LATE WRITE SRAM

TAP TIMING



TAP AC ELECTRICAL CHARACTERISTICS

(Notes 1, 2) (20°C ≤ T_J ≤ 110°C; +3.1V ≤ V_{DD} ≤ +3.6V)

DESCRIPTION	SYMBOL	MIN	MAX	UNITS
Clock				
Clock cycle time	^tTHTH	100		ns
Clock frequency	^fTF		10	MHz
Clock HIGH time	^tTHTL	40		ns
Clock LOW time	^tTLTH	40		ns
Output Times				
TCK LOW to TDO unknown	^tTLOX	0		ns
TCK LOW to TDO valid	^tTLOV		20	ns
TDI valid to TCK HIGH	^tDVTH	10		ns
TCK HIGH to TDI invalid	^tTHDX	10		ns
Setup Times				
TMS setup	^tMVTH	10		ns
Capture setup	^tCS	10		ns
Hold Times				
TMS hold	^tTHMX	10		ns
Capture hold	^tCH	10		ns

NOTE: 1. ^tCS and ^tCH refer to the setup and hold time requirements of latching data from the boundary scan register.
2. Test conditions are specified using the load in Figure 5.

IDENTIFICATION REGISTER DEFINITIONS

INSTRUCTION FIELD	256K x 18	128K x 36	DESCRIPTION
REVISION NUMBER (31:28)	xxxx	xxxx	Reserved for version number.
DEVICE DEPTH (27:23)	00110	00101	Defines depth of 256K or 128K words.
DEVICE WIDTH (22:18)	00011	00100	Defines width of x18 or x36 bits.
RESERVED (17:12)	xxxxx	xxxxx	Reserved for future use.
Micron JEDEC ID CODE (11:1)	00000101100	00000101100	Allows unique identification of SRAM vendor.
ID Register Presence Indicator (0)	1	1	Indicates the presence of an ID register.

SCAN REGISTER SIZES

REGISTER NAME	BIT SIZE (x18)	BIT SIZE (x36)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	51	70

INSTRUCTION CODES

INSTRUCTION	CODE	DESCRIPTION
EXTEST	000	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output to High-Z state. This instruction is not 1149.1-compliant.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operations.
SAMPLE Z	010	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High-Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the boundary scan register between TDI and TDO. Does not affect SRAM operation. This instruction does not implement 1149.1 PRELOAD function and is therefore not 1149.1-compliant.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operations.

NEW LATE WRITE SRAM

BOUNDARY SCAN ORDER (x18)

BIT#	SIGNAL NAME	BUMP ID
1	M2[1]	5R
2	SA	6T
3	SA	4P
4	SA	6R
5	SA	5T
6	ZZ	7T
7	DQa	7P
8	DQa	6N
9	DQa	6L
10	DQa	7K
11	BWa#	5L
12	CK#	4L
13	CK	4K
14	OE#	4F
15	DQa	6H
16	DQa	7G
17	DQa	6F
18	DQa	7E
19	DQa	6D
20	SA	6A
21	SA	6C
22	SA	5C
23	SA	5A
24	NC[2, 4]	6B
25	SA	5B
26	SA	3B

BIT#	SIGNAL NAME	BUMP ID
27	NC[3, 4]	2B
28	SA	3A
29	SA	3C
30	SA	2C
31	SA	2A
32	DQb	1D
33	DQb	2E
34	DQb	2G
35	DQb	1H
36	BWb#	3G
37	NC[4]	4D
38	SS#	4E
39	NC[4]	4G
40	NC[4]	4H
41	SW#	4M
42	DQb	2K
43	DQb	1L
44	DQb	2M
45	DQb	1N
46	DQb	2P
47	SA	3T
48	SA	2R
49	SA	4N
50	SA	2T
51	M1[1]	3R

NOTE:
1. M1 and M2 signals will be scanned out as V_{SS} and V_{DD}, respectively.
2. Reserved address bit for 9Mb Late Write SRAM.
3. Reserved address bit for 18Mb Late Write SRAM.
4. NC pads are true no connects. NC pads represent placeholder bits and are reserved for use as address bits on higher-density Late Write SRAMs that use the same boundary scan order. When reading out the boundary scan register, these bits are forced HIGH.

BOUNDARY SCAN ORDER (x36)

BIT#	SIGNAL NAME	BUMP ID
1	M2[1]	5R
2	SA	4P
3	SA	4T
4	SA	6R
5	SA	5T
6	ZZ	7T
7	DQa	6P
8	DQa	7P
9	DQa	6N
10	DQa	7N
11	DQa	6M
12	DQa	6L
13	DQa	7L
14	DQa	6K
15	DQa	7K
16	BWa#	5L
17	CK#	4L
18	CK	4K
19	OE#	4F
20	BWb#	5G
21	DQb	7H
22	DQb	6H
23	DQb	7G
24	DQb	6G
25	DQb	6F
26	DQb	7E
27	DQb	6E
28	DQb	7D
29	DQb	6D
30	SA	6A
31	SA	6C
32	SA	5C
33	SA	5A
34	NC[2, 4]	6B
35	SA	5B

BIT#	SIGNAL NAME	BUMP ID
36	SA	3B
37	NC[3, 4]	2B
38	SA	3A
39	SA	3C
40	SA	2C
41	SA	2A
42	DQc	2D
43	DQc	1D
44	DQc	2E
45	DQc	1E
46	DQc	2F
47	DQc	2G
48	DQc	1G
49	DQc	2H
50	DQc	1H
51	BWc#	3G
52	NC[4]	4D
53	SS#	4E
54	NC[4]	4G
55	NC[4]	4H
56	SW#	4M
57	BWd#	3L
58	DQd	1K
59	DQd	2K
60	DQd	1L
61	DQd	2L
62	DQd	2M
63	DQd	1N
64	DQd	2N
65	DQd	1P
66	DQd	2P
67	SA	3T
68	SA	2R
69	SA	4N
70	M1[1]	3R

NOTE:
1. M1 and M2 signals will be scanned out as V_{SS} and V_{DD}, respectively.
2. Reserved address bit for 9Mb Late Write SRAM.
3. Reserved address bit for 18Mb Late Write SRAM.
4. NC pads are true no connects. NC pads represent placeholder bits and are reserved for use as address bits on higher-density Late Write SRAMs that use the same boundary scan order. When reading out the boundary scan register, these bits are forced HIGH.