



1GB – 2x64Mx72 DDR SDRAM UNBUFFERED

FEATURES

- Double-data rate architecture
- DDR200, DDR266, DDR333 and DDR400
 - JEDEC design specifications
- BI-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2,2.5 (clock)
- Programmable Burst Length (2,4,8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input.
- Auto and self refresh
- Serial presence detect
- Dual Rank
- Power supply:
 - $V_{CC} = V_{CCQ} = +2.5V \pm 0.20V$ (100, 133, 166MHz)
 - $V_{CC} = V_{CCQ} = +2.6V \pm 0.10V$ (200MHz)
- JEDEC Standard 184 pin DIMM package
 - PCB height: 30.48 (1.20")

DESCRIPTION

the W3EG72128S is a 2x64Mx72 Double data Rate SDRAM memory module based on 512Mb DDR SDRAM components. The module consists of eighteen 64Mx8 DDR SDRAMs in 66 pin TSOP packages mounted on a 184 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	DDR400 @CL=3	DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5	DDR200 @CL=2
Clock Speed	200MHz	166MHz	133MHz	133MHz	100MHz
CL-t _{RC} -t _{RP}	3-3-3	2.5-3-3	2-2-2	2.5-3-3	2-2-2



PIN CONFIGURATION

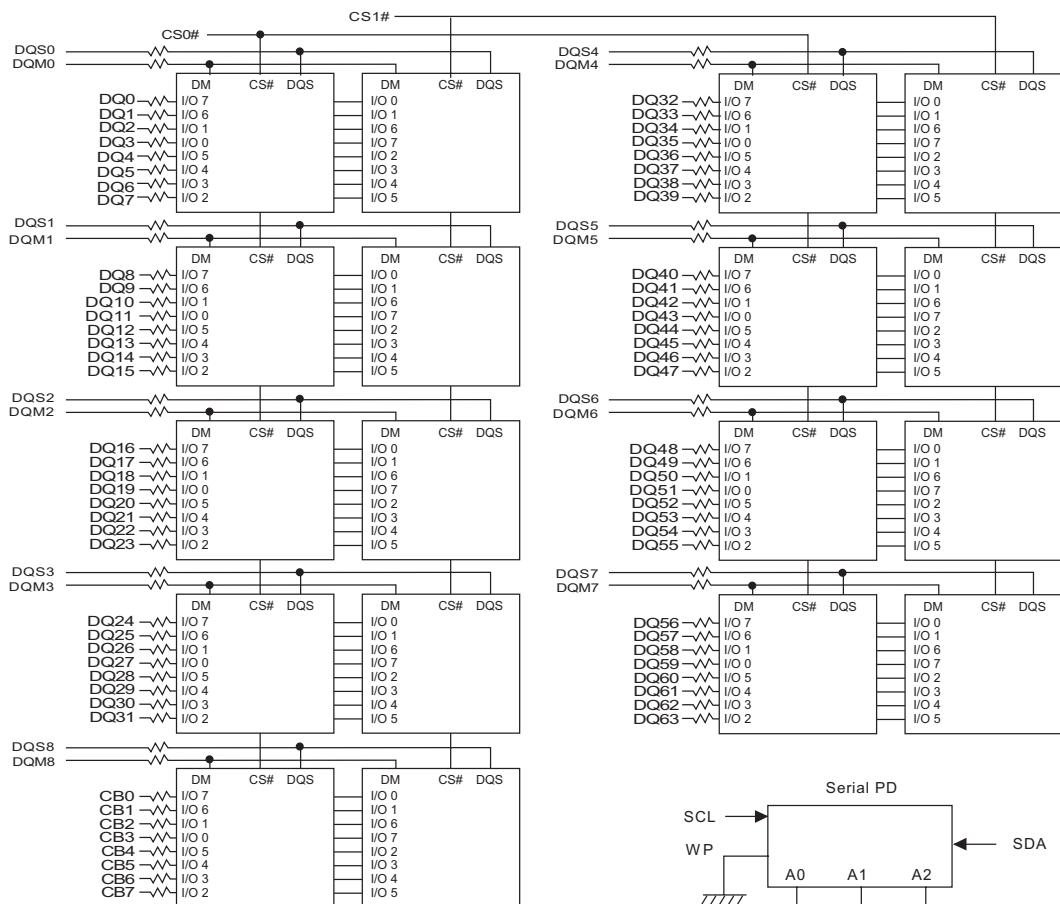
PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	47	DQS8	93	Vss	139	Vss
2	DQ0	48	A0	94	DQ4	140	DQM8
3	Vss	49	CB2	95	DQ5	141	A10
4	DQ1	50	Vss	96	Vccq	142	CB6
5	DQS0	51	CB3	97	DQM0	143	Vccq
6	DQ2	52	BA1	98	DQ6	144	CB7
7	Vcc	53	DQ32	99	DQ7	145	Vss
8	DQ3	54	Vccq	100	Vss	146	DQ36
9	NC	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC	148	Vcc
11	Vss	57	DQ34	103	NC	149	DQM4
12	DQ8	58	Vss	104	Vccq	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	Vss
15	Vccq	61	DQ40	107	DQM1	153	DQ44
16	CK1	62	Vccq	108	Vcc	154	RAS#
17	CK1#	63	WE#	109	DQ14	155	DQ45
18	Vss	64	DQ41	110	DQ15	156	Vccq
19	DQ10	65	CAS#	111	CKE1	157	CS0#
20	DQ11	66	Vss	112	Vccq	158	CS1#
21	CKE0	67	DQS5	113	NC	159	DQM5
22	Vccq	68	DQ42	114	DQ20	160	Vss
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	Vcc	116	Vss	162	DQ47
25	DQS2	71	NC	117	DQ21	163	NC
26	Vss	72	DQ48	118	A11	164	Vccq
27	A9	73	DQ49	119	DQM2	165	DQ52
28	DQ18	74	Vss	120	Vcc	166	DQ53
29	A7	75	CK2#	121	DQ22	167	NC
30	VCCQ	76	CK2	122	A8	168	Vcc
31	DQ19	77	Vccq	123	DQ23	169	DQM6
32	A5	78	DQS6	124	Vss	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	Vss	80	DQ51	126	DQ28	172	Vccq
35	DQ25	81	Vss	127	DQ29	173	NC
36	DQS3	82	Vccid	128	Vccq	174	DQ60
37	A4	83	DQ56	129	DQM3	175	DQ61
38	Vcc	84	DQ57	130	A3	176	Vss
39	DQ26	85	Vcc	131	DQ30	177	DQM7
40	DQ27	86	DQS7	132	Vss	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	Vss	88	DQ59	134	CB4	180	Vccq
43	A1	89	Vss	135	CB5	181	SA0
44	CB0	90	NC	136	Vccq	182	SA1
45	CB1	91	SDA	137	CK0	183	SA2
46	Vcc	92	SCL	138	CK0#	184	Vccspd

PIN NAMES

A0-A12	Address Input (Multiplexed)
BA0-BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CB0-CB7	Check bits
DQS0-DQS7	Data Strobe Input/Output
CK0, CK1, CK2	Clock Input
CK0#, CK1#, CK2#	Clock Input
CKE0, CKE1	Clock Enable input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
DQM0-DQM7	Data-In Mask
Vcc	Power Supply
Vccq	Power Supply for DQS
Vss	Ground
VREF	Power Supply for Reference
Vccspd	Serial EEPROM Power Supply
SDA	Serial data I/O
SCL	Serial clock
SA0-SA2	Address in EEPROM
Vccid	Vcc Identification Flag
NC	No Connect

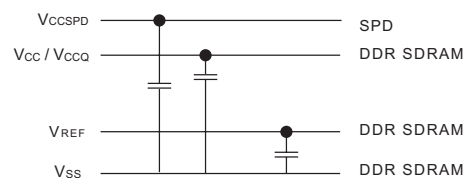


FUNCTIONAL BLOCK DIAGRAM



BA0-BA1 → BA0-BA1: DDR SDRAMs
A0-A12 → A0-A12: DDR SDRAMs
RAS# → RAS#: DDR SDRAMs
CAS# → CAS#: DDR SDRAMs
CKE1 → CKE: DDR SDRAMs
CKE0 → CKE: DDR SDRAMs
WE# → WE#: DDR SDRAMs

Clock Input	SDRAMs
CK0/CK0#	6 SDRAMs
CK1/CK1#	6 SDRAMs
CK2/CK2#	6 SDRAMs



NOTE: All resistor values are 22 ohms unless otherwise specified

**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Value	Units
Voltage on any pin relative to V _{SS}	V _{IN} , V _{OUT}	-0.5 to 3.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC} , V _{CCQ}	-1.0 to 3.6	V
Storage Temperature	T _{STG}	-55 to +150	°C
Power Dissipation	P _D	18	W
Short Circuit Current	I _{OS}	50	mA

Note: Permanent device damage may occur if 'ABSOLUTE MAXIMUM RATINGS' are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability

DC CHARACTERISTICS0°C ≤ T_A ≤ 70°C, V_{CC} = 2.5V ± 0.2V

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	2.3	2.7	V
Supply Voltage	V _{CCQ}	2.3	2.7	V
Reference Voltage	V _{REF}	1.15	1.35	V
Termination Voltage	V _{TT}	1.15	1.35	V
Input High Voltage	V _{IH}	V _{REF} + 0.15	V _{CCQ} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	V _{REF} - 0.15	V
Output High Voltage	V _{OH}	V _{TT} + 0.76	—	V
Output Low Voltage	V _{OL}	—	V _{TT} - 0.76	V

CAPACITANCET_A = 25°C, f = 1MHz, V_{CC} = 2.5V ± 0.2V

Parameter	Symbol	Max	Unit
Input Capacitance (A0-A12)	C _{IN1}	59	pF
Input Capacitance (RAS#, CAS#, WE#)	C _{IN2}	59	pF
Input Capacitance (CKE0, CKE1)	C _{IN3}	32	pF
Input Capacitance (CK0#, CK0)	C _{IN4}	59	pF
Input Capacitance (CS0#, CS1#)	C _{IN5}	32	pF
Input Capacitance (DQM0-DQM8)	C _{IN6}	13	pF
Input Capacitance (BA0-BA1)	C _{IN7}	59	pF
Data input/output capacitance (DQ0-DQ63)(DQS)	C _{OUT}	13	pF
Data input/output capacitance (CB0-CB7)	C _{OUT}	13	pF



IDD SPECIFICATIONS AND TEST CONDITIONS

V_{CCQ} = 2.5V ± 0.2V, V_{CC} = 2.5V ± 0.2V; DDR400: V_{CC} = V_{CCQ} = 2.6V ± 0.1V

Includes DDR SDRAM component only

Parameter	Symbol	Conditions	DDR400@ CL=3 Max	DDR333@ CL=2.5 Max	DDR266@ CL=2 Max	DDR266@ CL=2.5 Max	DDR200@ CL=2 Max	Units
Operating Current	IDD0	One device bank; Active - Precharge; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two cycles.	2475	2070	2070	2070	2070	mA
Operating Current	IDD1	One device bank; Active-Read-Precharge Burst = 2; t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); I _{OUT} = 0mA; Address and control inputs changing once per clock cycle.	2745	2340	2340	2340	2340	mA
Precharge Power-Down Standby Current	IDD2P	All device banks idle; Power-down mode; t _{CK} =t _{CK} (MIN); CKE=(low)	90	90	90	90	90	mA
Idle Standby Current	IDD2F	CS# = High; All device banks idle; t _{CK} =t _{CK} (MIN); CKE = high; Address and other control inputs changing once per clock cycle. V _{IN} = V _{REF} for DQ, DQS and DM.	990	810	810	810	810	mA
Active Power-Down Standby Current	IDD3P	One device bank active; Power-Down mode; t _{CK} (MIN); CKE=(low)	810	630	630	630	630	mA
Active Standby Current	IDD3N	CS# = High; CKE = High; One device bank; Active-Precharge; t _{RC} =t _{RAS} (MAX); t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle.	1080	900	900	900	900	mA
Operating Current	IDD4R	Burst = 2; Reads; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); I _{OUT} = 0mA.	2790	2385	2385	2385	2385	mA
Operating Current	IDD4W	Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t _{CK} =t _{CK} (MIN); DQ, DM and DQS inputs changing once per clock cycle.	2835	2475	2475	2475	2475	mA
Auto Refresh Current	IDD5	t _{RC} = t _{RC} (MIN)	4185	3510	3510	3510	3510	mA
Self Refresh Current	IDD6	CKE ≤ 0.2V	90	90	90	90	90	mA
Operating Current	IDD7A	Four bank interleaving Reads (BL=4) with auto precharge with t _{RC} =t _{RC} (MIN); t _{CK} =t _{CK} (MIN); Address and control inputs change only during Active Read or Write commands.	5130	4545	4500	4500	4500	mA



DETAILED TEST CONDITIONS FOR DDR SDRAM I_{DD1} & I_{DD7A}

I_{DD1} : OPERATING CURRENT : ONE BANK

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Only one bank is accessed with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{OUT} = 0mA
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RCD}=2*t_{CK}, t_{RAS}=5*t_{CK}
Read : A0 N R0 N N P0 N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL=2, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=9*t_{CK}, t_{RAS}=5*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RCD}=10*t_{CK}, t_{RAS}=7*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst
 - DDR400 (200MHz, CL=3) : t_{CK}=5ns, BL=4, t_{RCD}=15*t_{CK}, t_{RAS}=7*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing; 50% of data changing at every burst

I_{DD7A} : OPERATING CURRENT : FOUR BANKS

1. Typical Case : V_{CC}=2.5V, T=25°C
2. Worst Case : V_{CC}=2.7V, T=10°C
3. Four banks are being interleaved with t_{RC} (min), Burst Mode, Address and Control inputs on NOP edge are not changing. I_{OUT}=0mA
4. Timing Patterns :
 - DDR200 (100 MHz, CL=2) : t_{CK}=10ns, CL2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 A0 R3 A1 R0 repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2.5) : t_{CK}=7.5ns, CL=2.5, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}
Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR266 (133MHz, CL=2) : t_{CK}=7.5ns, CL2=2, BL=4, t_{RRD}=2*t_{CK}, t_{RCD}=2*t_{CK}
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, BL=4, t_{RRD}=3*t_{CK}, t_{RCD}=3*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst
 - DDR400 (200MHz, CL=3) : t_{CK}=5ns, BL=4, t_{RRD}=10*t_{CK}, t_{RCD}=15*t_{CK}, Read with Autoprecharge
Read : A0 N A1 R0 A2 R1 A3 R2 N R3 A0 N A1 R0 - repeat the same timing with random address changing; 100% of data changing at every burst

Legend:

A = Activate, R = Read, W = Write, P = Precharge, N = NOP

A (0-3) = Activate Bank 0-3

R (0-3) = Read Bank 0-3



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

DDR400: $V_{CC} = V_{CCQ} = +2.6V \pm 0.1V$; DDR333, 266, 200: $V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$

AC Characteristics			403		335		262/265		202			
Parameter	Symbol		Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Access window of DQs from CK, CK#	t_{AC}		-0.70	+0.70	-0.70	+0.70	-0.75	+0.75	-0.75	+0.75	ns	
CK high-level width	t_{CH}		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	16
CK low-level width	t_{CL}		0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	16
Clock cycle time	CL=3	$t_{CK} (3)$	5	7.5	6	13	7.5	13	7.5	13	ns	22
	CL=2.5	$t_{CK} (2.5)$	6	13	6	13	7.5	13	7.5	13	ns	22
	CL=2	$t_{CK} (2)$	7.5	13	7.5	13	7.5	13	10	13	ns	22
DQ and DM input hold time relative to DQS	t_{DH}		0.45		0.45		0.5		0.5		ns	14,17
DQ and DM input setup time relative to DQS	t_{DS}		0.45		0.45		0.5		0.5		ns	14,17
DQ and DM input pulse width (for each input)	t_{DIPW}		1.75		1.75		1.75		1.75		ns	17
Access window of DQS from CK, CK#	t_{DQSCK}		-0.60	+0.60	-0.60	+0.60	-0.75	+0.75	-0.75	+0.75	ns	
DQS input high pulse width	t_{DQSH}		0.35			0.35	0.35		0.35		t _{CK}	
DQS input low pulse width	t_{DQSL}		0.35			0.35	0.35		0.35		t _{CK}	
DQS-DQ skew, DQS to last DQ valid, per group, per access	t_{DQSQ}			0.40		0.45		0.5		0.5	ns	13,14
Write command to first DQS latching transition	t_{DQSS}		0.72	1.28	0.75	1.25	0.75	1.25	0.75	1.25	t _{CK}	
DQS falling edge to CK rising - setup time	t_{DSS}		0.2		0.2		0.2		0.2		t _{CK}	
DQS falling edge from CK rising - hold time	t_{DSH}		0.2		0.2		0.2		0.2		t _{CK}	
Half clock period	t_{HP}	t_{CH}, t_{CL}			t_{CH}, t_{CL}		t_{CH}, t_{CL}		t_{CH}, t_{CL}		ns	18
Data-out high-impedance window from CK, CK#	t_{HZ}			+0.70		+0.70		+0.75		+0.75	ns	8,19
Data-out low-impedance window from CK, CK#	t_{LZ}		-0.70		-0.70		-0.75		-0.75		ns	8,20
Address and control input hold time (fast slew rate)	t_{IHf}		0.60		0.75		0.90		0.90		ns	6
Address and control input set-up time (fast slew rate)	t_{ISf}		0.60		0.75		0.90		0.90		ns	6
Address and control input hold time (slow slew rate)	t_{IHs}		0.60		0.80		1		1		ns	6
Address and control input setup time (slow slew rate)	t_{ISs}		0.60		0.80		1		1		ns	6
Address and control input pulse width (for each input)	t_{IPW}		2.2		2.2		2.2		2.2		ns	
LOAD MODE REGISTER command cycle time	t_{MRD}		10		12		15		15		ns	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	$t_{HP}-t_{QHS}$			$t_{HP}-t_{QHS}$		$t_{HP}-t_{QHS}$		$t_{HP}-t_{QHS}$		ns	13,14
Data hold skew factor	t_{QHS}			0.55		0.55		0.75		0.75	ns	
ACTIVE to PRECHARGE command	t_{RAS}		40	70,000	42	70,000	40	120,000	45	120,000	ns	15
ACTIVE to READ with Auto precharge command	t_{RAP}		15		15		15		20		ns	
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}		55		60		60		65		ns	
AUTO REFRESH command period	t_{RFC}		70		72		75		75		ns	21



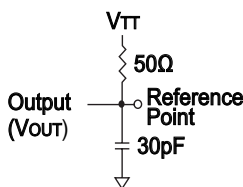
**DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND
RECOMMENDED AC OPERATING CONDITIONS (continued)**

DDR400: $V_{CC} = V_{CCQ} = +2.6V \pm 0.1V$; DDR333, 266, 200: $V_{CC} = V_{CCQ} = +2.5V \pm 0.2V$

AC Characteristics		403		335		262/265		202			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
ACTIVE to READ or WRITE delay	t_{RCD}	15		15		15		20		ns	
PRECHARGE command period	t_{RP}	15		15		15		20		ns	
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	10		12		15		15		ns	
DQS write preamble	t_{WPRE}	0.25		0.25		0.25		0.25		t _{CK}	
DQS write preamble setup time	t_{WPRES}	0		0		0		0		ns	10,11
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	9
Write recovery time	t_{WR}	15		15		15		15		ns	
Internal WRITE to READ command delay	t_{WTR}	2		1		1		1		t _{CK}	
Data valid output window	NA	$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		$t_{QH} - t_{DQSQ}$		ns	13
REFRESH to REFRESH command interval	t_{REFC}		70.3		70.3		70.3		70.3	μs	12
Average periodic refresh interval	t_{REFI}		7.8		7.8		7.8		7.8	μs	12
Terminating voltage delay to V_{CC}	t_{VTD}	0		0		0		0		ns	
Exit SELF REFRESH to non-READ command	t_{XSNR}	70		75		75		75		ns	
Exit SELF REFRESH to READ command	t_{XSRD}	200		200		200		200		t _{CK}	

**Notes**

1. All voltages referenced to V_{SS}
2. Tests for AC timing, I_{DD} , and electrical AC and DC characteristics may be conducted at normal reference / supply voltage levels, but the related specifications and device operations are guaranteed for the full voltage range specified.
3. Outputs are measured with equivalent load:



4. AC timing and I_{DD} tests may use a V_{IL} -to- V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to V_{REF} (or to the crossing point for CK/CK#), and parameter specifications are guaranteed for the specified AC input levels under normal use conditions. The minimum slew rate for the input signals used to test the device is 1V/ns in the range between $V_{IL}(AC)$ and $V_{IH}(AC)$.
5. The AC and DC input level specifications are defined in the SSTL_2 standard (i.e., the receiver will effectively switch as a result of the signal crossing the AC input level, and will remain in that state as long as the signal does not ring back above [below] the DC input LOW [high] level).
6. For slew rates less than 1V/ns and greater than or equal to 0.5V/ns. If the slew rate is less than 0.5V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100mV/ns reduction in slew rate from the 500mV/ns. t_{IH} has 0ps added, that is, it remains constant. If the slew rate exceeds 4.5V/ns, functionality is uncertain. For 403 and 335, slew rates must be greater than or equal to 0.5V/ns.
7. Inputs are not recognized as valid until V_{REF} stabilizes. Exception: during the period before V_{REF} stabilizes, $CKE \leq 0.3 \times V_{CCQ}$ is recognized as LOW.
8. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) and begins driving (LZ).
9. The intent of the "Don't Care" state after completion of the postamble is the DQS-driven signal should either be HIGH, LOW, or high-Z, and that any signal transition within the input switching region must follow valid input requirements. That is, if DQS transitions HIGH (above V_{IHDC} (MIN)) then it must not transition LOW (below V_{IHDC}) prior to t_{DQSH} (MIN).
10. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
11. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic LOW) applies when no WRITES were previously in progress on the bus. If a previous WRITE was in progress, DQS could be high during this time, depending on t_{BOSS} .
12. The refresh period is 64ms. This equates to an average refresh rate of 7.8125 μ s. However, an AUTO REFRESH command must be asserted at least once every 70.3 μ s; burst refreshing or posting by the DRAM controller greater than eight refresh cycles is not allowed.
13. The valid data window is derived by achieving other specifications - t_{HP} ($t_{CK}/2$), t_{DQSQ} , and t_{QH} ($t_{QH} = t_{HP} - t_{QHS}$). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is allowed a maximum duty cycled variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio. The data valid window derating curves are provided below for duty cycles ranging between 50/50 and 45/55.
14. Referenced to each output group: $x8 = DQS$ with $DQ0-DQ7$.
15. READs and WRITEs with auto precharge are not allowed to be issued until t_{RAS} (MIN) can be satisfied prior to the internal precharge command being issued.
16. JEDEC specifies CK and CK# input slew rate must be $\geq 1V/ns$ (2V/ns differentially).
17. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/DQS slew rate is less than 0.5V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100mV/ns reduction in slew rate. If slew rates exceed 4V/ns, functionality is uncertain.
18. t_{HP} min is the lesser of t_{CL} min and t_{CH} min actually applied to the device CK and CK# inputs, collectively during bank active.
19. t_{HZ} (MAX) will prevail over the t_{DQSQ} (MAX) + t_{RPST} (MAX) condition. t_{LZ} (MIN) will prevail over t_{DQSQ} (MIN) + PRE (MAX) condition.
20. For slew rates greater than 1V/ns the (LZ) transition will start about 310ps earlier.
21. CKE must be active (High) during the entire time a refresh command is executed. That is, from the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge, until t_{RFC} has been satisfied.
22. Whenever the operating frequency is altered, not including jitter, the DLL is required to be reset. This is followed by 200 clock cycles (before READ commands).

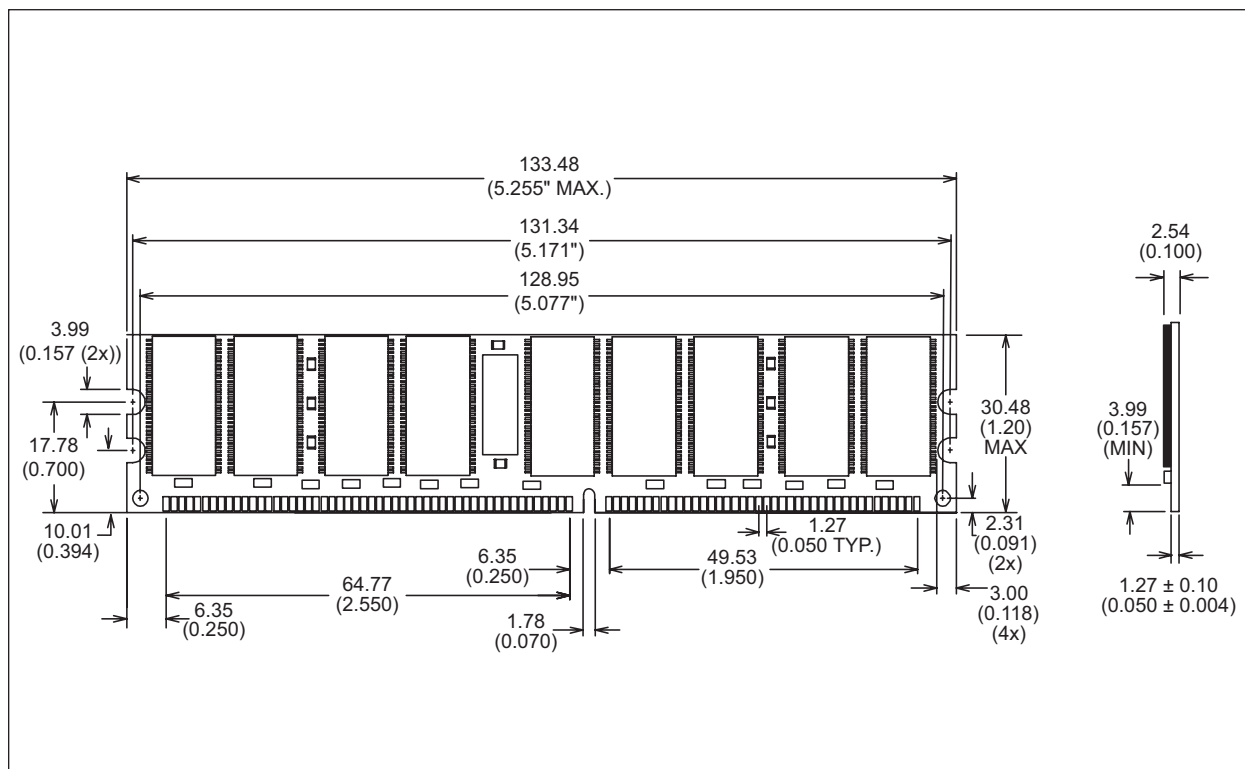


ORDERING INFORMATION FOR JD3

Part Number	Speed	CAS Latency	t _{RCD}	t _{RP}	Height*
W3EG72128S403JD3	200MHz/400Mb/s	3	3	3	30.48 (1.20")
W3EG72128S335JD3	166MHz/333Mb/s	2.5	3	3	30.48 (1.20")
W3EG72128S262JD3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG72128S265JD3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")
W3EG72128S202JD3	100MHz/200Mb/s	2	2	2	30.48 (1.20")

- NOTES:
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
 - Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
 - Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR JD3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

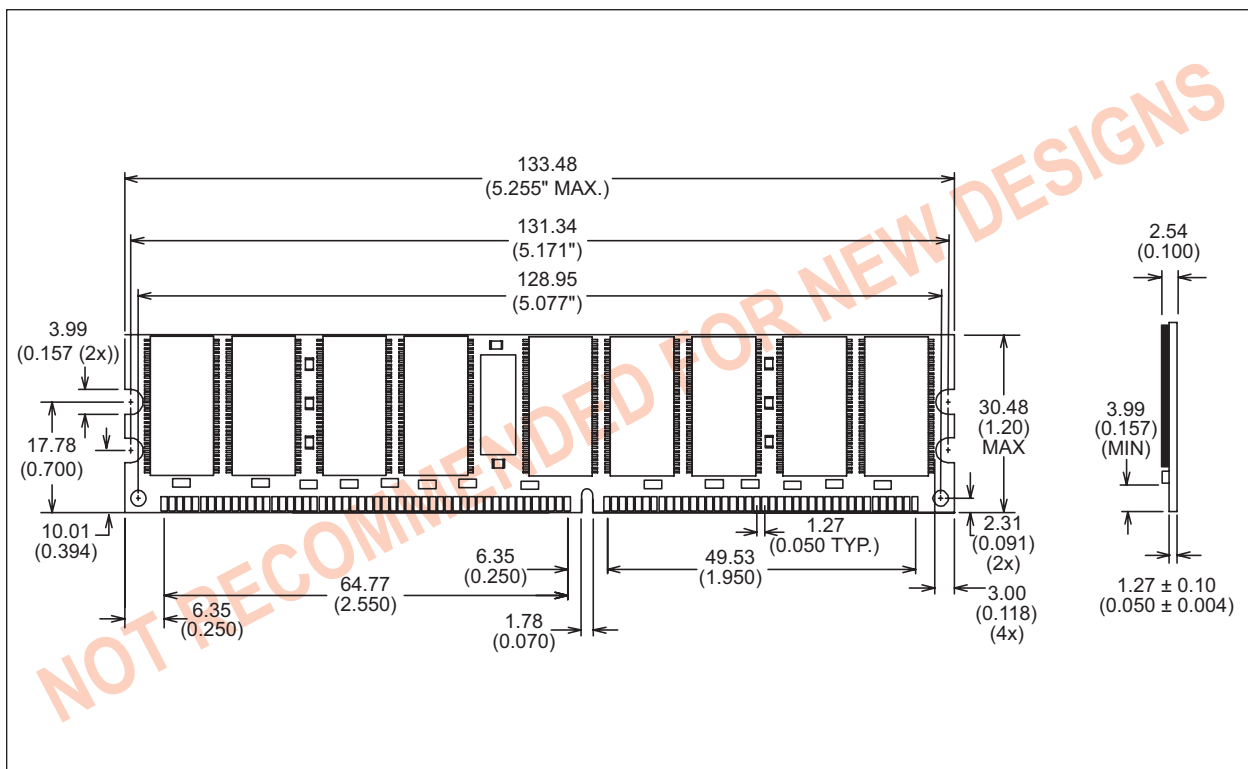


ORDERING INFORMATION FOR D3

Part Number	Speed	CAS Latency	t _{RCD}	t _{RP}	Height*
W3EG72128S403D3	200MHz/400Mb/s	3	3	3	30.48 (1.20")
W3EG72128S335D3	166MHz/333Mb/s	2.5	3	3	30.48 (1.20")
W3EG72128S262D3	133MHz/266Mb/s	2	2	2	30.48 (1.20")
W3EG72128S265D3	133MHz/266Mb/s	2.5	3	3	30.48 (1.20")
W3EG72128S202D3	100MHz/200Mb/s	2	2	2	30.48 (1.20")

- NOTES:
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
 - Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
 - Consult factory for availability of industrial temperature (-40°C to 85°C) option

PACKAGE DIMENSIONS FOR D3



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



Document Title

1GB – 2x64Mx72 DDR SDRAM UNBUFFERED

Revision History

Rev #	History	Release Date	Status
Rev A	Created Datasheet	3-6-02	Advanced
Rev B	Corrected Mechanical Drawing	5-22-02	Advanced
Rev C	Added 333MHz speed	2-3-02	Advanced
Rev 0	0.1 Added 400MHz speed 0.2 Updated AC specs	10-4-04	Advanced
Rev 1	1.1 Updated I _{DD} specs 1.2 Updated CAP specs	11-04	Advanced
Rev 2	2.1 Added lead-free notes	12-04	Advanced
Rev 3	3.1 Added JEDEC Standard (JD3) Package Option 3.2 D3 Not Recommended For New Designs.	5-05	Advanced