



HIGH-SPEED 2.5V 256/128/64K x 36 SYNCHRONOUS DUAL-PORT STATIC RAM WITH 3.3V OR 2.5V INTERFACE

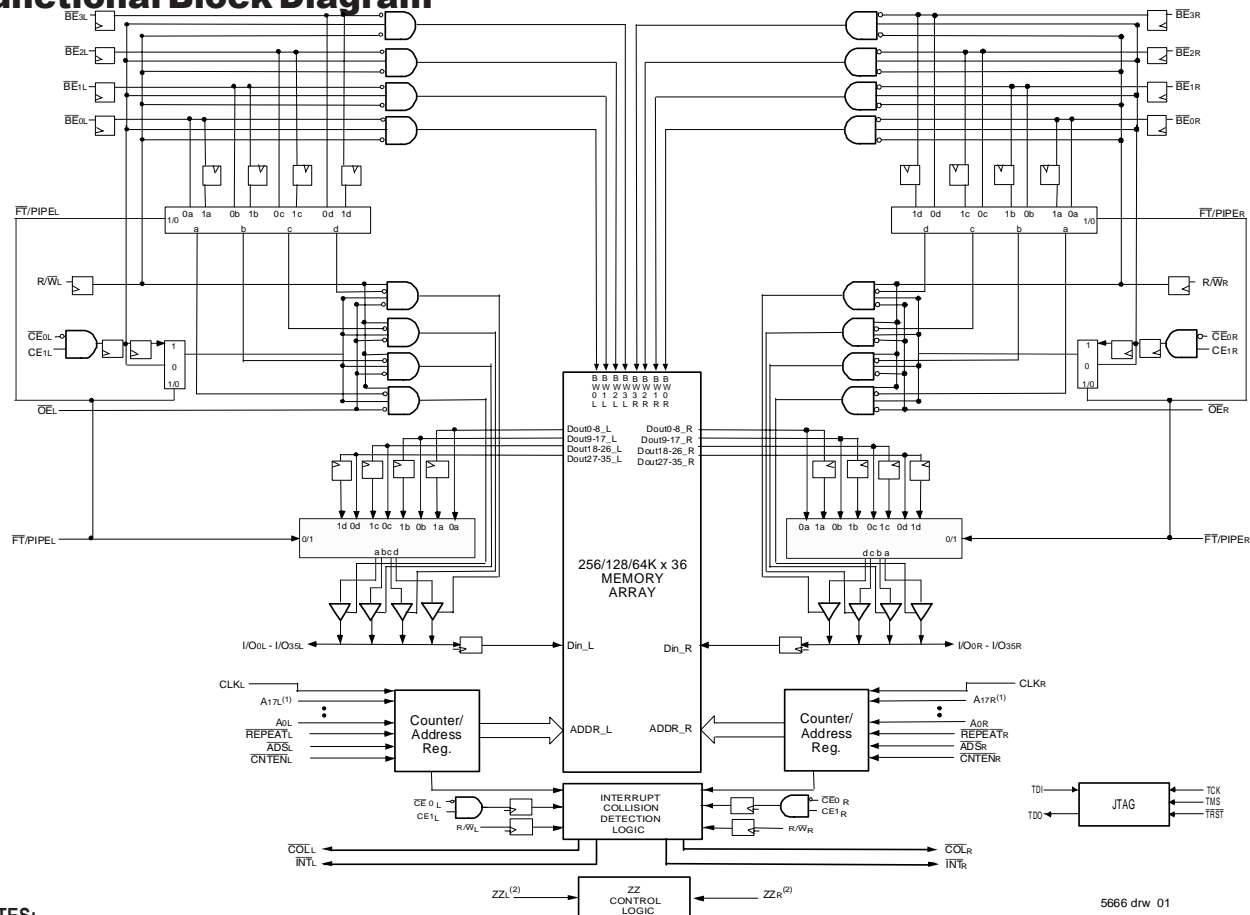
IDT70T3519/99/89S

Features:

- ◆ True Dual-Port memory cells which allow simultaneous access of the same memory location
- ◆ High-speed data access
 - Commercial: 3.4 (200MHz)/3.6ns (166MHz)/4.2ns (133MHz)(max.)
 - Industrial: 3.6ns (166MHz)/4.2ns (133MHz) (max.)
- ◆ Selectable Pipelined or Flow-Through output mode
- ◆ Counter enable and repeat features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Interrupt and Collision Detection Flags
- ◆ Full synchronous operation on both ports
 - 5ns cycle time, 200MHz operation (14Gbps bandwidth)
 - Fast 3.4ns clock to data out
 - 1.5ns setup to clock and 0.5ns hold on all control, data, and address inputs @ 200MHz

- Data input, address, byte enable and control registers
- Self-timed write allows fast cycle time
- ◆ Separate byte controls for multiplexed bus and bus matching compatibility
- ◆ Dual Cycle Deselect (DCD) for Pipelined Output Mode
- ◆ 2.5V ($\pm 100\text{mV}$) power supply for core
- ◆ LVTTTL compatible, selectable 3.3V ($\pm 150\text{mV}$) or 2.5V ($\pm 100\text{mV}$) power supply for I/Os and control signals on each port
- ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available at 166MHz and 133MHz
- ◆ Available in a 256-pin Ball Grid Array (BGA), a 208-pin Plastic Quad Flatpack (PQFP) and 208-pin fine pitch Ball Grid Array (fpBGA)
- ◆ Supports JTAG features compliant with IEEE 1149.1
- ◆ Due to limited pin count JTAG is not supported on the 208-pin PQFP package

Functional Block Diagram



NOTES:

1. Address A17 is a NC for the IDT70T3599. Also, Addresses A17 and A16 are NC's for the IDT70T3589.
2. The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/FTx and OPTx and the sleep mode pins themselves (ZZx) are not affected during sleep mode.

5666 drw 01

APRIL 2004

Description:

The IDT70T3519/99/89 is a high-speed 256/128/64K x 36 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times. With an input data register, the IDT70T3519/99/89 has been optimized for applications having unidirec-

tional or bidirectional data flow in bursts. An automatic power down feature, controlled by $\overline{CE}0$ and $CE1$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The 70T3519/99/89 can support an operating voltage of either 3.3V or 2.5V on one or both ports, controllable by the OPT pins. The power supply for the core of the device (V_{DD}) is at 2.5V.

Pin Configuration (3,4,5,6,9)

70T3519/99/89BC
BC-256⁽⁷⁾256-Pin BGA
Top View⁽⁸⁾

06/19/02

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16
NC	TDI	NC	A17L ⁽¹⁾	A14L	A11L	A8L	\overline{BE}_{2L}	CE1L	\overline{OE}_{L}	CNTENL	A5L	A2L	A0L	NC	NC
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16
I/O18L	NC	TDO	NC	A15L	A12L	A9L	\overline{BE}_{3L}	\overline{CE}_{0L}	R/WL	REPEATL	A4L	A1L	VDD	I/O17L	NC
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16
I/O18R	I/O19L	VSS	A16L ⁽²⁾	A13L	A10L	A7L	\overline{BE}_{1L}	\overline{BE}_{0L}	CLKL	ADSL	A6L	A3L	OPTL	I/O17R	I/O16L
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16
I/O20R	I/O19R	I/O20L	PIPE/FTL	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDD	I/O15R	I/O15L	I/O16R
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	E16
I/O21R	I/O21L	I/O22L	VDDQL	VDD	VDD	\overline{INTL}	VSS	VSS	VSS	VDD	VDD	VDDQR	I/O13L	I/O14L	I/O14R
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11	F12	F13	F14	F15	F16
I/O23L	I/O22R	I/O23R	VDDQL	VDD	NC	\overline{COLL}	VSS	VSS	VSS	VSS	VDD	VDDQR	I/O12R	I/O13R	I/O12L
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11	G12	G13	G14	G15	G16
I/O24R	I/O24L	I/O25L	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O10L	I/O11L	I/O11R
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11	H12	H13	H14	H15	H16
I/O26L	I/O25R	I/O26R	VDDQR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQL	I/O9R	I/O9L	I/O10R
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
I/O27L	I/O28R	I/O27R	VDDQL	ZZR	VSS	VSS	VSS	VSS	VSS	VSS	VSS	ZZL	VDDQR	I/O8R	I/O7R
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11	K12	K13	K14	K15	K16
I/O29R	I/O29L	I/O28L	VDDQL	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQR	I/O6R	I/O6L	I/O7L
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11	L12	L13	L14	L15	L16
I/O30L	I/O31R	I/O30R	VDDQR	VDD	NC	\overline{COLR}	VSS	VSS	VSS	VSS	VDD	VDDQL	I/O5L	I/O4R	I/O5R
M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	M11	M12	M13	M14	M15	M16
I/O32R	I/O32L	I/O31L	VDDQR	VDD	VDD	\overline{INTR}	VSS	VSS	VSS	VDD	VDD	VDDQL	I/O3R	I/O3L	I/O4L
N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11	N12	N13	N14	N15	N16
I/O33L	I/O34R	I/O33R	PIPE/FTR	VDDQR	VDDQR	VDDQL	VDDQL	VDDQR	VDDQR	VDDQL	VDDQL	VDD	I/O2L	I/O1R	I/O2R
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
I/O35R	I/O34L	TMS	A16R ⁽²⁾	A13R	A10R	A7R	\overline{BE}_{1R}	\overline{BE}_{0R}	CLKR	ADSR	A6R	A3R	I/O0L	I/O0R	I/O1L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16
I/O35L	NC	\overline{TRST}	NC	A15R	A12R	A9R	\overline{BE}_{3R}	\overline{CE}_{0R}	R/WR	REPEATR	A4R	A1R	OPTR	NC	NC
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16
NC	TCK	NC	A17R ⁽¹⁾	A14R	A11R	A8R	\overline{BE}_{2R}	CE1R	\overline{OE}_{R}	CNTENR	A5R	A2R	A0R	NC	NC

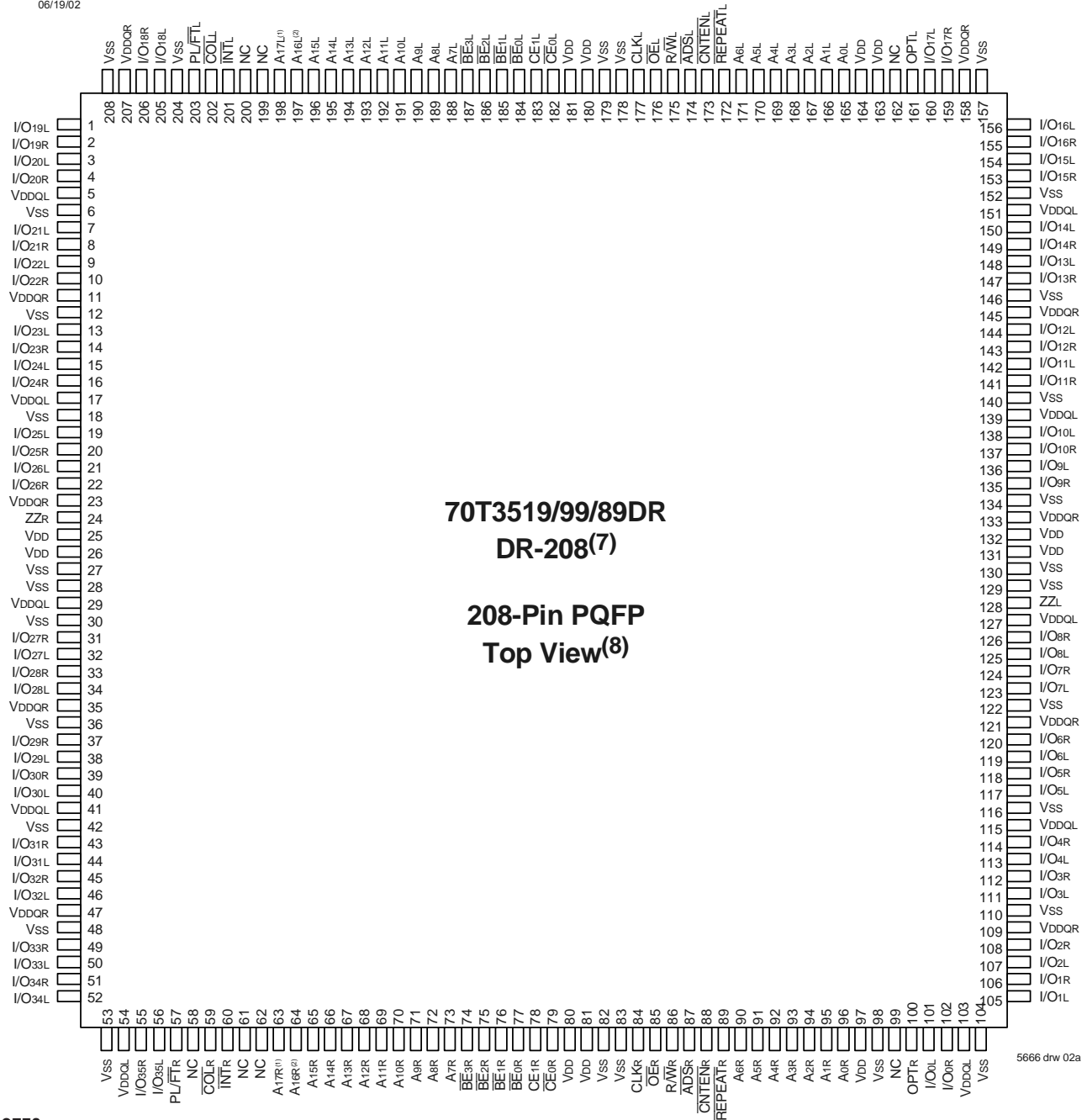
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NOTES:

- Pin is a NC for IDT70T3599 and IDT70T3589.
- Pin is a NC for IDT70T3589.
- All VDD pins must be connected to 2.5V power supply.
- All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VDD (2.5V), and 2.5V if OPT pin for that port is set to VSS (0V).
- All VSS pins must be connected to ground supply.
- Package body is approximately 17mm x 17mm x 1.4mm, with 1.0mm ball-pitch.
- This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.
- Pins A15 and T15 will be VREFL and VREFR respectively for future HSTL device.

Pin Configuration (3,4,5,6,9,10) (con't.)

06/19/02



NOTES:

1. Pin is a NC for IDT70T3599 and IDT70T3589.
2. Pin is a NC for IDT70T3589.
3. All VDD pins must be connected to 2.5V power supply.
4. All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VDD (2.5V), and 2.5V if OPT pin for that port is set to VSS (0V).
5. All VSS pins must be connected to ground supply.
6. Package body is approximately 28mm x 28mm x 3.5mm.
7. This package code is used to reference the package diagram.
8. This text does not indicate orientation of the actual part-marking.
9. Due to limited pin count, JTAG is not supported in the DR-208 package.
10. Pins 162 and 99 will be VREFL and VREFR respectively for future HSTL device.

Pin Configuration (3,4,5,6,9) (con't.)

01/23/03

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17
I/O19L	I/O18L	VSS	TDO	$\overline{\text{COLL}}$	A16L ⁽²⁾	A12L	A8L	$\overline{\text{BE}}_{1L}$	VDD	CLKL	$\overline{\text{CNTEN}}_L$	A4L	A0L	OPTL	I/O17L	VSS
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15	B16	B17
I/O20R	VSS	I/O18R	TDI	A17L ⁽¹⁾	A13L	A9L	$\overline{\text{BE}}_{2L}$	$\overline{\text{CE}}_{0L}$	VSS	$\overline{\text{ADS}}_L$	A5L	A1L	NC	VDDQR	I/O16L	I/O15R
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14	C15	C16	C17
VDDQL	I/O19R	VDDQR	PL/FTL	$\overline{\text{INT}}_L$	A14L	A10L	$\overline{\text{BE}}_{3L}$	CE1L	VSS	R/WL	A6L	A2L	VDD	I/O16R	I/O15L	VSS
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17
I/O22L	VSS	I/O21L	I/O20L	A15L	A11L	A7L	$\overline{\text{BE}}_{0L}$	VDD	$\overline{\text{OE}}_L$	$\overline{\text{REPEAT}}_L$	A3L	VDD	I/O17R	VDDQL	I/O14L	I/O14R
E1	E2	E3	E4	70T3519/99/89BF BF-208⁽⁷⁾ 208-Pin fpBGA Top View⁽⁸⁾								E14	E15	E16	E17	
I/O23L	I/O22R	VDDQR	I/O21R									I/O12L	I/O13R	VSS	I/O13L	
F1	F2	F3	F4									F14	F15	F16	F17	
VDDQL	I/O23R	I/O24L	VSS									VSS	I/O12R	I/O11L	VDDQR	
G1	G2	G3	G4									G14	G15	G16	G17	
I/O26L	VSS	I/O25L	I/O24R									I/O9L	VDDQL	I/O10L	I/O11R	
H1	H2	H3	H4									H14	H15	H16	H17	
VDD	I/O26R	VDDQR	I/O25R									VDD	I/O9R	VSS	I/O10R	
J1	J2	J3	J4									J14	J15	J16	J17	
VDDQL	VDD	VSS	ZZR									ZZL	VDD	VSS	VDDQR	
K1	K2	K3	K4	K14	K15	K16	K17									
I/O28R	VSS	I/O27R	VSS	I/O7R	VDDQL	I/O8R	VSS									
L1	L2	L3	L4	L14	L15	L16	L17									
I/O29R	I/O28L	VDDQR	I/O27L	I/O6R	I/O7L	VSS	I/O8L									
M1	M2	M3	M4	M14	M15	M16	M17									
VDDQL	I/O29L	I/O30R	VSS	VSS	I/O6L	I/O5R	VDDQR									
N1	N2	N3	N4	N14	N15	N16	N17									
I/O31L	VSS	I/O31R	I/O30L	I/O3R	VDDQL	I/O4R	I/O5L									
P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16	P17
I/O32R	I/O32L	VDDQR	I/O35R	$\overline{\text{TRST}}$	A16R ⁽²⁾	A12R	A8R	$\overline{\text{BE}}_{1R}$	VDD	CLKR	$\overline{\text{CNTEN}}_R$	A4R	I/O2L	I/O3L	VSS	I/O4L
R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	R17
VSS	I/O33L	I/O34R	TCK	A17R ⁽¹⁾	A13R	A9R	$\overline{\text{BE}}_{2R}$	$\overline{\text{CE}}_{0R}$	VSS	$\overline{\text{ADS}}_R$	A5R	A1R	NC	VDDQL	I/O1R	VDDQR
T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13	T14	T15	T16	T17
I/O33R	I/O34L	VDDQL	TMS	$\overline{\text{INT}}_R$	A14R	A10R	$\overline{\text{BE}}_{3R}$	CE1R	VSS	R/WR	A6R	A2R	VSS	I/O0R	VSS	I/O2R
U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15	U16	U17
VSS	I/O35L	PL/FTL	$\overline{\text{COLR}}$	A15R	A11R	A7R	$\overline{\text{BE}}_{0R}$	VDD	$\overline{\text{OE}}_R$	$\overline{\text{REPEAT}}_R$	A3R	A0R	VDD	OPTR	I/O0L	I/O1L

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NOTES:

- Pin is a NC for IDT70T3599 and IDT70T3589.
- Pin is a NC for IDT70T3589.
- All VDD pins must be connected to 2.5V power supply.
- All VDDQ pins must be connected to appropriate power supply: 3.3V if OPT pin for that port is set to VDD (2.5V), and 2.5V if OPT pin for that port is set to VSS (0V).
- All VSS pins must be connected to ground supply.
- Package body is approximately 15mm x 15mm x 1.4mm with 0.8mm ball pitch.
- This package code is used to reference the package diagram.
- This text does not indicate orientation of the actual part-marking.
- Pins B14 and R14 will be VREFL and VREFR respectively for future HSTL device.

Pin Names

Left Port	Right Port	Names
\overline{CE}_{0L} , CE_{1L}	\overline{CE}_{0R} , CE_{1R}	Chip Enables (Input) ⁽⁷⁾
R/\overline{W}_L	R/\overline{W}_R	Read/Write Enable (Input)
\overline{OE}_L	\overline{OE}_R	Output Enable (Input)
A_{0L} - A_{17L} ⁽⁶⁾	A_{0R} - A_{17R} ⁽⁶⁾	Address (Input)
I/O_{0L} - I/O_{35L}	I/O_{0R} - I/O_{35R}	Data Input/Output
CLK_L	CLK_R	Clock (Input)
PL/\overline{FT}_L	PL/\overline{FT}_R	Pipeline/Flow-Through (Input)
\overline{ADS}_L	\overline{ADS}_R	Address Strobe Enable (Input)
\overline{CNTEN}_L	\overline{CNTEN}_R	Counter Enable (Input)
\overline{REPEAT}_L	\overline{REPEAT}_R	Counter Repeat ⁽³⁾
\overline{BE}_{0L} - \overline{BE}_{3L}	\overline{BE}_{0R} - \overline{BE}_{3R}	Byte Enables (9-bit bytes) (Input) ⁽⁷⁾
V_{DDQL}	V_{DDQR}	Power (I/O Bus) (3.3V or 2.5V) ⁽¹⁾ (Input)
OPT_L	OPT_R	Option for selecting V_{DDQX} ^(1,2) (Input)
ZZ_L	ZZ_R	Sleep Mode pin ⁽⁴⁾ (Input)
V_{DD}		Power (2.5V) ⁽¹⁾ (Input)
V_{SS}		Ground (0V) (Input)
TDI ⁽⁵⁾		Test Data Input
TDO ⁽⁵⁾		Test Data Output
TCK ⁽⁵⁾		Test Logic Clock (10MHz) (Input)
TMS ⁽⁵⁾		Test Mode Select (Input)
\overline{TRST} ⁽⁶⁾		Reset (Initialize TAP Controller) (Input)
\overline{INT}_L	\overline{INT}_R	Interrupt Flag (Output)
\overline{COL}_L	\overline{COL}_R	Collision Alert (Output)

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NOTES:

- V_{DD} , OPT_x , and V_{DDQX} must be set to appropriate operating levels prior to applying inputs on the I/Os and controls for that port.
- OPT_x selects the operating voltage levels for the I/Os and controls on that port. If OPT_x is set to V_{DD} (2.5V), then that port's I/Os and controls will operate at 3.3V levels and V_{DDQX} must be supplied at 3.3V. If OPT_x is set to V_{SS} (0V), then that port's I/Os and address controls will operate at 2.5V levels and V_{DDQX} must be supplied at 2.5V. The OPT pins are independent of one another—both ports can operate at 3.3V levels, both can operate at 2.5V levels, or either can operate at 3.3V with the other at 2.5V.
- When \overline{REPEAT}_x is asserted, the counter will reset to the last valid address loaded via \overline{ADS}_x .
- The sleep mode pin shuts off all dynamic inputs, except JTAG inputs, when asserted. All static inputs, i.e., PL/\overline{FT}_x and OPT_x and the sleep mode pins themselves (ZZ_x) are not affected during sleep mode. It is recommended that boundary scan not be operated during sleep mode.
- Due to limited pin count, JTAG is not supported in the DR-208 package.
- Address A_{17x} is a NC for the IDT70T3599. Also, Addresses A_{17x} and A_{16x} are NC's for the IDT 70T3589.
- Chip Enables and Byte Enables are double buffered when $PL/\overline{FT} = V_{IH}$, i.e., the signals take two cycles to deselect.

Truth Table I—Read/Write and Enable Control (1,2,3,4)

\overline{OE}	CLK	\overline{CE}_0	CE ₁	\overline{BE}_3	\overline{BE}_2	\overline{BE}_1	\overline{BE}_0	R/ \overline{W}	ZZ	Byte 3 I/O ₂₇₋₃₅	Byte 2 I/O ₁₈₋₂₆	Byte 1 I/O ₉₋₁₇	Byte 0 I/O ₀₋₈	MODE
X	↑	H	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	H	H	X	L	High-Z	High-Z	High-Z	High-Z	All Bytes Deselected
X	↑	L	H	H	H	H	L	L	L	High-Z	High-Z	High-Z	D _{IN}	Write to Byte 0 Only
X	↑	L	H	H	H	L	H	L	L	High-Z	High-Z	D _{IN}	High-Z	Write to Byte 1 Only
X	↑	L	H	H	L	H	H	L	L	High-Z	D _{IN}	High-Z	High-Z	Write to Byte 2 Only
X	↑	L	H	L	H	H	H	L	L	D _{IN}	High-Z	High-Z	High-Z	Write to Byte 3 Only
X	↑	L	H	H	H	L	L	L	L	High-Z	High-Z	D _{IN}	D _{IN}	Write to Lower 2 Bytes Only
X	↑	L	H	L	L	H	H	L	L	D _{IN}	D _{IN}	High-Z	High-Z	Write to Upper 2 bytes Only
X	↑	L	H	L	L	L	L	L	L	D _{IN}	D _{IN}	D _{IN}	D _{IN}	Write to All Bytes
L	↑	L	H	H	H	H	L	H	L	High-Z	High-Z	High-Z	D _{OUT}	Read Byte 0 Only
L	↑	L	H	H	H	L	H	H	L	High-Z	High-Z	D _{OUT}	High-Z	Read Byte 1 Only
L	↑	L	H	H	L	H	H	H	L	High-Z	D _{OUT}	High-Z	High-Z	Read Byte 2 Only
L	↑	L	H	L	H	H	H	H	L	D _{OUT}	High-Z	High-Z	High-Z	Read Byte 3 Only
L	↑	L	H	H	H	L	L	H	L	High-Z	High-Z	D _{OUT}	D _{OUT}	Read Lower 2 Bytes Only
L	↑	L	H	L	L	H	H	H	L	D _{OUT}	D _{OUT}	High-Z	High-Z	Read Upper 2 Bytes Only
L	↑	L	H	L	L	L	L	H	L	D _{OUT}	D _{OUT}	D _{OUT}	D _{OUT}	Read All Bytes
H	↑	X	X	X	X	X	X	X	L	High-Z	High-Z	High-Z	High-Z	Outputs Disabled
X	X	X	X	X	X	X	X	X	H	High-Z	High-Z	High-Z	High-Z	Sleep Mode

5666 tbl 02

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- \overline{ADS} , \overline{CNTEN} , \overline{REPEAT} = V_{IH}.
- \overline{OE} and ZZ are asynchronous input signals.
- It is possible to read or write any combination of bytes during a given access. A few representative samples have been illustrated here.

Truth Table II—Address Counter Control (1,2)

Address	Previous Internal Address	Internal Address Used	CLK	\overline{ADS}	\overline{CNTEN}	$\overline{REPEAT}^{(6)}$	I/O ⁽³⁾	MODE
An	X	An	↑	L ⁽⁴⁾	X	H	D _{I/O} (n)	External Address Used
X	An	An + 1	↑	H	L ⁽⁵⁾	H	D _{I/O} (n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	D _{I/O} (n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	An	↑	X	X	L ⁽⁴⁾	D _{I/O} (n)	Counter Set to last valid \overline{ADS} load

5666 tbl 03

NOTES:

- "H" = V_{IH}, "L" = V_{IL}, "X" = Don't Care.
- Read and write operations are controlled by the appropriate setting of R/ \overline{W} , \overline{CE}_0 , CE₁, \overline{BE}_n and \overline{OE} .
- Outputs configured in flow-through output mode: if outputs are in pipelined mode the data out will be delayed by one cycle.
- \overline{ADS} and \overline{REPEAT} are independent of all other memory control signals including \overline{CE}_0 , CE₁ and \overline{BE}_n .
- The address counter advances if \overline{CNTEN} = V_{IL} on the rising edge of CLK, regardless of all other memory control signals including \overline{CE}_0 , CE₁, \overline{BE}_n .
- When \overline{REPEAT} is asserted, the counter will reset to the last valid address loaded via \overline{ADS} . This value is not set at power-up: a known location should be loaded via \overline{ADS} during initialization if desired. Any subsequent \overline{ADS} access during operations will update the \overline{REPEAT} address location.

Recommended Operating Temperature and Supply Voltage ⁽¹⁾

Grade	Ambient Temperature	GND	V _{DD}
Commercial	0°C to +70°C	0V	2.5V \pm 100mV
Industrial	-40°C to +85°C	0V	2.5V \pm 100mV

5666 tbl 04

NOTES:

1. This is the parameter TA. This is the "instant on" case temperature.

Recommended DC Operating Conditions with V_{DDQ} at 2.5V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	2.4	2.5	2.6	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	2.4	2.5	2.6	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address, Control & Data I/O Inputs) ⁽³⁾	1.7	—	V _{DDQ} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG	1.7	—	V _{DD} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, OPT, PIPE/FT	V _{DD} - 0.2V	—	V _{DD} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.7	V
V _{IL}	Input Low Voltage - ZZ, OPT, PIPE/FT	-0.3 ⁽¹⁾	—	0.2	V

5666 tbl 05a

NOTES:

1. V_{IL} (min.) = -1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
3. To select operation at 2.5V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{SS}(0V), and V_{DDQX} for that port must be supplied as indicated above.

Recommended DC Operating Conditions with V_{DDQ} at 3.3V

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{DD}	Core Supply Voltage	2.4	2.5	2.6	V
V _{DDQ}	I/O Supply Voltage ⁽³⁾	3.15	3.3	3.45	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage (Address, Control & Data I/O Inputs) ⁽³⁾	2.0	—	V _{DDQ} + 150mV ⁽²⁾	V
V _{IH}	Input High Voltage - JTAG	1.7	—	V _{DD} + 100mV ⁽²⁾	V
V _{IH}	Input High Voltage - ZZ, OPT, PIPE/FT	V _{DD} - 0.2V	—	V _{DD} + 100mV ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.3 ⁽¹⁾	—	0.8	V
V _{IL}	Input Low Voltage - ZZ, OPT, PIPE/FT	-0.3 ⁽¹⁾	—	0.2	V

5666 tbl 05b

NOTES:

1. V_{IL} (min.) = -1.0V for pulse width less than tcyc/2, or 5ns, whichever is less.
2. V_{IH} (max.) = V_{DDQ} + 1.0V for pulse width less than tcyc/2 or 5ns, whichever is less.
3. To select operation at 3.3V levels on the I/Os and controls of a given port, the OPT pin for that port must be set to V_{DD} (2.5V), and V_{DDQX} for that port must be supplied as indicated above.

Absolute Maximum Ratings ⁽¹⁾

Symbol	Rating	Commercial & Industrial	Unit
V _{TERM} (V _{DD})	V _{DD} Terminal Voltage with Respect to GND	-0.5 to 3.6	V
V _{TERM} ⁽²⁾ (V _{DDQ})	V _{DDQ} Terminal Voltage with Respect to GND	-0.3 to V _{DDQ} + 0.3	V
V _{TERM} ⁽²⁾ (INPUTS and I/O's)	Input and I/O Terminal Voltage with Respect to GND	-0.3 to V _{DDQ} + 0.3	V
T _{BIAS} ⁽³⁾	Temperature Under Bias	-55 to +125	°C
T _{STG}	Storage Temperature	-65 to +150	°C
T _{JN}	Junction Temperature	+150	°C
I _{OUT} (For V _{DDQ} = 3.3V)	DC Output Current	50	mA
I _{OUT} (For V _{DDQ} = 2.5V)	DC Output Current	40	mA

5666 tbl 06

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- This is a steady-state DC parameter that applies after the power supply has reached its nominal operating value. Power sequencing is not necessary; however, the voltage on any Input or I/O pin cannot exceed V_{DDQ} during power supply ramp up.
- Ambient Temperature under DC Bias. No AC Conditions. Chip Deselected.

Capacitance ⁽¹⁾

(T_A = +25°C, F = 1.0MHz) PQFP ONLY

Symbol	Parameter	Conditions ⁽²⁾	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	8	pF
C _{OUT} ⁽³⁾	Output Capacitance	V _{OUT} = 3dV	10.5	pF

5666 tbl 07

NOTES:

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C_{OUT} also references C_{I/O}.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 2.5V ± 100mV)

Symbol	Parameter	Test Conditions	70T3519/99/89S		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current ⁽¹⁾	V _{DDQ} = Max., V _{IN} = 0V to V _{DDQ}	—	10	μA
I _{LI}	JTAG & ZZ Input Leakage Current ^(1,2)	V _{DD} = Max., V _{IN} = 0V to V _{DD}	—	±30	μA
I _{LO}	Output Leakage Current ^(1,3)	$\overline{CE}_0 = V_{IH}$ or $CE_1 = V_{IL}$, V _{OUT} = 0V to V _{DDQ}	—	10	μA
V _{OL} (3.3V)	Output Low Voltage ⁽¹⁾	I _{OL} = +4mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (3.3V)	Output High Voltage ⁽¹⁾	I _{OH} = -4mA, V _{DDQ} = Min.	2.4	—	V
V _{OL} (2.5V)	Output Low Voltage ⁽¹⁾	I _{OL} = +2mA, V _{DDQ} = Min.	—	0.4	V
V _{OH} (2.5V)	Output High Voltage ⁽¹⁾	I _{OH} = -2mA, V _{DDQ} = Min.	2.0	—	V

5666 tbl 08

NOTES:

- V_{DDQ} is selectable (3.3V/2.5V) via OPT pins. Refer to p.5 for details.
- Applicable only for TMS, TDI and TRST inputs.
- Outputs tested in tri-state mode.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ⁽³⁾ ($V_{DD} = 2.5V \pm 100mV$)

Symbol	Parameter	Test Condition	Version	70T3519/99/89 S200 Com'l Only ⁽⁸⁾		70T3519/99/89 S166 Com'l & Ind ⁽⁷⁾		70T3519/99/89 S133 Com'l & Ind		Unit	
				Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.	Typ. ⁽⁴⁾	Max.		
IDD	Dynamic Operating Current (Both Ports Active)	\overline{CE}_L and $\overline{CE}_R = V_{IL}$, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	375	525	320	450	260	370	mA
			IND	S	—	—	320	510	260	450	
ISB1 ⁽⁶⁾	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	205	270	175	230	140	190	mA
			IND	S	—	—	175	275	140	235	
ISB2 ⁽⁶⁾	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^A = V_{IL}$ and $\overline{CE}^B = V_{IH}^{(9)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	300	375	250	325	200	250	mA
			IND	S	—	—	250	365	200	310	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports \overline{CE}_L and $\overline{CE}_R = V_{DDQ} - 0.2V$, $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(2)}$	COM'L	S	5	15	5	15	5	15	mA
			IND	S	—	—	5	20	5	20	
ISB4 ⁽⁶⁾	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^A \leq 0.2V$ and $\overline{CE}^B \geq V_{DDQ} - 0.2V^{(5)}$ $V_{IN} \geq V_{DDQ} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L	S	300	375	250	325	200	250	mA
			IND	S	—	—	250	365	200	310	
Izz	Sleep Mode Current (Both Ports - TTL Level Inputs)	$ZZ_L = ZZ_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L	S	5	15	5	15	5	15	mA
			IND	S	—	—	5	20	5	20	

5666 tbl 09

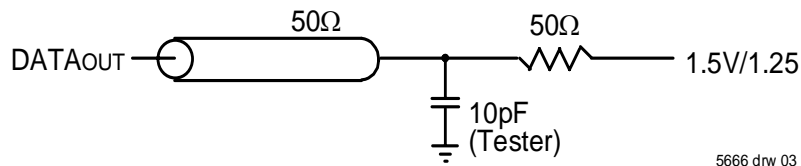
NOTES:

- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of $1/t_{cyc}$, using "AC TEST CONDITIONS".
- $f = 0$ means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 2.5V$, $T_A = 25^\circ C$ for Typ, and are not production tested. $I_{DD}(f=0) = 15mA$ (Typ).
- $\overline{CE}_X = V_{IL}$ means $\overline{CE}_{0X} = V_{IL}$ and $CE_{1X} = V_{IH}$
 $\overline{CE}_X = V_{IH}$ means $\overline{CE}_{0X} = V_{IH}$ or $CE_{1X} = V_{IL}$
 $\overline{CE}_X \leq 0.2V$ means $\overline{CE}_{0X} \leq 0.2V$ and $CE_{1X} \geq V_{DD} - 0.2V$
 $\overline{CE}_X \geq V_{DD} - 0.2V$ means $\overline{CE}_{0X} \geq V_{DD} - 0.2V$ or $CE_{1X} \leq 0.2V$
"X" represents "L" for left port or "R" for right port.
- ISB1, ISB2 and ISB4 will all reach full standby levels (ISB3) on the appropriate port(s) if ZZ_L and/or $ZZ_R = V_{IH}$.
- 166MHz I-Temp is not available in the BF-208 package.
- 200Mhz is not available in the BF-208 and DR-208 packages.

AC Test Conditions (V_{DDQ} - 3.3V/2.5V)

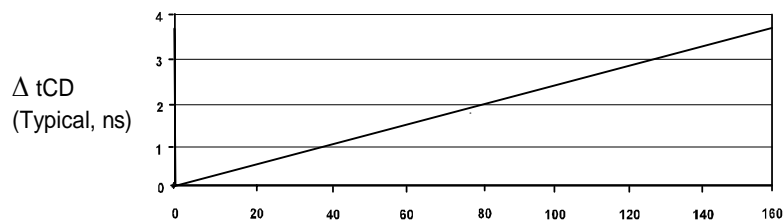
Input Pulse Levels (Address & Controls)	GND to 3.0V/GND to 2.4V
Input Pulse Levels (I/Os)	GND to 3.0V/GND to 2.4V
Input Rise/Fall Times	2ns
Input Timing Reference Levels	1.5V/1.25V
Output Reference Levels	1.5V/1.25V
Output Load	Figure 1

5666 tbl 10



5666 drw 03

Figure 1. AC Output Test load.



Δ Capacitance (pF) from AC Test Load

5666 drw 04

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing) ^(2,3) ($V_{DD} = 2.5V \pm 100mV$, $T_A = 0^\circ C$ to $+70^\circ C$)

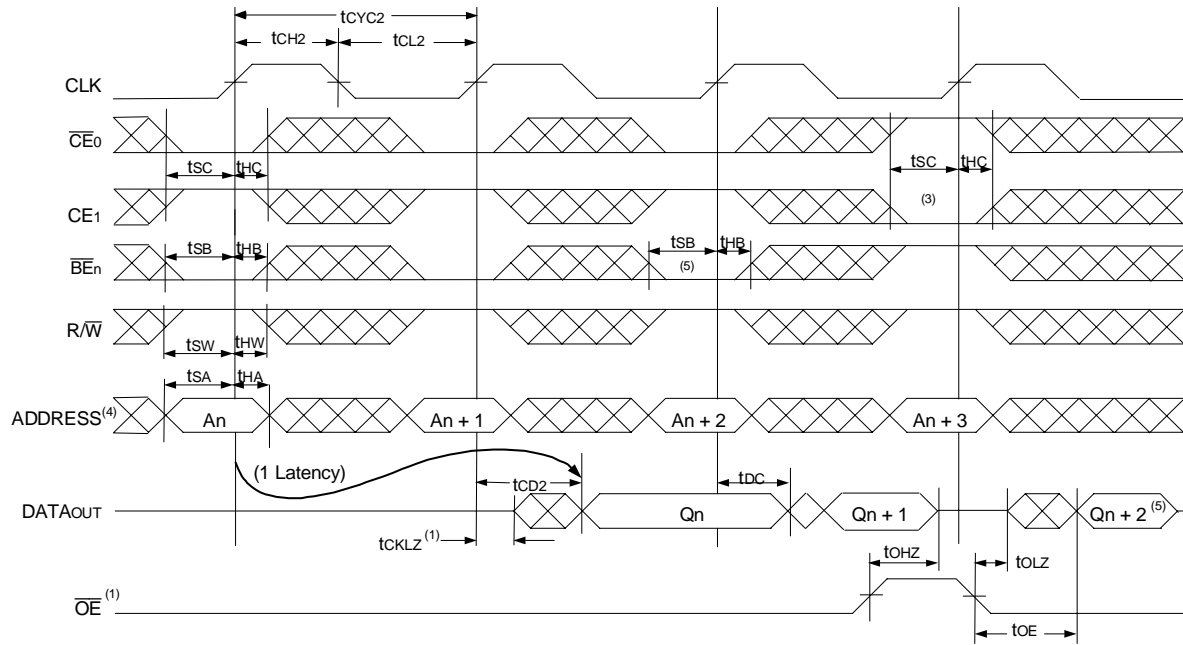
Symbol	Parameter	70T3519/99/89 S200 Com'l Only ⁽⁵⁾		70T3519/99/89 S166 Com'l & Ind ⁽⁴⁾		70T3519/99/89 S133 Com'l & Ind		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t _{CYC1}	Clock Cycle Time (Flow-Through) ⁽¹⁾	15	—	20	—	25	—	ns
t _{CYC2}	Clock Cycle Time (Pipelined) ⁽¹⁾	5	—	6	—	7.5	—	ns
t _{CH1}	Clock High Time (Flow-Through) ⁽¹⁾	6	—	8	—	10	—	ns
t _{CL1}	Clock Low Time (Flow-Through) ⁽¹⁾	6	—	8	—	10	—	ns
t _{CH2}	Clock High Time (Pipelined) ⁽²⁾	2	—	2.4	—	3	—	ns
t _{CL2}	Clock Low Time (Pipelined) ⁽¹⁾	2	—	2.4	—	3	—	ns
t _{SA}	Address Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HA}	Address Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SC}	Chip Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HC}	Chip Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SB}	Byte Enable Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HB}	Byte Enable Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SW}	R/W Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HW}	R/W Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SD}	Input Data Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HD}	Input Data Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SAD}	\overline{ADS} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HAD}	\overline{ADS} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SCN}	\overline{CNTEN} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HCN}	\overline{CNTEN} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{SRPT}	\overline{REPEAT} Setup Time	1.5	—	1.7	—	1.8	—	ns
t _{HRPT}	\overline{REPEAT} Hold Time	0.5	—	0.5	—	0.5	—	ns
t _{OE}	Output Enable to Data Valid	—	4.4	—	4.4	—	4.6	ns
t _{OLZ} ⁽⁶⁾	Output Enable to Output Low-Z	1	—	1	—	1	—	ns
t _{OHZ} ⁽⁶⁾	Output Enable to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CD1}	Clock to Data Valid (Flow-Through) ⁽¹⁾	—	10	—	12	—	15	ns
t _{CD2}	Clock to Data Valid (Pipelined) ⁽¹⁾	—	3.4	—	3.6	—	4.2	ns
t _{DC}	Data Output Hold After Clock High	1	—	1	—	1	—	ns
t _{CKHZ} ⁽⁶⁾	Clock High to Output High-Z	1	3.4	1	3.6	1	4.2	ns
t _{CKLZ} ⁽⁶⁾	Clock High to Output Low-Z	1	—	1	—	1	—	ns
t _{INS}	Interrupt Flag Set Time	—	7	—	7	—	7	ns
t _{INR}	Interrupt Flag Reset Time	—	7	—	7	—	7	ns
t _{COLS}	Collision Flag Set Time	—	3.4	—	3.6	—	4.2	ns
t _{COLR}	Collision Flag Reset Time	—	3.4	—	3.6	—	4.2	ns
t _{ZZSC}	Sleep Mode Set Cycles	2	—	2	—	2	—	cycles
t _{ZZRC}	Sleep Mode Recovery Cycles	3	—	3	—	3	—	cycles
Port-to-Port Delay								
t _{CO}	Clock-to-Clock Offset	4	—	5	—	6	—	ns
t _{OFs}	Clock-to-Clock Offset for Collision Detection	Please refer to Collision Detection Timing Table on Page 21						

NOTES:

5666 tbl 11

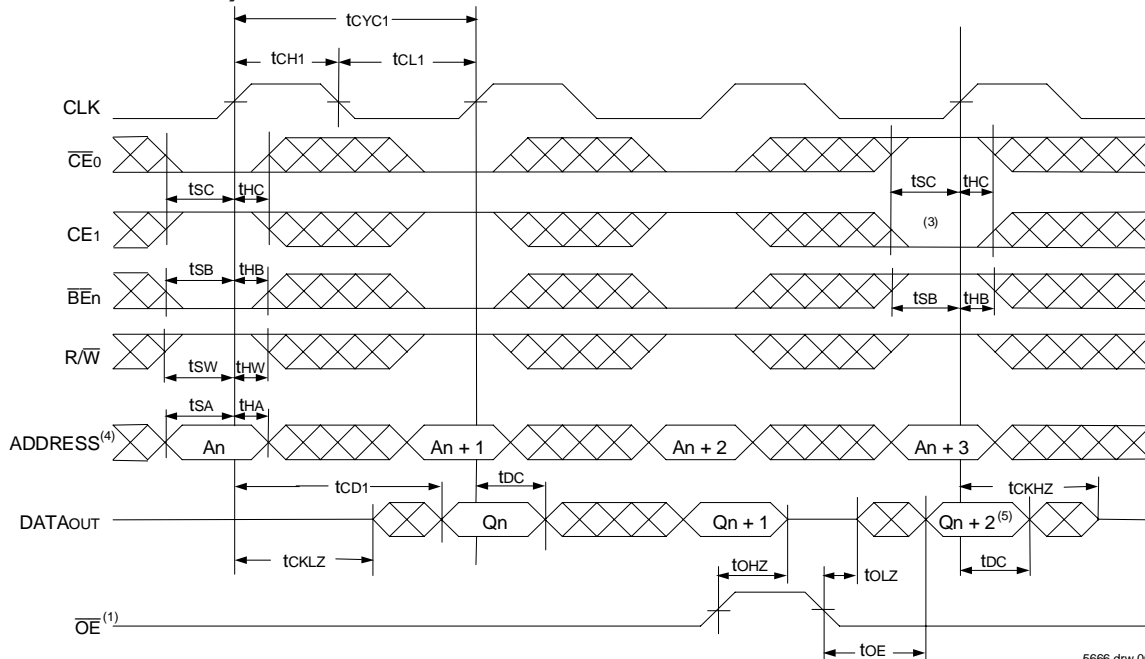
- The Pipelined output parameters (t_{CYC2}, t_{CD2}) apply to either or both left and right ports when $\overline{FT}/PIPEx = V_{DD}$ (2.5V). Flow-through parameters (t_{CYC1}, t_{CD1}) apply when $\overline{FT}/PIPE = V_{SS}$ (0V) for that port.
- All input signals are synchronous with respect to the clock except for the asynchronous Output Enable (\overline{OE}), $\overline{FT}/PIPE$ and OPT. $\overline{FT}/PIPE$ and OPT should be treated as DC signals, i.e. steady state during operation.
- These values are valid for either level of V_{DDQ} (3.3V/2.5V). See page 6 for details on selecting the desired operating voltage levels for each port.
- 166MHz I-Temp is not available in the BF-208 package.
- 200Mhz is not available in the BF-208 and DR-208 packages.
- Guaranteed by design (not production tested).

Timing Waveform of Read Cycle for Pipelined Operation ($\overline{FT}/\text{PIPE}^*x = V_{IH}$)(1,2)



5666 drw 05

Timing Waveform of Read Cycle for Flow-through Output ($\overline{FT}/\text{PIPE}^*x = V_{IL}$)(1,2,6)

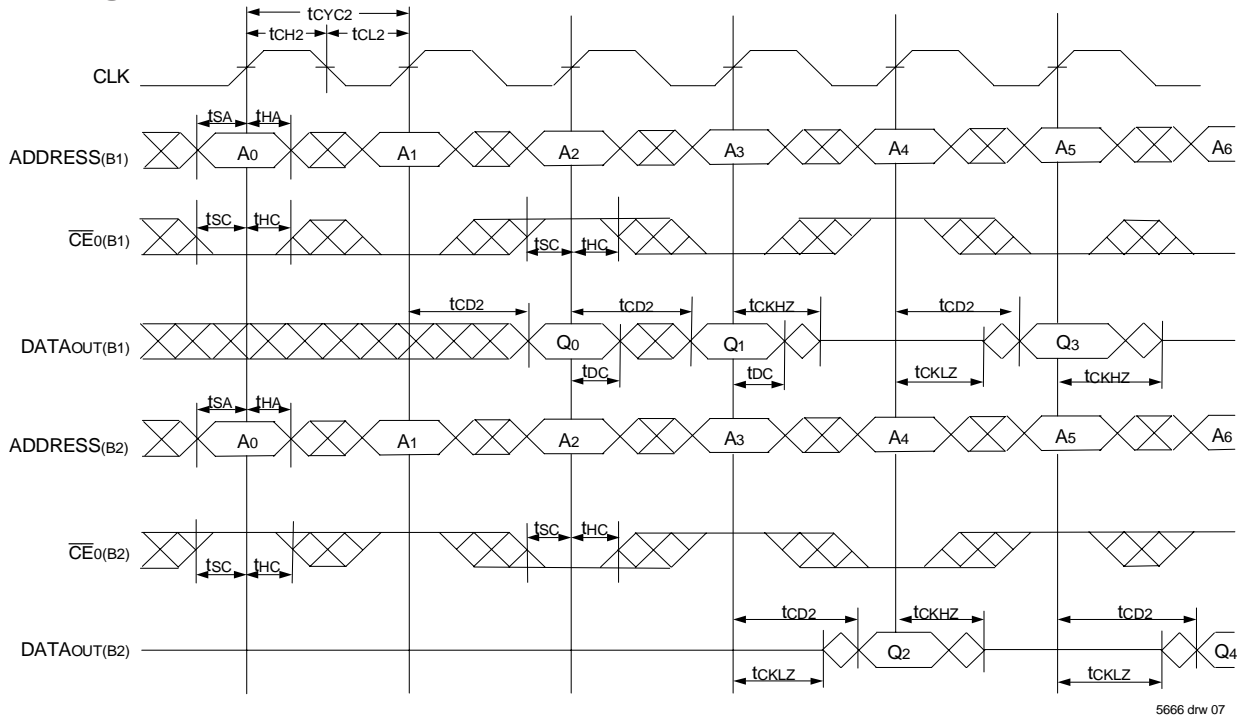


5666 drw 06

NOTES:

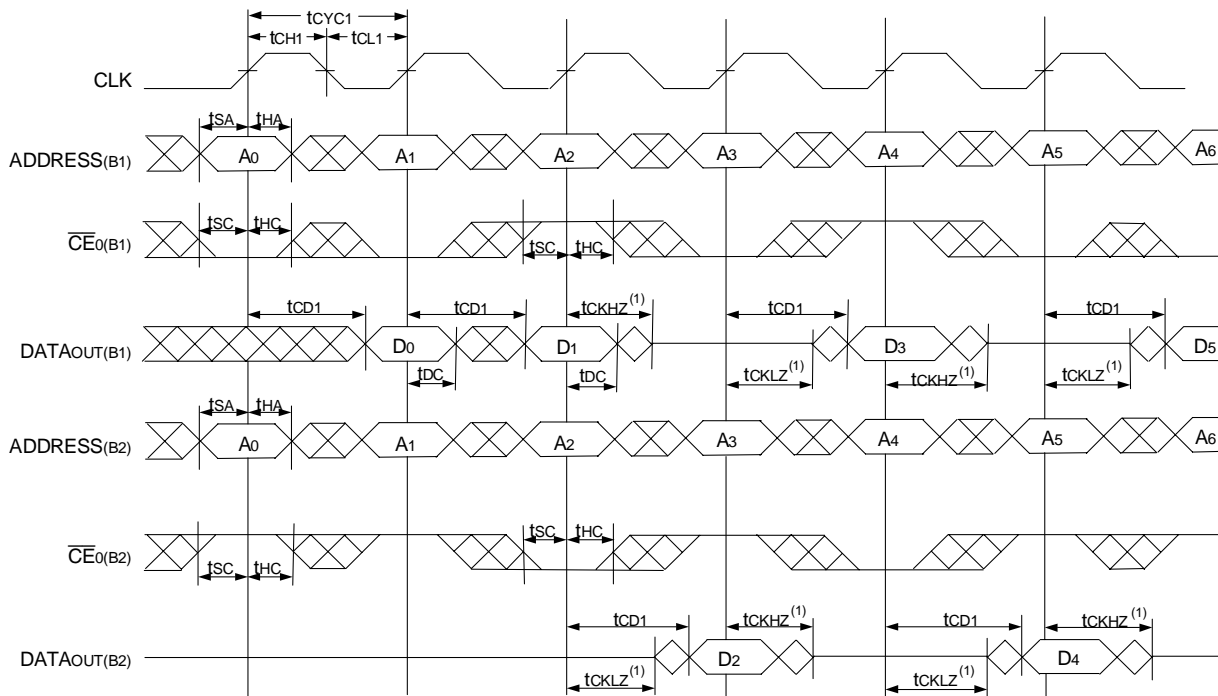
- \overline{OE} is asynchronously controlled; all other inputs depicted in the above waveforms are synchronous to the rising clock edge.
- $\overline{ADS} = V_{IL}$, \overline{CNTEN} and $\overline{REPEAT} = V_{IH}$.
- The output is disabled (High-Impedance state) by $\overline{CE}_0 = V_{IH}$, $\overline{CE}_1 = V_{IL}$, $\overline{BE}_n = V_{IH}$ following the next rising edge of the clock. Refer to Truth Table 1.
- Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
- If \overline{BE}_n was HIGH, then the appropriate Byte of DATAout for Q_{n+2} would be disabled (High-Impedance state).
- "x" denotes Left or Right port. The diagram is with respect to that port.

Timing Waveform of a Multi-Device Pipelined Read (1,2)



5666 drw 07

Timing Waveform of a Multi-Device Flow-Through Read (1,2)

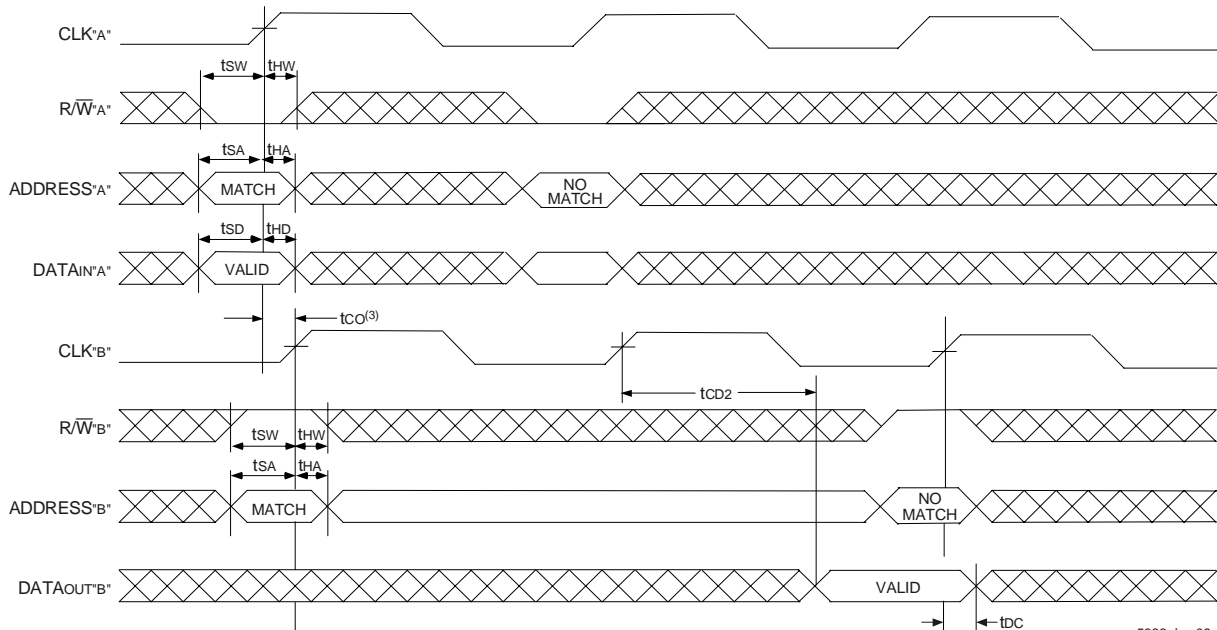


5666 drw 08

NOTES:

1. B1 Represents Device #1; B2 Represents Device #2. Each Device consists of one IDT70T3519/99/89 for this waveform, and are setup for depth expansion in this example. ADDRESS(B1) = ADDRESS(B2) in this situation.
2. BE_n, OE, and ADS = VIH; CE1(B1), CE1(B2), R/W, CNTEN, and REPEAT = VIH.

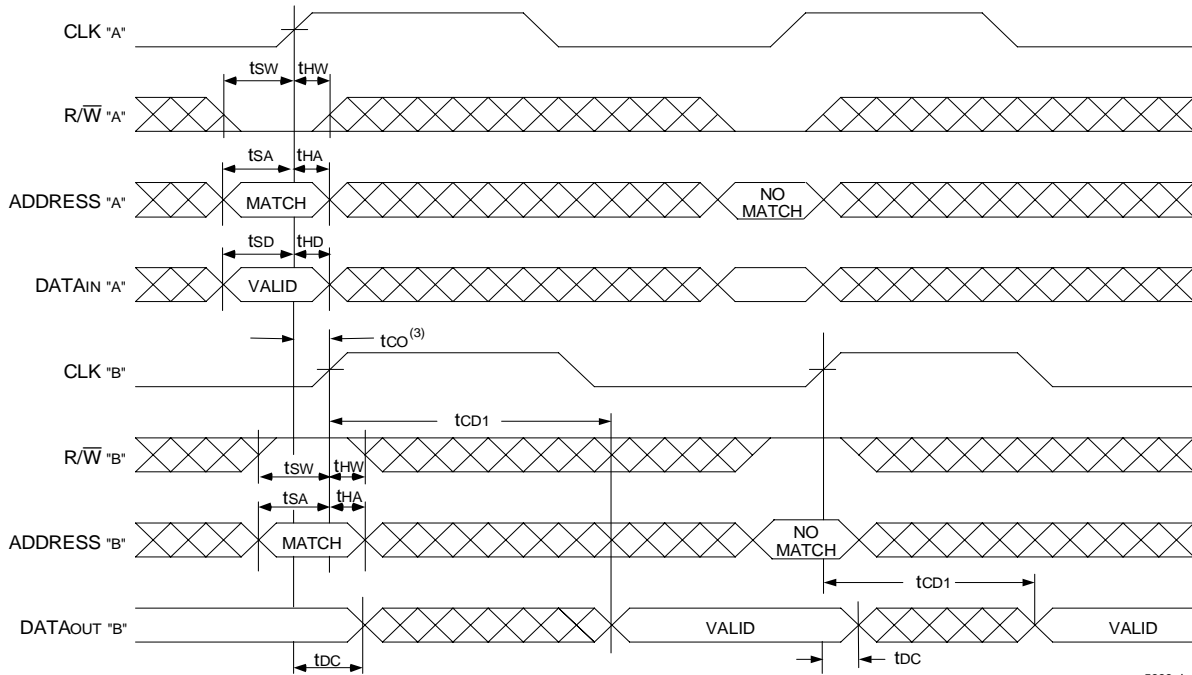
Timing Waveform of Left Port Write to Pipelined Right Port Read (1,2,4)



NOTES:

1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS} = V_{IL}$; $\overline{CE_1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for Port "B", which is being read from. $\overline{OE} = V_{IH}$ for Port "A", which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + 2 t_{CYC2} + t_{CD2}$). If $t_{CO} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (ie, time from write to valid read on opposite port will be $t_{CO} + t_{CYC2} + t_{CD2}$).
4. All timing is the same for Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite of Port "A"

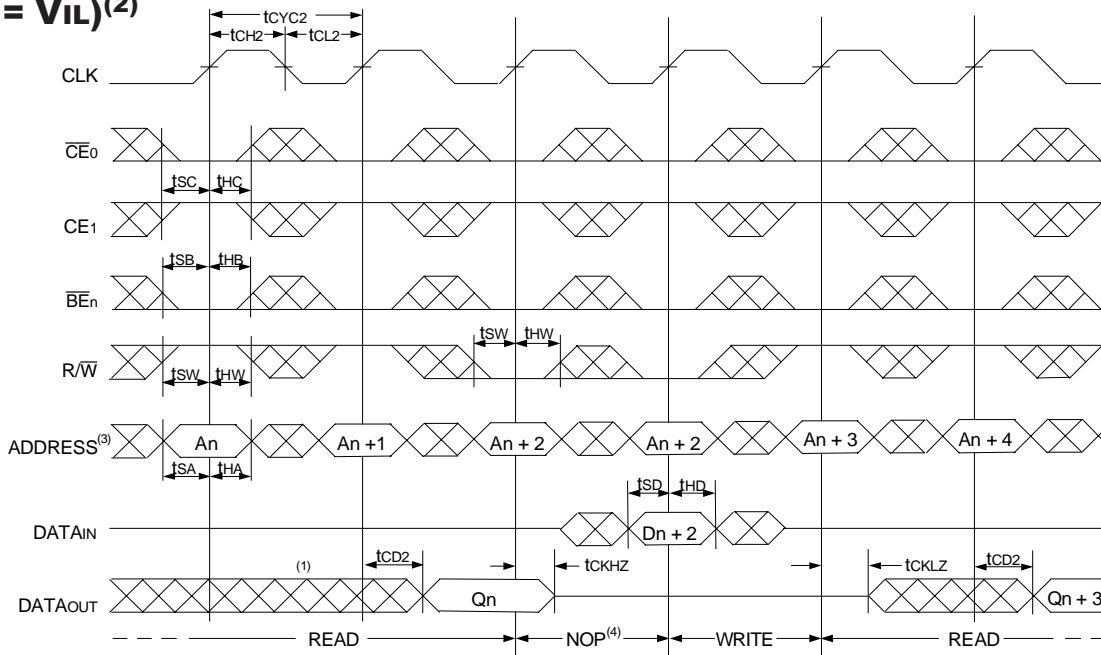
Timing Waveform with Port-to-Port Flow-Through Read (1,2,4)



NOTES:

1. $\overline{CE_0}$, $\overline{BE_n}$, and $\overline{ADS} = V_{IL}$; $\overline{CE_1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
2. $\overline{OE} = V_{IL}$ for the Right Port, which is being read from. $\overline{OE} = V_{IH}$ for the Left Port, which is being written to.
3. If $t_{CO} \leq$ minimum specified, then data from Port "B" read is not valid until following Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CYC} + t_{CD1}$). If $t_{CO} >$ minimum, then data from Port "B" read is available on first Port "B" clock cycle (i.e., time from write to valid read on opposite port will be $t_{CO} + t_{CD1}$).
4. All timing is the same for both left and right ports. Port "A" may be either left or right port. Port "B" is the opposite of Port "A".

Timing Waveform of Pipelined Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾

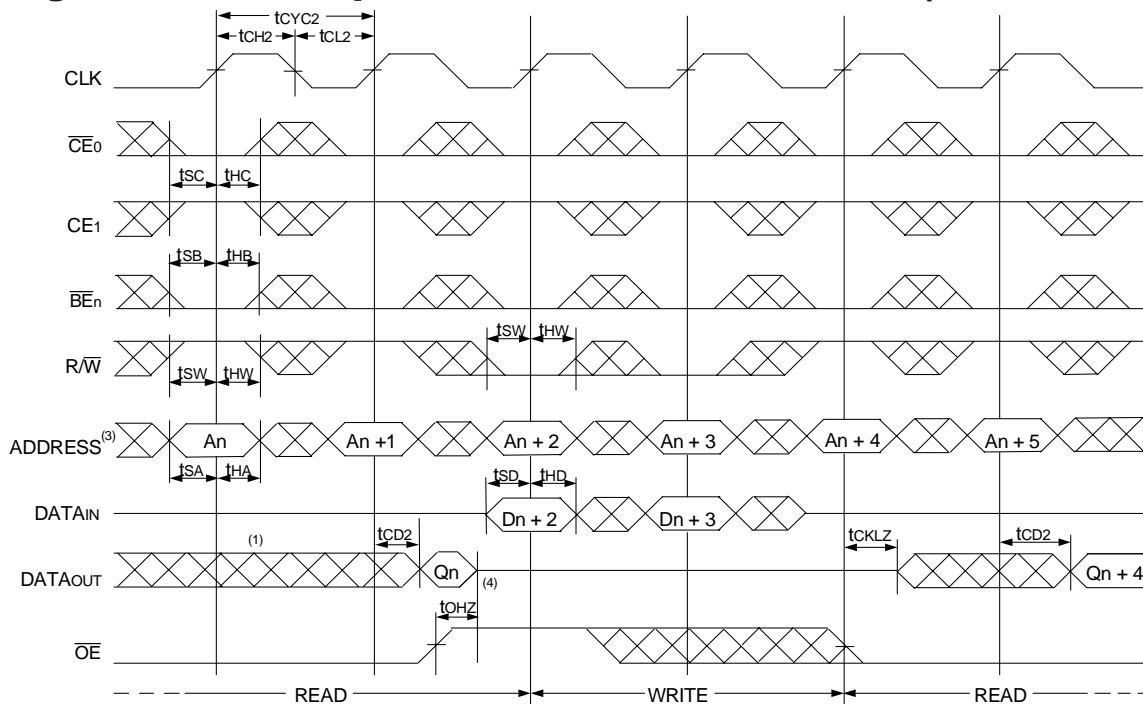


NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $REPEAT = V_{IH}$. "NOP" is "No Operation".
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

5666 drw 11

Timing Waveform of Pipelined Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾

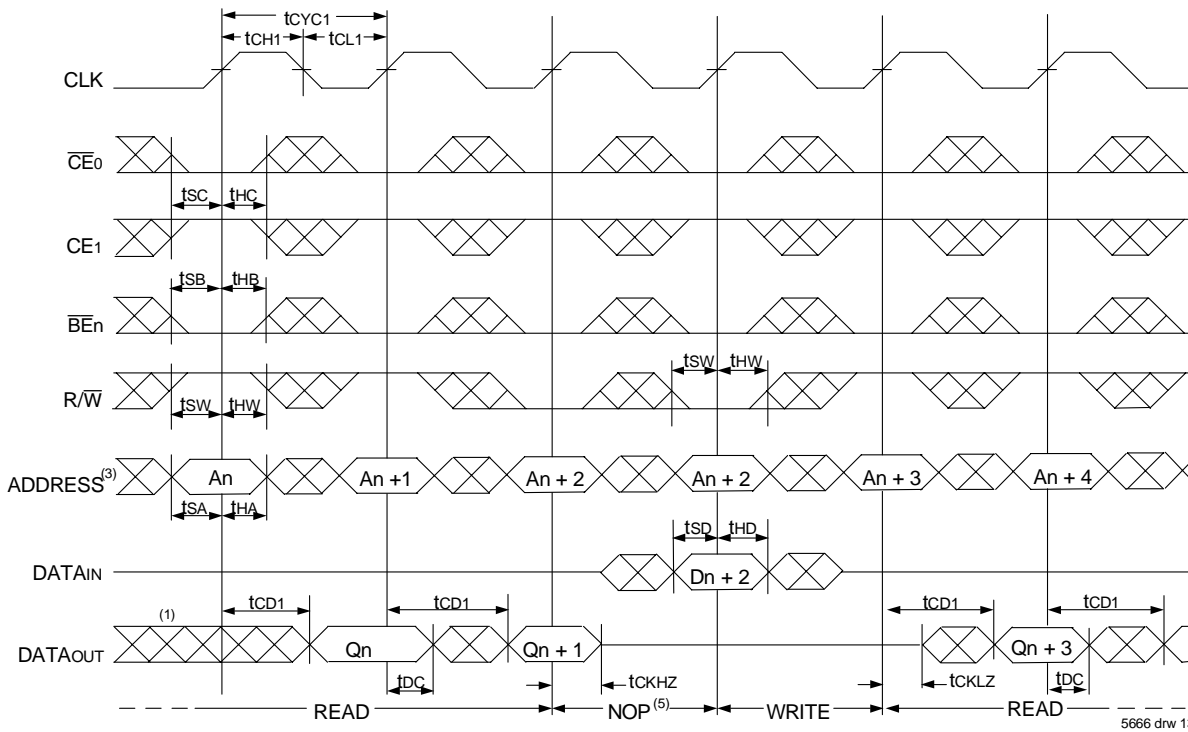


NOTES:

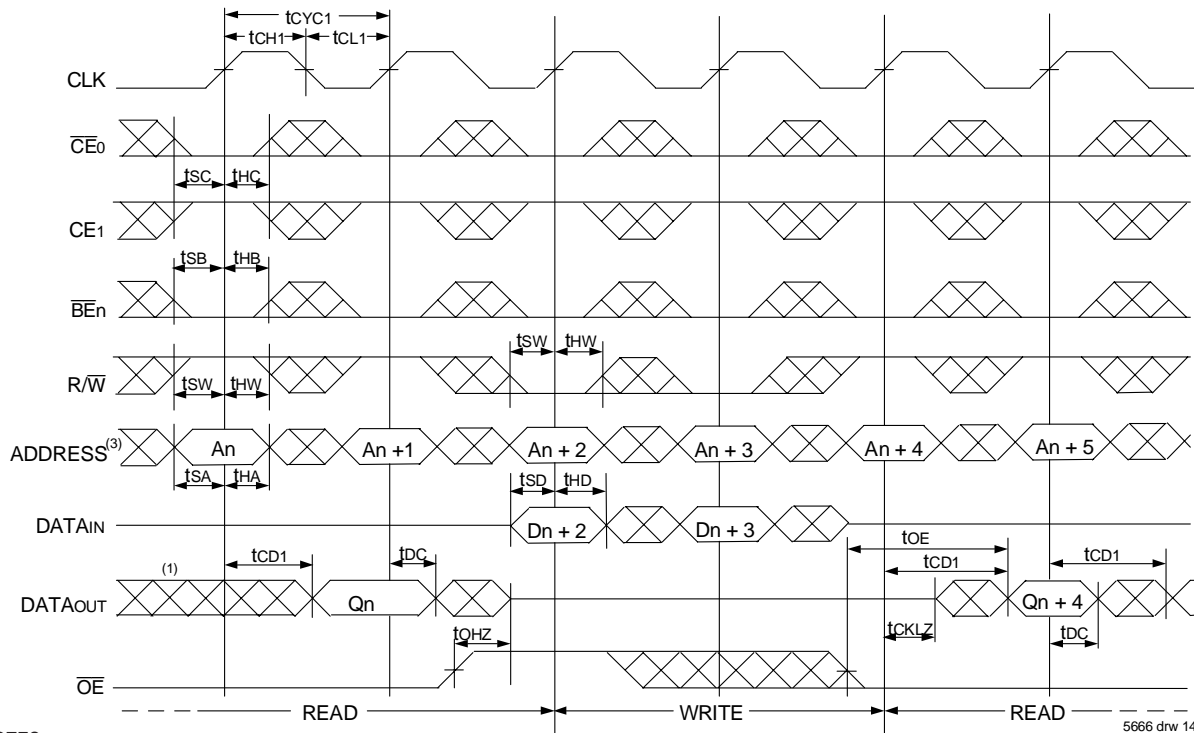
1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. \overline{CE}_0 , \overline{BE}_n , and $\overline{ADS} = V_{IL}$; CE_1 , $CNTEN$, and $REPEAT = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. This timing does not meet requirements for fastest speed grade. This waveform indicates how logically it could be done if timing so allows.

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Timing Waveform of Flow-Through Read-to-Write-to-Read ($\overline{OE} = V_{IL}$)⁽²⁾



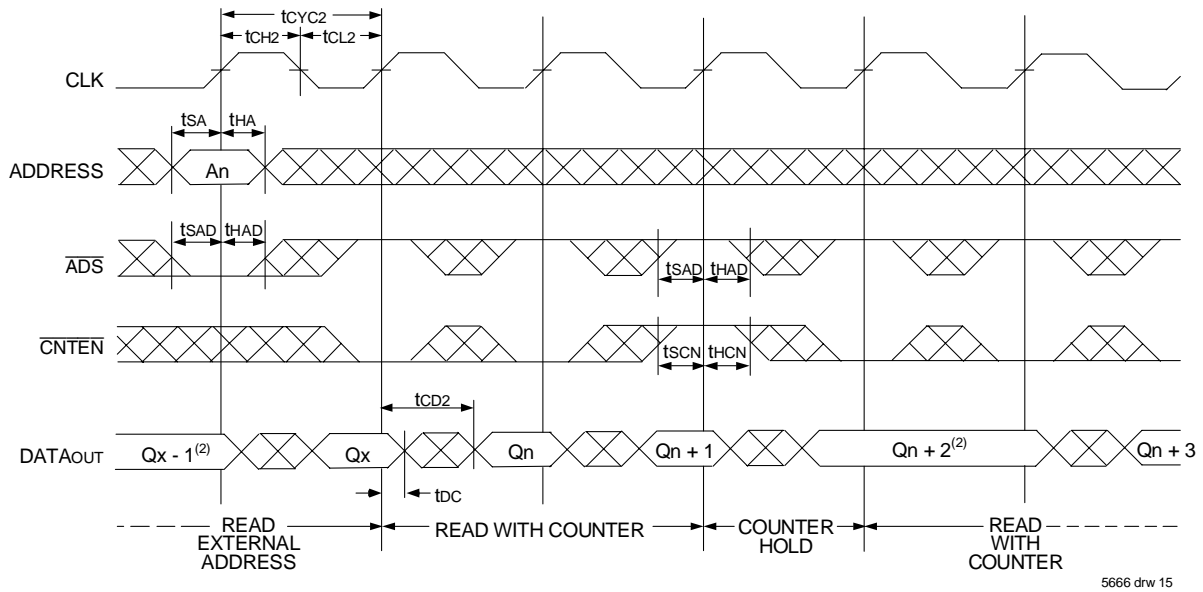
Timing Waveform of Flow-Through Read-to-Write-to-Read (\overline{OE} Controlled)⁽²⁾



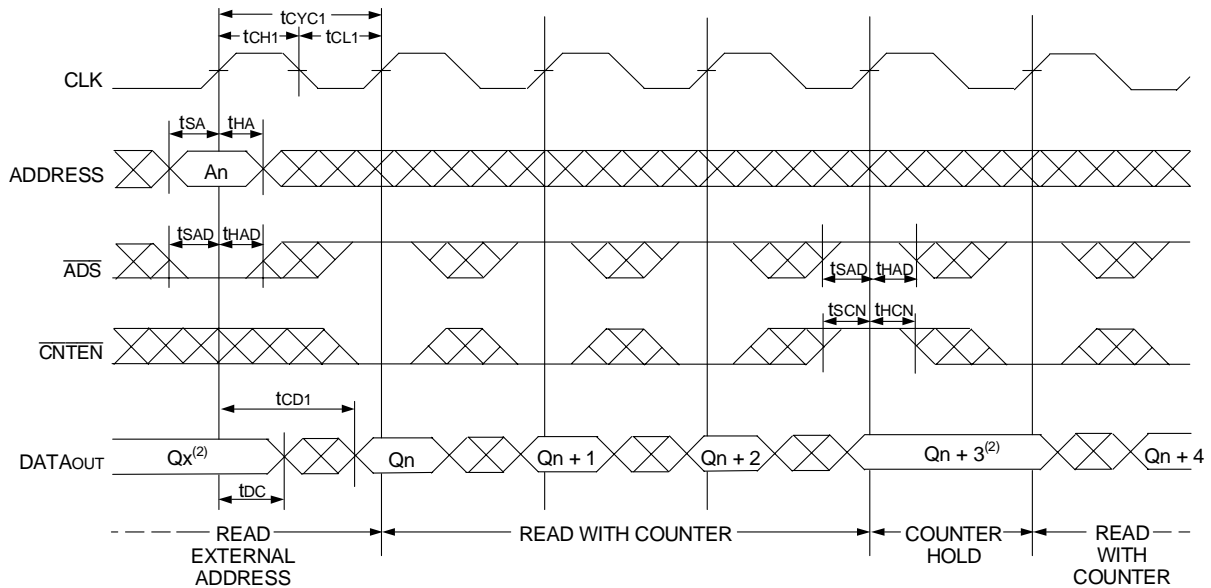
NOTES:

1. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
2. $\overline{CE0}$, \overline{BEn} , and $\overline{ADS} = V_{IL}$; $\overline{CE1}$, \overline{CNTEN} , and $\overline{REPEAT} = V_{IH}$.
3. Addresses do not have to be accessed sequentially since $\overline{ADS} = V_{IL}$ constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
4. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

Timing Waveform of Pipelined Read with Address Counter Advance (1)



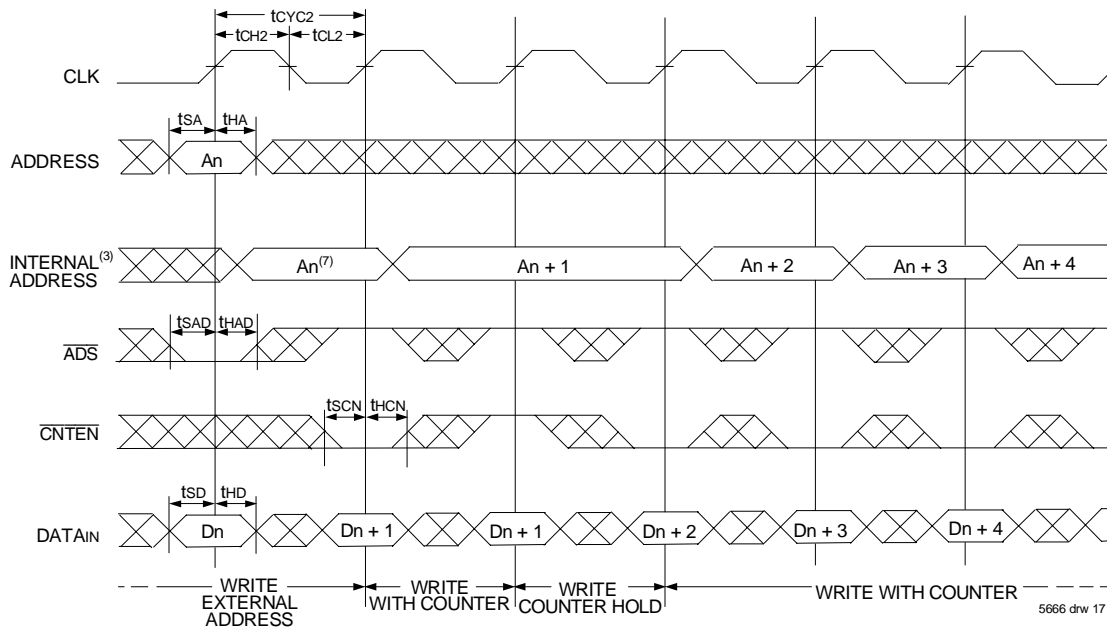
Timing Waveform of Flow-Through Read with Address Counter Advance (1)



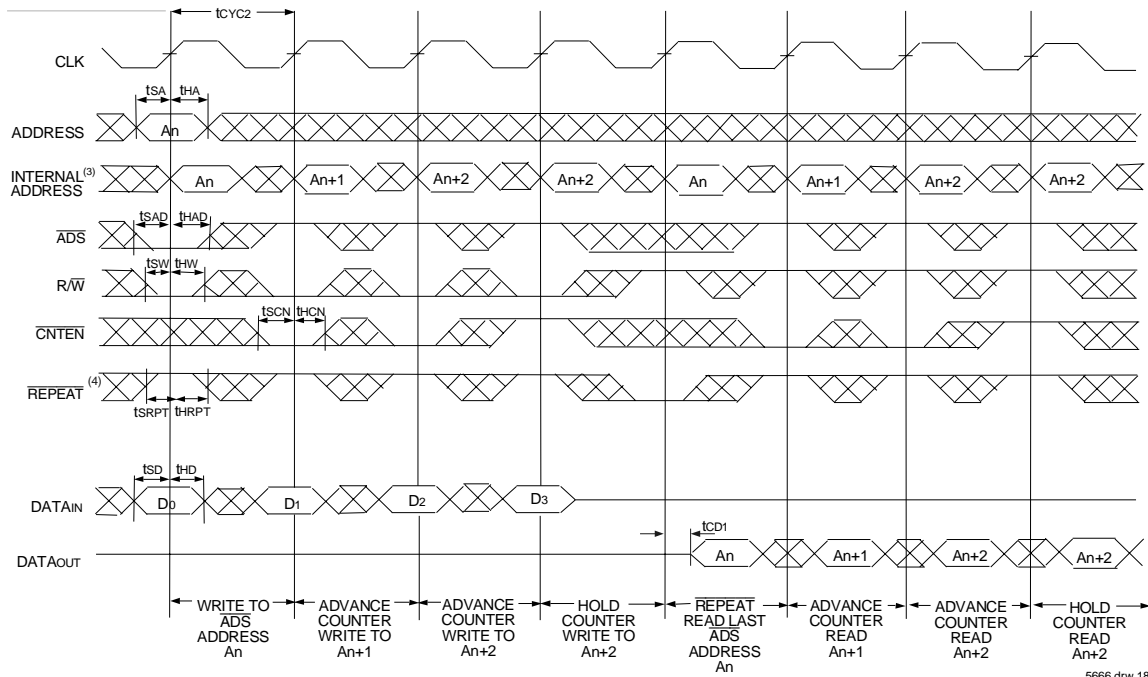
NOTES:

1. \overline{CE}_0 , \overline{OE} , $\overline{BE}_n = V_{IL}$; \overline{CE}_1 , R/\overline{W} , and $\overline{REPEAT} = V_{IH}$.
2. If there is no address change via $\overline{ADS} = V_{IL}$ (loading a new address) or $\overline{CNTEN} = V_{IL}$ (advancing the address), i.e. $\overline{ADS} = V_{IH}$ and $\overline{CNTEN} = V_{IH}$, then the data output remains constant for subsequent clocks.

Timing Waveform of Write with Address Counter Advance (Flow-through or Pipelined Inputs) (1)



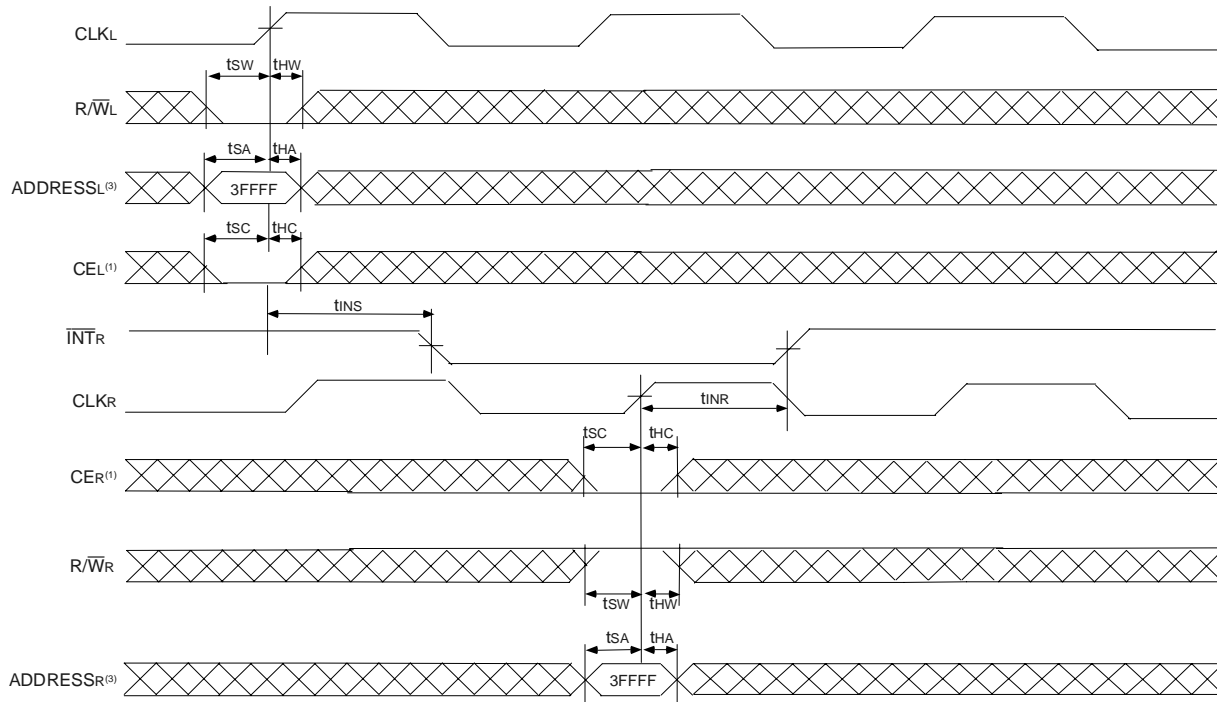
Timing Waveform of Counter Repeat (2,6)



NOTES:

1. \overline{CE}_0 , \overline{BE}_n , and $R/\overline{W} = V_{IL}$; CE_1 and $\overline{REPEAT} = V_{IH}$.
2. \overline{CE}_0 , $\overline{BE}_n = V_{IL}$; $CE_1 = V_{IH}$.
3. The "Internal Address" is equal to the "External Address" when $\overline{ADS} = V_{IL}$ and equals the counter output when $\overline{ADS} = V_{IH}$.
4. No dead cycle exists during REPEAT operation. A READ or WRITE cycle may be coincidental with the counter REPEAT cycle: Address loaded by last valid \overline{ADS} load will be accessed. For more information on REPEAT function refer to Truth Table II.
5. $\overline{CNTEN} = V_{IL}$ advances Internal Address from 'An' to 'An +1'. The transition shown indicates the time required for the counter to advance. The 'An +1' Address is written to during this cycle.
6. For Pipelined Mode user should add 1 cycle latency for outputs as per timing waveform of read cycle for pipelined operations.

Waveform of Interrupt Timing (2)



NOTES:

1. CE0 = VIL and CE1 = VIH
2. All timing is the same for Left and Right ports.
3. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

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Truth Table III — Interrupt Flag (1)

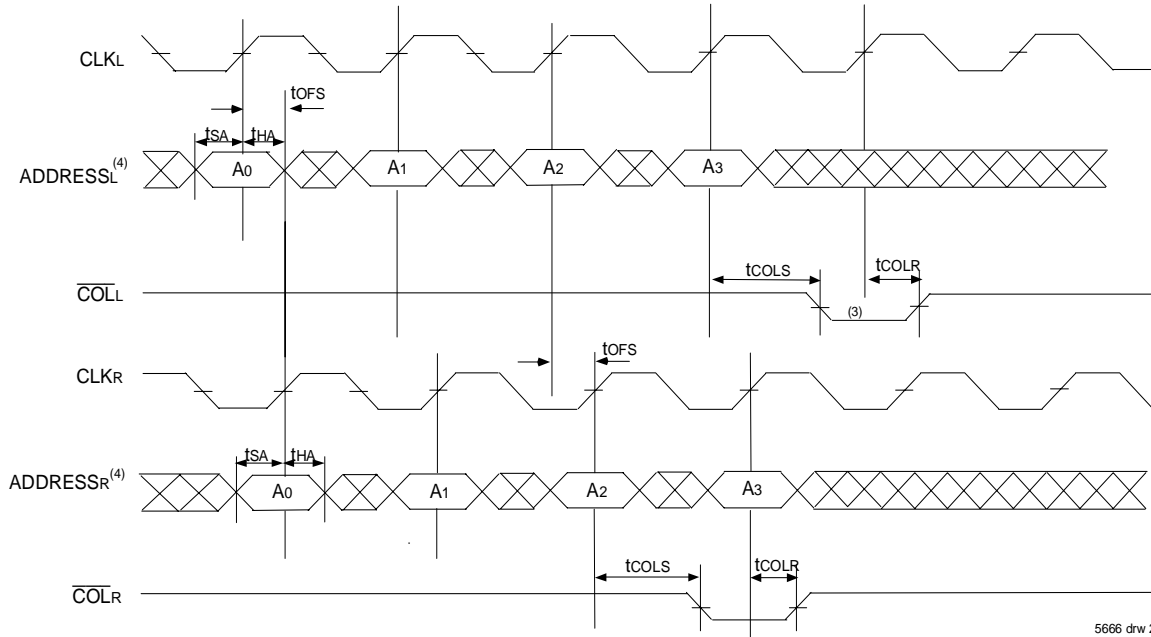
Left Port					Right Port					Function
CLKL	R/WL ⁽²⁾	CEL ⁽²⁾	A17L-A0L ^(3,4,5)	INTL	CLKR	R/WR ⁽²⁾	CER ⁽²⁾	A17R-A0R ^(3,4,5)	INTR	
↑	L	L	3FFFF	X	↑	X	X	X	L	Set Right INTR Flag
↑	X	X	X	X	↑	H	L	3FFFF	H	Reset Right INTR Flag
↑	X	X	X	L	↑	L	L	3FFFE	X	Set Left INTL Flag
↑	H	L	3FFFE	H	↑	X	X	X	X	Reset Left INTL Flag

NOTES:

1. INTL and INTR must be initialized at power-up by Resetting the flags.
2. CE0 = VIL and CE1 = VIH. R/W and CE are synchronous with respect to the clock and need valid set-up and hold times.
3. A17x is a NC for IDT70T3599, therefore Interrupt Addresses are 1FFFF and 1FFFE.
4. A17x and A16x are NC's for IDT70T3589, therefore Interrupt Addresses are FFFF and FFFE.
5. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

5666 tbl 12

Waveform of Collision Timing^(1,2) Both Ports Writing with Left Port Clock Leading



NOTES:

1. $\overline{CE}_0 = V_{IL}$, $CE_1 = V_{IH}$.
2. For reading port, \overline{OE} is a Don't care on the Collision Detection Logic. Please refer to Truth Table IV for specific cases.
3. Leading Port Output flag might output $3t_{OFS} + t_{COLS}$ after Address match.
4. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

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Collision Detection Timing^(3,4)

Cycle Time	t _{OFS} (ns)	
	Region 1 (ns) ⁽¹⁾	Region 2 (ns) ⁽²⁾
5ns	0 - 2.8	2.81 - 4.6
6ns	0 - 3.8	3.81 - 5.6
7.5ns	0 - 5.3	5.31 - 7.1

5666 tbl 13

NOTES:

1. **Region 1**
Both ports show collision after 2nd cycle for Addresses 0, 2, 4 etc.
2. **Region 2**
Leading port shows collision after 3rd cycle for addresses 0, 3, 6, etc. while trailing port shows collision after 2nd cycle for addresses 0, 2, 4 etc.
3. All the production units are tested to midpoint of each region.
4. These ranges are based on characterization of a typical device.

Truth Table IV — Collision Detection Flag

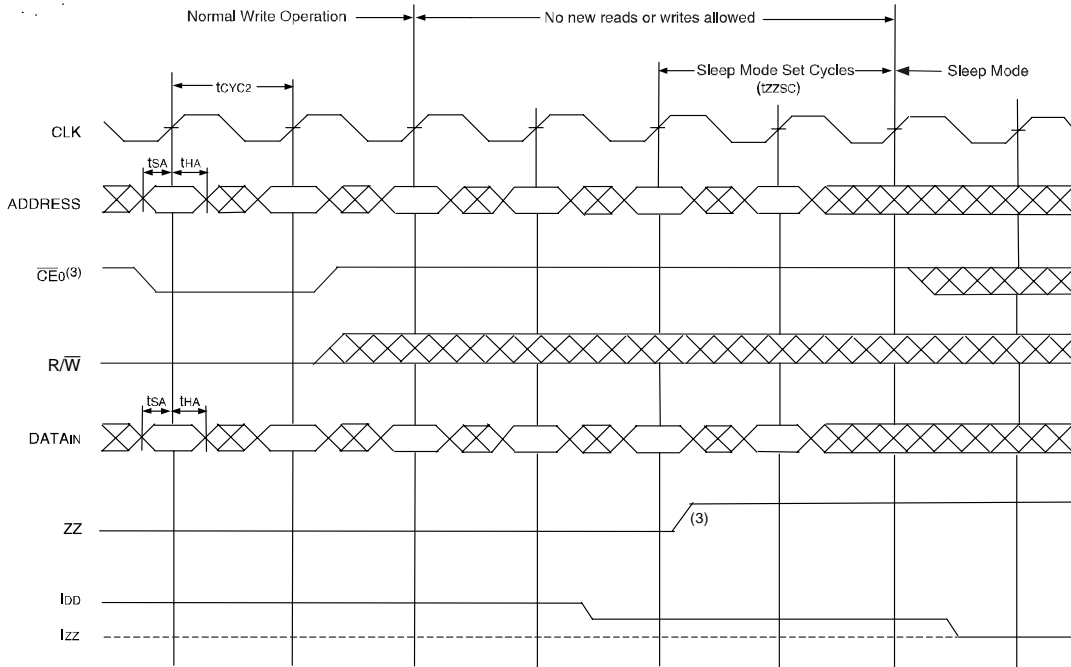
Left Port					Right Port					Function
CLKL	R \overline{W} L ⁽¹⁾	CE _L ⁽¹⁾	A _{17L} -A _{0L} ⁽²⁾	\overline{COLL}	CLKR	R \overline{W} R ⁽¹⁾	CE _R ⁽¹⁾	A _{17R} -A _{0R} ⁽²⁾	\overline{COLR}	
↑	H	L	MATCH	H	↑	H	L	MATCH	H	Both ports reading. Not a valid collision. No flag output on either port.
↑	H	L	MATCH	L	↑	L	L	MATCH	H	Left port reading, Right port writing. Valid collision, flag output on Left port.
↑	L	L	MATCH	H	↑	H	L	MATCH	L	Right port reading, Left port writing. Valid collision, flag output on Right port.
↑	L	L	MATCH	L	↑	L	L	MATCH	L	Both ports writing. Valid collision. Flag output on both ports.

NOTES:

1. $\overline{CE}_0 = V_{IL}$ and $CE_1 = V_{IH}$. R \overline{W} and CE are synchronous with respect to the clock and need valid set-up and hold times.
2. Address is for internal register, not the external bus, i.e., address needs to be qualified by one of the Address counter control signals.

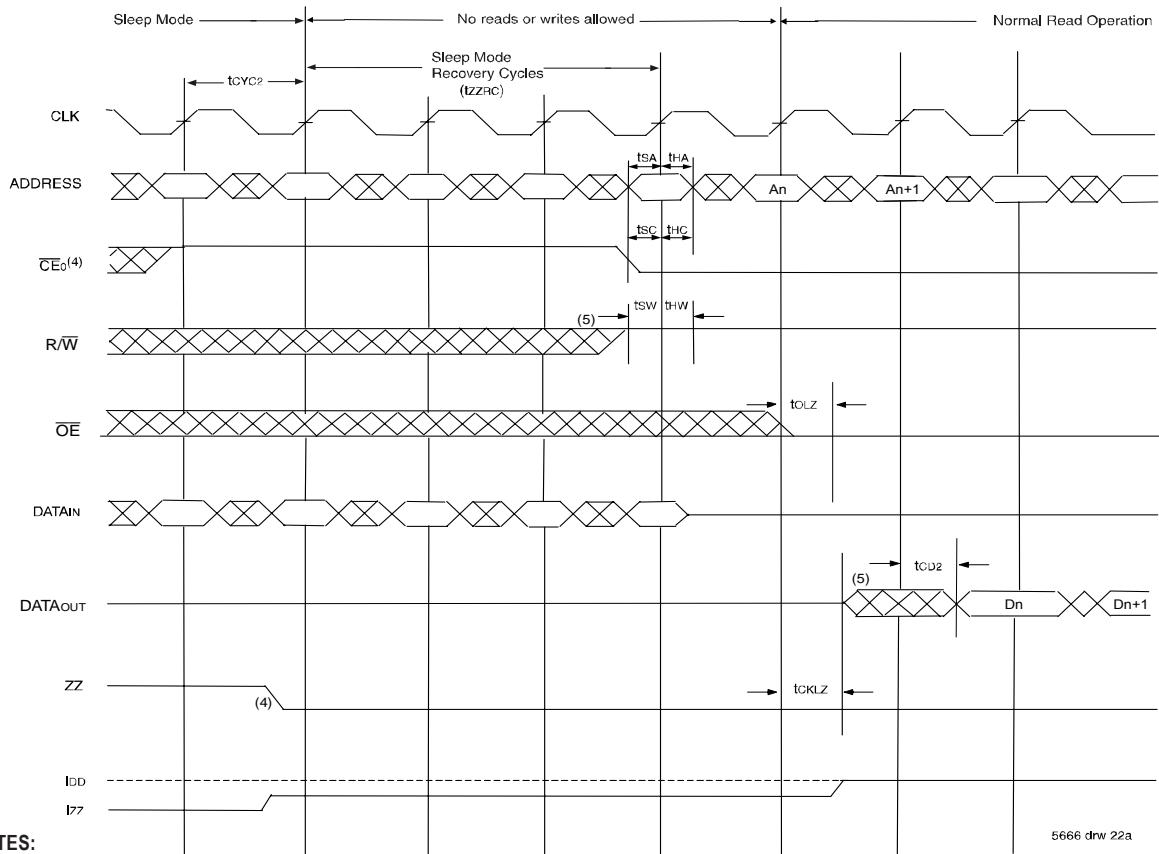
5666 tbl 14

Timing Waveform - Entering Sleep Mode (1,2)



5666 drw 22

Timing Waveform - Exiting Sleep Mode (1,2)



5666 drw 22a

NOTES:

1. $CE_1 = V_{IH}$.
2. All timing is same for Left and Right ports.
3. \overline{CE}_0 has to be deactivated ($\overline{CE}_0 = V_{IH}$) three cycles prior to asserting ZZ ($ZZx = V_{IH}$) and held for two cycles after asserting ZZ ($ZZx = V_{IH}$).
4. \overline{CE}_0 has to be deactivated ($\overline{CE}_0 = V_{IH}$) one cycle prior to de-asserting ZZ ($ZZx = V_{IL}$) and held for three cycles after de-asserting ZZ ($ZZx = V_{IL}$).
5. The device must be in Read Mode (R/\overline{W} High) when exiting sleep mode. Outputs are active but data is not valid until the following cycle.

Functional Description

The IDT70T3519/99/89 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse width is independent of the cycle time.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

A HIGH on \overline{CE}_0 or a LOW on CE1 for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T3519/99/89s for depth expansion configurations. Two cycles are required with \overline{CE}_0 LOW and CE1 HIGH to re-activate the outputs.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INT}_L) is asserted when the right port writes to memory location 3FFFE (HEX), where a write is defined as $\overline{CE}_R = R/\overline{W}_R = V_{IL}$ per the Truth Table. The left port clears the interrupt through access of address location 3FFFE when $\overline{CE}_L = V_{IL}$ and $R/\overline{W}_L = V_{IH}$. Likewise, the right port interrupt flag (\overline{INT}_R) is asserted when the left port writes to memory location 3FFFF (HEX) and to clear the interrupt flag (\overline{INT}_R), the right port must read the memory location 3FFFF (1FFFF or 1FFFE for IDT70T3599 and FFFF or FFFE for IDT70T3589). The message (36 bits) at 3FFFE or 3FFFF (1FFFF or 1FFFE for IDT70T3599 and FFFF or FFFE for IDT70T3589) is user-defined since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FFFE and 3FFFF (1FFFF or 1FFFE for IDT70T3599 and FFFF or FFFE for IDT70T3589) are not used as mail boxes, but as part of the random access memory. Refer to Truth Table III for the interrupt operation.

Collision Detection

Collision is defined as an overlap in access between the two ports resulting in the potential for either reading or writing incorrect data to a specific address. For the specific cases: (a) Both ports reading - no data is corrupted, lost, or incorrectly output, so no collision flag is output on either port. (b) One port writing, the other port reading - the end result of the write will still be valid. However, the reading port might capture data that is in a state of transition and hence the reading port's collision flag is output. (c) Both ports writing - there is a risk that the two ports will interfere with each other, and the data stored in memory will not be a valid write from either port (it may essentially be a random combination of the two). Therefore, the collision flag is output on both ports. Please refer to Truth Table IV for all of the above cases.

The alert flag (\overline{COL}_x) is asserted on the 2nd or 3rd rising clock edge of the affected port following the collision, and remains low for one cycle. Please refer to Collision Detection Timing table on Page 21. During that next cycle, the internal arbitration is engaged in resetting the alert flag (this avoids a specific requirement on the part of the user to reset the alert flag). If two collisions occur on subsequent clock cycles, the second collision may not generate the appropriate alert

flag. A third collision will generate the alert flag as appropriate. In the event that a user initiates a burst access on both ports with the same starting address on both ports and one or both ports writing during each access (i.e., imposes a long string of collisions on contiguous clock cycles), the alert flag will be asserted and cleared every other cycle. Please refer to the Collision Detection timing waveform on Page 21. Collision detection on the IDT70T3519/99/89 represents a significant advance in functionality over current sync multi-ports, which have no such capability. In addition to this functionality the IDT70T3519/99/89 sustains the key features of bandwidth and flexibility. The collision detection function is very useful in the case of bursting data, or a string of accesses made to sequential addresses, in that it indicates a problem within the burst, giving the user the option of either repeating the burst or continuing to watch the alert flag to see whether the number of collisions increases above an acceptable threshold value. Offering this function on chip also allows users to reduce their need for arbitration circuits, typically done in CPLD's or FPGA's. This reduces board space and design complexity, and gives the user more flexibility in developing a solution.

Sleep Mode

The IDT70T3519/99/89 is equipped with an optional sleep or low power mode on both ports. The sleep mode pin on both ports is asynchronous and active high. During normal operation, the ZZ pin is pulled low. When ZZ is pulled high, the port will enter sleep mode where it will meet lowest possible power conditions. The sleep mode timing diagram shows the modes of operation: Normal Operation, No Read/Write Allowed and Sleep Mode.

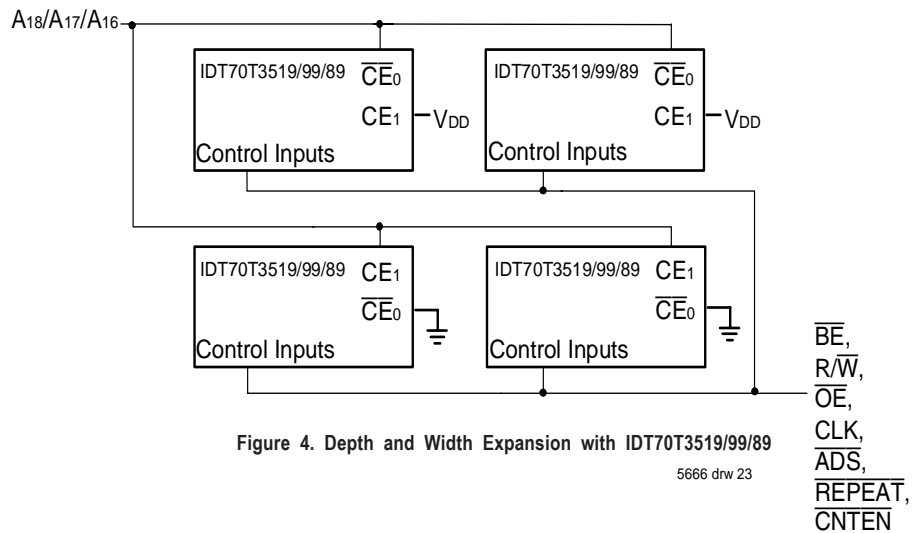
For normal operation all inputs must meet setup and hold times prior to sleep and after recovering from sleep. Clocks must also meet cycle high and low times during these periods. Three cycles prior to asserting ZZ ($ZZx = V_{IH}$) and three cycles after de-asserting ZZ ($ZZx = V_{IL}$), the device must be disabled via the chip enable pins. If a write or read operation occurs during these periods, the memory array may be corrupted. Validity of data out from the RAM cannot be guaranteed immediately after ZZ is asserted (prior to being in sleep). When exiting sleep mode, the device must be in Read mode ($R/\overline{W}_x = V_{IH}$) when chip enable is asserted, and the chip enable must be valid for one full cycle before a read will result in the output of valid data.

During sleep mode the RAM automatically deselects itself. The RAM disconnects its internal clock buffer. The external clock may continue to run without impacting the RAMs sleep current (I_{ZZ}). All outputs will remain in high-Z state while in sleep mode. All inputs are allowed to toggle. The RAM will not be selected and will not perform any reads or writes.

Depth and Width Expansion

The IDT70T3519/99/89 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70T3519/99/89 can also be used in applications requiring expanded width, as indicated in Figure 4. Through combining the control signals, the devices can be grouped as necessary to accommodate applications needing 72-bits or wider.



NOTE:

1. A18 is for IDT70T3519, A17 is for IDT70T3599, A16 is for IDT70T3589.

JTAG Timing Specifications

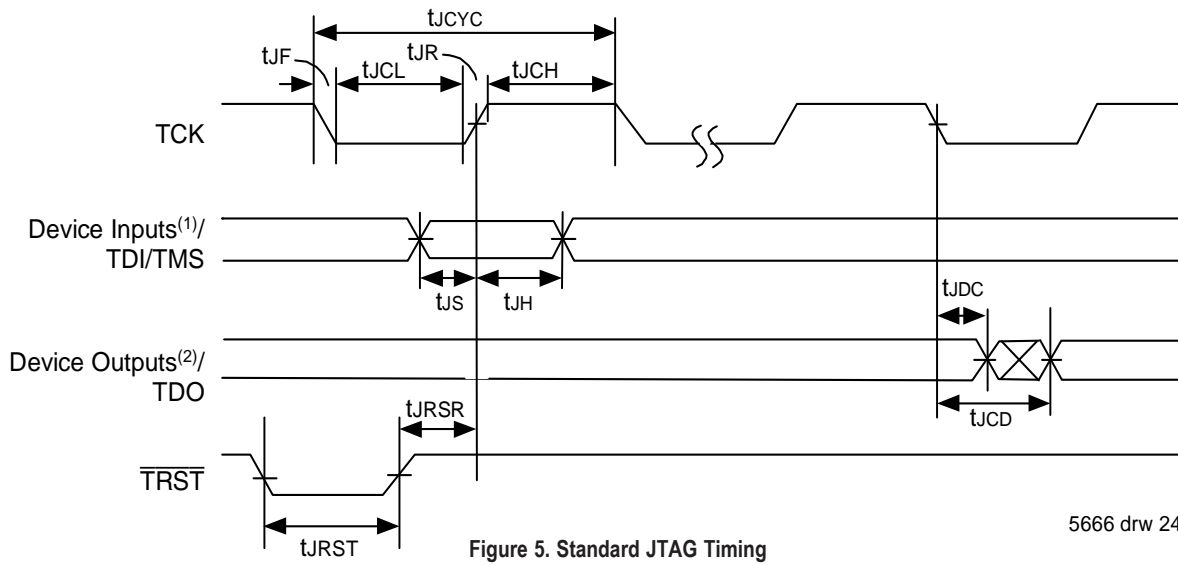


Figure 5. Standard JTAG Timing

NOTES:

1. Device inputs = All device inputs except TDI, TMS, and TRST.
2. Device outputs = All device outputs except TDO.

JTAG AC Electrical Characteristics (1,2,3,4)

Symbol	Parameter	70T3519/99/89		
		Min.	Max.	Units
t_{JCYC}	JTAG Clock Input Period	100	—	ns
t_{JCH}	JTAG Clock HIGH	40	—	ns
t_{JCL}	JTAG Clock Low	40	—	ns
t_{JR}	JTAG Clock Rise Time	—	3 ⁽¹⁾	ns
t_{JF}	JTAG Clock Fall Time	—	3 ⁽¹⁾	ns
t_{JRST}	JTAG Reset	50	—	ns
t_{JRSR}	JTAG Reset Recovery	50	—	ns
t_{JCD}	JTAG Data Output	—	25	ns
t_{JDC}	JTAG Data Output Hold	0	—	ns
t_{JS}	JTAG Setup	15	—	ns
t_{JH}	JTAG Hold	15	—	ns

5666 tbl 15

NOTES:

1. Guaranteed by design.
2. 30pF loading on external output signals.
3. Refer to AC Electrical Test Conditions stated earlier in this document.
4. JTAG operations occur at one speed (10MHz). The base device may run at any speed specified in this datasheet.

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x330 ⁽¹⁾	Defines IDT part number
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5666 tbl 16

NOTE:

1. Device ID for IDT70T3599 is 0x331. Device ID for IDT70T3589 is 0x332.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note (3)

5666 tbl 17

System Interface Parameters

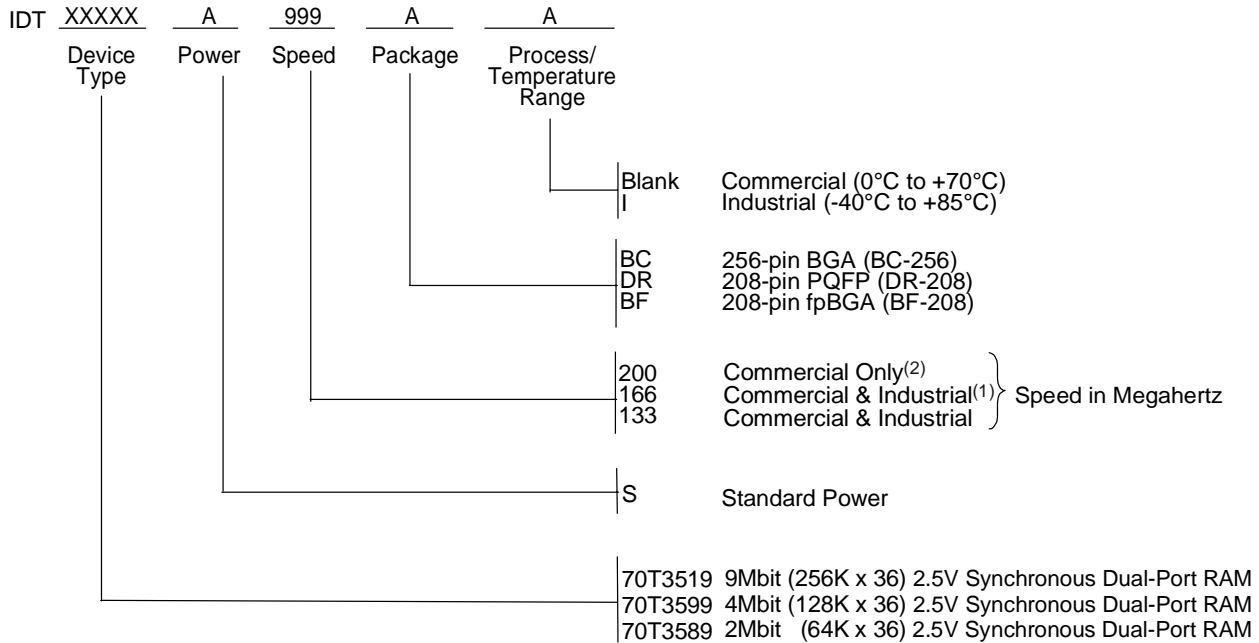
Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs ⁽¹⁾ . Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state except \overline{COLx} & \overline{INTx} outputs.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs ⁽²⁾ to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	0101, 0111, 1000, 1001, 1010, 1011, 1100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	0110, 1110, 1101	For internal use only.

5666 tbl 18

NOTES:

1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and \overline{TRST} .
3. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

Ordering Information



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NOTES:

- 166MHz I-Temp is not available in the BF-208 package.
- 200MHz is not available in the BF-208 and DR-208 packages.

IDT Clock Solution for IDT70T3519/99/89 Dual-Port

IDT Dual-Port Part Number	Dual-Port I/O Specifications		Clock Specifications				IDT PLL Clock Device	IDT Non-PLL Clock Device
	Voltage	I/O	Input Capacitance	Input Duty Cycle Requirement	Maximum Frequency	Jitter Tolerance		
70T3519/99/89	2.5	LVTTTL	8pF	40%	200	75ps	5T2010	5T9010 5T9050, 5T9050 5T907, 5T9070

5666 tbl 19

Datasheet Document History:

- 01/23/03: Initial Datasheet
- 01/30/03: Page 1 Corrected 208-pin package from TQFP to PQFP
- 04/25/03: Page 11 Added Capacitance Derating drawing
Page 12 Changed t_{INS} and t_{INR} specs in AC Electrical Characteristics table
- 11/11/03: Page 10 Updated power numbers in DC Electrical Characteristics table
Page 12 Added t_{OFS} symbol and parameter to AC Electrical Characteristics table
Page 21 Updated Collision Timing waveform
Page 22 Added Collision Detection Timing table and footnotes
Page 26 Updated HIGHZ function in System Interface Parameters table
Page 27 Added IDT Clock Solution table
- 03/30/04: Page 22 & 23 Clarified Sleep Mode Text and Waveforms
Page 1 & 27 Removed Preliminary status
- 04/22/04: Page 6 Added another sentence to footnote 4 to recommend that boundary scan not be operated during sleep mode

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