INTEGRATED TECHNOLOGY EXPRESS, INC.

IT8875F

PCI Parallel Port

Preliminary Specification V0.1

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Additional copies of this manual or other ITE literature may be obtained from:

ITE, Inc.
Marketing Department
7F, No. 435, Nei Hu District, Jui Kuang Rd.,
Taipei 114, Taiwan, R.O.C.

Phone: (02) 2657-9896
Fax: (02) 2657-8561, 2657-8576

ITE (USA) Inc.
Marketing Department
1235 Midas Way
Sunnyvale, CA 94086
U.S.A.

Phone: (408) 530-8860
Fax: (408) 530-8861

ITE (USA) Inc.
Eastern U.S.A. Sales Office
896 Summit St., #105
Round Rock, TX 78664
U.S.A.

Phone: (512) 388-7880
Fax: (512) 388-3108

If you have any marketing or sales questions, please contact:

Lawrence Liu, at ITE Taiwan: E-mail: lawrence.liu@ite.com.tw, Tel: 886-2-26579896 X6071, Fax: 886-2-26578561
David Lin, at ITE U.S.A: E-mail: david.lin@iteusa.com, Tel: (408) 530-8860 X238, Fax: (408) 530-8861
Don Gardenhire, at ITE Eastern USA Office: E-mail: don.gardenhire@iteusa.com, Tel: (512) 388-7880, Fax: (512) 388-3108

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- **PCI Interface**
  - PCI Specification V2.1 compliant
  - Supports 32-bit PCI bus & up to 33 MHz PCI bus frequency
  - Supports PERR# & SERR# Error Reporting
  - Supports Delayed Transaction

- **Programmable PCI Address Decoders**
  - Supports 6 programmable, size configurable, I/O and memory spaces
  - Provides 5 positively decoded I/O blocks

- **Compact Bus Interface**
  - Supports a compact bus structure to hook up an external I/O device
  - Supports maximum 4 decoding chip selects

- **IEEE 1284 Parallel Port**
  - Standard mode –Bi-directional SPP compliant
  - Enhanced mode –EPP V. 1.7 and V. 1.9 compliant
  - High speed mode –ECP, IEEE 1284 compliant
  - Back-drive current reduction
  - Printer power-on damage reduction

- **SM Bus**
  - Compliant with System Management Bus Specification R. 1.0
  - Supports single master mode
  - Interfaced to Serial E^2PROM

- **Power-on Serial Bus Configuration**
  - Power-on auto configuration through SM bus
  - Patent pending on auto-start and auto-stop scheme

- **Miscellanies**
  - Supports 24 MHz Oscillator circuit

- **+3.3V PCI I/F with +5V tolerant I/O buffers, +5V ISA I/F and core Power Supply**

- **Package: 128-pin PQFP**

2. General Description

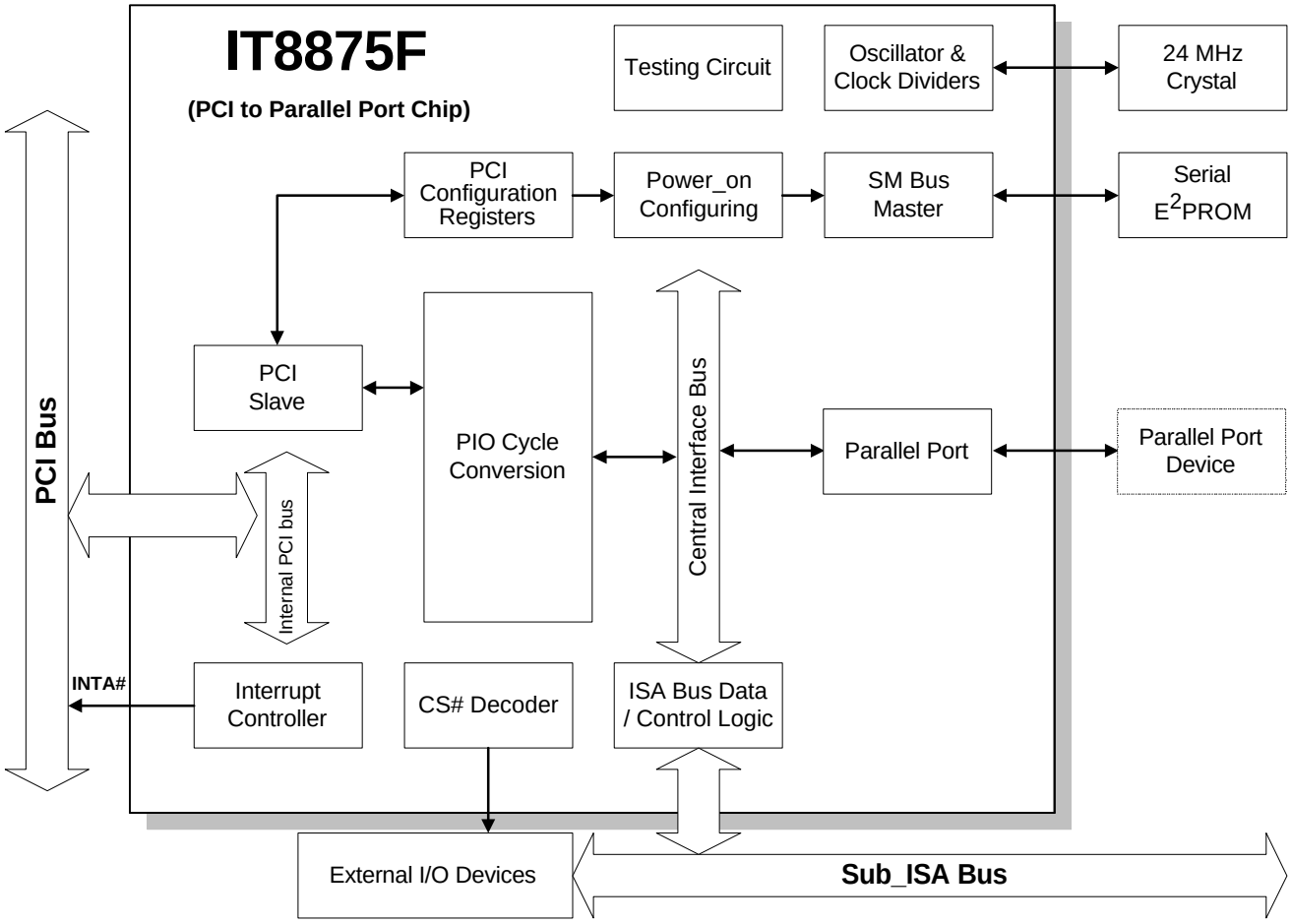
The IT8875F is a PCI interface to a parallel port chip. The IT8875F s 32-bit PCI bus interface is compliant with PCI Specification V2.1.

The parallel port in IT8875F supports standard mode (SPP), EPP V.17 and V.19 and ECP mode. Due to the variation of system platform, DMA mode is NOT supported in IT8875F. The IT8875F also provides a compact bus structure to connect an external device. The compact bus structure facilitates the system engineers to hook an 8-bit external device by programming the INTC base address register and positive decoding registers. Overall, the IT8875F provides a simple solution to build a parallel port on PCI bus.

In addition, the IT8875F also integrates one SM bus (single master mode) which can be connected to a Serial E^2PROM for automatic power-on configuration and providing customers with maximum design flexibility.

The IT8875F is available in 128-pin PQFP package.

3. Block Diagram



4. Pin Configuration

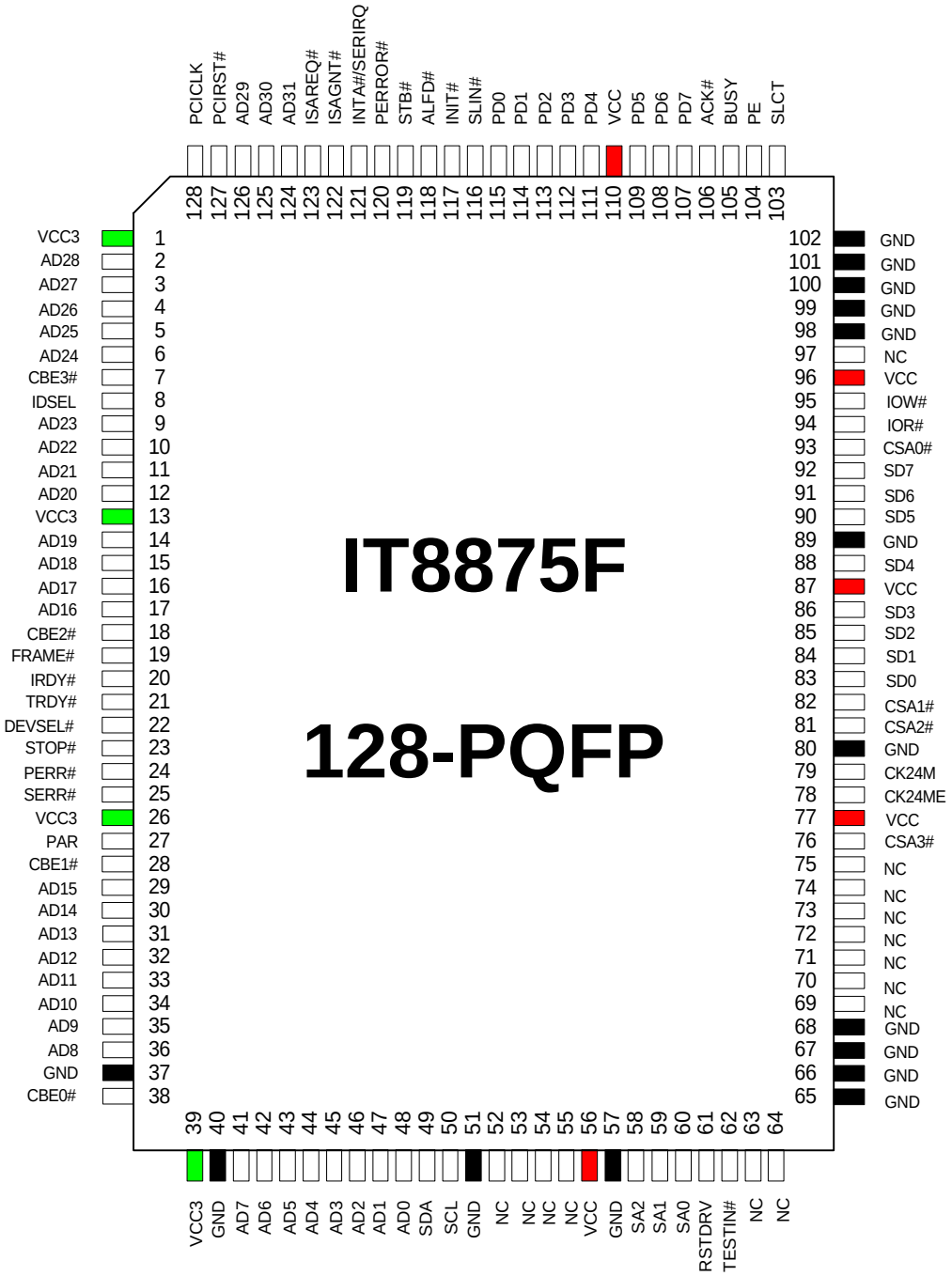


Table 4-1. Pins Listed in Numeric Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VCC3	33	AD11	65	GND	97	NC
2	AD28	34	AD10	66	GND	98	GND
3	AD27	35	AD9	67	GND	99	GND
4	AD26	36	AD8	68	GND	100	GND
5	AD25	37	GND	69	NC	101	GND
6	AD24	38	CBE0#	70	NC	102	GND
7	CBE3#	39	VCC3	71	NC	103	SLCT
8	IDSEL	40	GND	72	NC	104	PE
9	AD23	41	AD7	73	NC	105	BUSY
10	AD22	42	AD6	74	NC	106	ACK#
11	AD21	43	AD5	75	NC	107	PD7
12	AD20	44	AD4	76	CSA3#	108	PD6
13	VCC3	45	AD3	77	VCC	109	PD5
14	AD19	46	AD2	78	CK24ME	110	VCC
15	AD18	47	AD1	79	CK24M	111	PD4
16	AD17	48	AD0	80	GND	112	PD3
17	AD16	49	SDA	81	CSA2#	113	PD2
18	CBE2#	50	SCL	82	CSA1#	114	PD1
19	FRAME#	51	GND	83	SD0	115	PD0
20	IRDY#	52	NC	84	SD1	116	SLIN#
21	TRDY#	53	NC	85	SD2	117	INIT#
22	DEVSEL#	54	NC	86	SD3	118	ALFD#
23	STOP#	55	NC	87	VCC	119	STB#
24	PERR#	56	VCC	88	SD4	120	PERROR#
25	SERR#	57	GND	89	GND	121	INTA#/SERIRQ
26	VCC3	58	SA2	90	SD5	122	ISAGNT#
27	PAR	59	SA1	91	SD6	123	ISAREQ#
28	CBE1#	60	SA0	92	SD7	124	AD31
29	AD15	61	RSTDRV	93	CSA0#	125	AD30
30	AD14	62	TESTIN#	94	IOR#	126	AD29
31	AD13	63	NC	95	IOW#	127	PCIRST#
32	AD12	64	NC	96	VCC	128	PCICLK

5. IT8875F Pin Descriptions

Table 5-1. Pin Descriptions of Supplies Signals

Pin(s) No.	Symbol	Attribute	Power	Description
56, 77 ,87, 96, 110	**VCC**	PWR	-	***+5V Power Supply.***
1, 13, 26, 39	**VCC3**	PWR	-	***+3.3V Power Supply.***
37, 40, 51, 57, 65, 66, 67, 68, 80, 89, 98, 99, 100, 101, 102	**GND**	GND	-	***Ground.***

Table 5-2. Pin Descriptions of PCI Bus Interface Signals

Pin(s) No.	Symbol	Attribute	Power	Description
124-126, 2-6, 9-12, 14-17, 29-36, 41-48	**AD[31:0]**	I/O16	VCC3	***PCI Multiplexed Address / Data 31 – 0.*** 32-bit bi-directional address/data multiplexed lines. AD31 is the MSB and AD0 is the LSB. The direction of these pins are defined below: ***PHASE*** — ***Bus Master*** — ***Target*** Address Phase — Output — Input Read Data Phase — Input — Output Write Data Phase — Output — Input
7, 18, 28, 38	**CBE[3:0]#**	I/O16	VCC3	***Command/Byte Enable 3 - 0 #.*** Multiplexed bus command and byte enables.
22	**DEVSEL#**	I/O16	VCC3	***Device Select #.*** When driven active low, the signal indicates the driving device has decoded its address as the target of the current access. This pin acts as an output pin when the IT8875F (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.
21	**TRDY#**	I/O16	VCC3	***Target Ready #.*** This signal indicates that the target of the current data phase of the transaction is ready to be completed. This pin acts as an output pin when the IT8875F (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.
20	**IRDY#**	I/O16	VCC3	***Initiator Ready #.*** This signal indicates that the initiator is ready to complete the current data phase of the transaction.

Table 5-2. Pin Descriptions of PCI Bus Interface Signals (cont' d)

Pin(s) No.	Symbol	Attribute	Power	Description
19	**FRAME#**	I/O16	VCC3	***FRAME #.*** This signal is driven by the initiator to indicate the beginning and duration of a PCI access.
8	**IDSEL**	I	VCC3	***Initialization Device Select.*** This signal is used as a chip select during PCI Configuration read / write transactions.
27	**PAR**	I/O16	VCC3	***Parity.*** This signal is used for the even parity check on both AD[31:0] & CBE[3:0]# lines. The PAR input/output direction follows the AD[31:0] input/output direction.
24	**PERR#**	I/O16	VCC3	***Parity Error #.*** This signal is used for reporting data parity errors during all PCI transactions, except in a Special Cycle. PERR# is an output when it detects a parity error in receiving data as a PCI Target.
25	**SERR#**	I/O16_OD	VCC3	***System Error #.*** This signal is used for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. (input for IC test only)
23	**STOP#**	I/O16	VCC3	***Stop #.*** This signal indicates that the current target is requesting the initiator to stop the current transaction. This pin acts as an output pin when the IT8875F (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.
121	**INTA# / SERIRQ**	I/O16_OD	VCC3	***PCI Bus Interrupt Request A # / Serialized IRQ.*** Interrupt Request A# of PCI bus. Serialized IRQ (for on board testing only).
123	**ISAREQ#**	I/O8	VCC3	***PCI Bus Request #.*** This request signal is asserted to request the host bridge.
122	**ISAGNT#**	I	VCC3	***PCI Bus Grant #.*** This acknowledge (grant) signal is asserted from the host bridge.
128	**PCICLK**	I	VCC3	***33 MHz PCI Clock.***
127	**PCIRST#**	I	VCC3	***PCI Bus Reset #.*** PCIRST# is used to reset PCI bus devices.

Table 5-3. Pin Descriptions of Partial ISA Bus Signals

Pin(s) No.	Symbol	Attribute	Power	Description
58-60	**SA[2:0]**	I_SC_PU/O8	VCC	***ISA Address 2 - 0.*** SA[2:0] are ISA address outputs. They are also testing inputs.
83-86, 88, 90-92	**SD[7:0]**	I_SC_PU/O8	VCC	***ISA Data 7 - 0.*** 8-bit bi-directional data lines. SD7 is the MSB.
94	**IOR#**	I_SC_PU/O8	VCC	***I/O Read #.*** Active low output asserted by the CPU to read data or status information from the ISA device. This pin acts as input when the chip is being tested.
95	**IOW#**	I_SC_PU/O8	VCC	***I/O Write #.*** Active low output asserted by the CPU to write data or control information to the ISA device. This pin acts as an input when the chip is being tested.
61	**RSTDRV**	I_SC_PU/O8	VCC	***ISA Reset.*** A high level on this output resets the ISA bus. This signal asynchronously terminates any activity and places the ISA device in the reset state.

Table 5-4. Pin Descriptions of Parallel Port Signals

Pin(s) No.	Symbol	Attribute	Power	Description
103	**SLCT**	I_SC_PU	VCC	***Printer Being Selected Indicator.*** The SLCT is the input status to indicate the printer is being selected to respond to the Parallel port transaction.
104	**PE**	I_SC_PU	VCC	***Printer Paper End Indicator.*** The PE is the input status to indicate the printer has run out of paper.
105	**BUSY**	I_SC_PU	VCC	***Printer Busy Indicator.*** The BUSY is the input status to indicate the printer has a local operation in progress and can not accept data.
106	**ACK#**	I_SC_PU	VCC	***Printer Acknowledge Indicator#.*** The ACK# is the input status to indicate the printer has already received a character and ready to accept another one.
120	**PERROR#**	I_SC_PU	VCC	***Printer ERROR#.*** Printer Error input for Parallel Port I/F.
116	**SLIN#**	I_SC_PU/O 24	VCC	***Printer SLIN #.*** Printer Selecting output for Parallel Port I/F.
117	**INIT#**	I_SC_PU/O 24	VCC	***Printer INIT#.*** Printer initializing output for Parallel Port I/F.
118	**ALFD#**	I_SC_PU/O 24	VCC	***Printer ALFD#.*** Printer Auto Line Feed output for Parallel Port I/F.
119	**STB#**	I_SC_PU/O 24	VCC	***Printer STB#.*** Printer STROBE output for Parallel Port I/F.
107-109, 111-115	**PD[7:0]**	I_SC_PU/O 24	VCC	***Parallel Port Data Bus: PD7~PD0.*** Printer Data bus for Parallel Port I/F.

Table 5-5. Pin Descriptions of Miscellaneous Signals

Pin(s) No.	Symbol	Attribute	Power	Description
49	**SDA**	I_SC_PU/O4_OD	VCC	***Serial Bus Data.*** System Management Bus data for Serial E^2PROM.
50	**SCL**	I_SC_PU/O4_OD	VCC	***Serial Bus Clock.*** System Management Bus clock output for Serial E^2PROM. (input for IC test only)
62	**TESTIN#**	I_PU	VCC	***Chip Test Mode.*** For Chip testing only, and should be left unconnected or P/U.
78, 79	**CK24ME/ CK24M**	I/O_OSC/ I_OSC	VCC	***24 MHz Oscillator.*** ***Connected to 24 MHz Crystal.***
76, 81, 82, 93	**CSA[3:0]#**	I_SC_PU/O4	VCC	***Chip Select Group_A[3:0] #.*** Chip Select Group_A[3-0] output which shares the same high base address.
52-55	**NC**	-	-	***Not Connected.***
63-64	**NC**	-	-	***Not Connected.***
69-75	**NC**	-	-	***Not Connected.***
97	**NC**	-	-	***Not Connected.***

Attributes:

I: Input
I/O8: 8mA Input/Output
I/O16: 16mA Input/Output
I/O16_OD: 16mA Input/Open Drain Output
I_SC_PU: Schmitt Input with 50K Pull Down
I_SC_PU/O8: 8 mA Schmitt input with 50K Pull Up/Output
I_SC_PU/O24: 24 mA Schmitt input with 50K Pull Up/Output

6. Power On Strapping Options

Symbol	Pin #	Jumper	Description
CSA0#	**93**	(P/Up)	INTA#.
		P/Down	SERIRQ#.
CSA2#	**81**	(P/Up)	Enable SM Bus Boot ROM Configuration. It will set Cfg_50h<4>, but will be auto-cleared when finishing download configure code.
		P/Down	Disable SM Bus Boot ROM Configuration.

7. System Configuration

7.1 Overview

The IT8875F is a PCI to parallel port interface and provides a method to hook up an I/O device onto PCI bus with a compact bus interface. The IT8875F's 32-bit PCI bus interface is compliant with PCI Specification V2.1. The PCI interface also supports positive decode space and 6 PCI I/O or Memory spaces.

The device also contains one SM bus (single master mode) which can be connected to Serial E^2PROM for automatic power-on configuration.

The IT8875F also provides one PCI interrupt pin and Serial IRQ which can be selected during the power-on strapping. The IT8875F is available in 128-pin PQFP package.

7.2 Features

- **PCI Interface**
  - PCI Specification V2.1 Compliant
  - Supports 32-bit PCI bus & up to 33 MHz PCI bus frequency
  - Supports PERR# & SERR# Error Reporting
  - Supports Delayed Transaction
- **IEEE 1284 Parallel Port**
  - Standard mode – Bi-directional SPP compliant
  - Enhanced mode – EPP V. 1.7 and V. 1.9 compliant
  - High speed mode – ECP, only PIO mode supported
  - Back-drive current reduction
  - Printer power-on damage reduction
- **Compact External Bus Interface**
  - Supports only 8-bit I/O interface
- **Programmable PCI Address Decoders**
  - Supports programmable positive decode of PCI cycles only
  - Provides 5 positively decoded I/O blocks
- **SM Bus**
  - Compliant with System Management Bus Specification R. 1.0
  - Supports single master mode
  - Interfaces to Serial E^2PROM
- **Power-on Serial Bus Configuration**
  - Power-on auto configuration through SM bus
  - Patent pending on auto-start and auto-stop scheme
- **Serial IRQ**
  - Complies with Serialized IRQ Support for PCI system R6.0
  - Supports both continuous and quiet modes
  - Auto-detects Start Frame width and slot number
- **4 Chip Selects**
  - Supports 8 bytes space

8. Functional Description

The IT8875F provides a PCI bus to parallel port interface and a compact bus structure used to connect an external device. There are some sub-function blocks in the IT8875F as described below:

8.1 PCI Slave Interface

The IT8875F PCI Slave interface provides some positively decode spaces:

- IT8875F PCI configuration register spaces – positively decode w/ medium DEVSEL# speed on the Type0 PCI configuration cycle. The access space is described in section 9.2 Access Configuration Registers on page 24
- 6 PCI I/O or memory spaces. The space size and attribute of the address register depend on SMB load value for the corresponding register. For size, when the bit is loaded with a "0", it is read only, and hard wired to "0": Cfg_10h ~ Cfg_24h
- Five I/O positively decode spaces – defined in IT8875F Configuration Registers: Cfg_60h ~ Cfg_70h.

The IT8875F supports PCI 2.1 Delayed Transaction feature which can be enabled / disabled by programming Cfg_40h<21>. The benefit of Delayed Transaction is that the PCI bus is still available and can be used by another PCI master, even when there is an ISA PIO cycle in progress behind IT8875F.

8.2 PCI Parity

The IT8875F, like other standard PCI devices, can handle parity error and other errors. Whenever the IT8875F detects address parity error, it is able to assert SERR# if the SERR# reporting mechanism is enabled in PCI Command/Status register.

8.3 Positively Decode Spaces

The five positively decode I/O spaces can be programmed to claim the PCI I/O cycle with Fast / Medium / Slow / DEVSEL# timing speed.

8.4 SMB Boot ROM Configuration

In addition that the IT8875F configuration can be done by PCI Configuration cycles through system chipset, the IT8875F also offers an optional configuration method via the System Management Bus (SMB, similar to I^2C BUS) Boot ROM. As the current version of IT8875F only supports single master mode, users are prohibited to connect the IT8875F SMB interface to another system SMB bus. Only Serial E^2PROM can be connected, and the preset slave address is 1010000b.

The Serial E^2PROM Data is grouped by each five bytes into the 1st byte, which serves as an index to indicate which PCI Configuration register is. The other 4 bytes are the 32-bit data, which will be written to the indexed register.

SMB ROM Data format in Serial E^2PROM is illustrated below:

ROM Address	ROM Data	IT8875F Operation
top		
5n	Index = AAh	Stop
5m+4	Data	Cfg_50h<31:24>
5m+3	Data	Cfg_50h<23:16>
5m+2	Data	Cfg_50h<15:8>
5m+1	Data	Cfg_50h<7:0>
5m	Index = 50h	Cfg_50h
6	Data	Cfg_XXh<7:0>
5	Index = XXh	Cfg_XXh
4	Data	Cfg_??h<31:24>
3	Data	Cfg_??h<23:16>
2	Data	Cfg_??h<15:8>
1	Data	Cfg_??h<7:0>
0	Index = ??h	Cfg_??h

Whether the chip will execute SMB Boot ROM Configuring Sequence or not is determined by one power-on-strap setting. Please refer to the table in section 6 Power On Strapping Options on page 15. If SMB Boot ROM Configuration is enabled, the IT8875F will then set the SMB_In_Progress status bit (Cfg_40h<18>) on page 32 and begin to issue the I^2C Sequential Read Operation. It writes to PCI Configuration Registers after it has finished reading every five bytes from SMB ROM. If it reads an Index value as AA_{hex}, it will then stop I^2C Sequential Read Operation and clear the SMB_In_Progress status bit. The system BIOS can monitor the status bit to see if SMB is in progress before BIOS can decide to enable some computer system sub-functions.

Conversely, if SMB Boot ROM Configuration is disabled in power-on-strap setting, the IT8875F will then clear the SMB_In_Progress status bit, and no I^2C Sequential Read Operation occurs.

For instance, if users intend to claim one I/O space of $02AC_h$ ~ $02AD_h$ (2byte size) for a special ISA card (or users try to hook up the ISA device to PCI bus), a Serial E^2PROM can be programmed. The resulted data are listed on the next page:

Serial E^{2}PROM Address	Serial E^{2}PROM Data	IT8875F Configuration Register
top ~ 6	XX_h	
5	**AA_h**	IT8875F SMB I/F Stop
4	$C1_h$	Cfg_64h<31:24> Medium DEVSEL#, 2Byte size
3	00_h	Cfg_64h<23:16> = reserved
2	02_h	Cfg_64h<15:0> = $02AC_h$
1	AC_h	
0	64_h	Index 64_h => Cfg_64h

In the example above, the IT8875F SMB Configuration block will write the 32-bit data of $C10002AC_h$ to Cfg_64h when it finishes reading bytes 0~4 of Serial E^{2}PROM. After it receives an AA_h in the ROM position of 5xN (i.e. address of 5_d, 10_d, 15_d, .. etc.), the SMB I/F stops fetching more data and clears the SMB_In_Progress status bit.

For detailed SMB Configuration operation, please refer to the "IT8875F SMB Configuration Programming Guide". The SMB Boot Configuring mechanism is patent pending.

8.5 4 Chip Selects

IT8875F provides 4 chip selects for application usage. It could be 8 bytes for each space. Please refer to page 40 for more details.

8.6 Parallel Port

- Standard mode – Bi-directional SPP compliant
- Enhanced mode – EPP V. 1.7 and V. 1.9 compliant
- High speed mode – ECP, Only PIO mode supported
- Back-drive current reduction
- Printer power-on damage reduction

9. Register Descriptions

9.1 Configuration Register Map

The IT8875F PCI header configuration register set complies with Type 00h Configuration Space Header described in the PCI Specification R. 2.1.

Table 9-1. IT8875F Configuration Register Map

31 16	15 00	Index
Device ID (8875h)	Vendor ID (1283h)	00h
Status	Command	04h
Base Class Code (07h) / Sub-class code(00/01)	Programming I/F (02h) / Revision ID (01h)	08h
Reserved (00h) / Header Type (00h)	Latency Timer (00h) / Cache Line Size (00h)	0Ch
PCI Space_0 Base Address		10h
PCI Space_1 Base Address		14h
PCI Space_2 Base Address		18h
PCI Space_3 Base Address		1Ch
PCI Space_4 Base Address		20h
PCI Space_5 Base Address		24h
Reserved (00000000h)		28h
Sub-system Device ID (0000h)	Sub-system Vendor ID (0000h)	2Ch
Reserved		30h
Reserved (00000000h)		34~3Bh
Reserved (0000h)	Interrupt Pin / Interrupt Line	3Ch
Global Control_1 Register		40h
Global Control_2 Register		44h
Reserved		48h
Reserved		4Ch
PCI Space_1/0 Remap Register		50h
PCI Space_3/2 Remap Register		54h
PCI Space_5/4 Remap Register		58h
Reserved		5Ch
Positively Decoded I/O_Space_0 Register		60h
Positively Decoded I/O_Space_1 Register		64h
Positively Decoded I/O_Space_2 Register		68h
Positively Decoded I/O_Space_3 Register		6Ch
Positively Decoded I/O_Space_4 Register		70h
Reserved		74h
INTC Base Address Register		78h
Reserved		7Ch
Internal Parallel Port Base Address Register		80h
Reserved		84h
External Devices Base Address Register 1		88h
Reserved		8Ch
Reserved		90h
Reserved		94h
Reserved		98h
Miscellaneous Control Register (MISCR)		9Ch
Reserved		A0h~FFh

9.2 Access Configuration Registers

The IT8875F will respond to all PCI Bus Configuration cycles when the IDSEL input is asserted high. Address bits 1-0 of the Configuration cycle are both "0", and address bits 10-8 correspond to internal functions.

The Type0 configuration address format is as follows:

AD31-11	AD10-8	AD7-2	AD1-0	CBE3-0#
Only one asserted to active IDSEL	Function Select, IT8875F only responds to Function = 000b	Register Select, to select one double-word register	Configuration Type, IT8875F only responds to Type = 00b	Byte Select, to select one or more bytes in selected double-word register

The configuration registers can be accessed as byte, or word (16 bits) or Double-Word (32 bits) quantities or any byte combination. In all of these accesses, only byte enables are used, AD[1:0] is always 00b when accessing the configuration registers. All multi-byte fields use "little-endian" ordering (that is, lower addresses contain the least significant parts of the fields). Registers that are marked "**Reserved**" will be decoded and return zeros when read. All bits defined as "**Reserved**" within IT8875F's PCI Configuration Registers will be read as zero and will be unaffected by writes, unless specifically documented otherwise.

The software can use the PCI Configuration Mechanism One to read or write the IT8875F PCI configuration register space. The PCI Configuration Mechanism One utilizes two 32-bit I/O ports located at addresses 0CF8h and 0CFCh. These two ports are:

INDEX Port: 32-bit in bit width, occupying I/O address 0CF8h through 0CFBh.
DATA Port: 32-bit in bit width, occupying I/O address 0CFCh through 0CFFh.

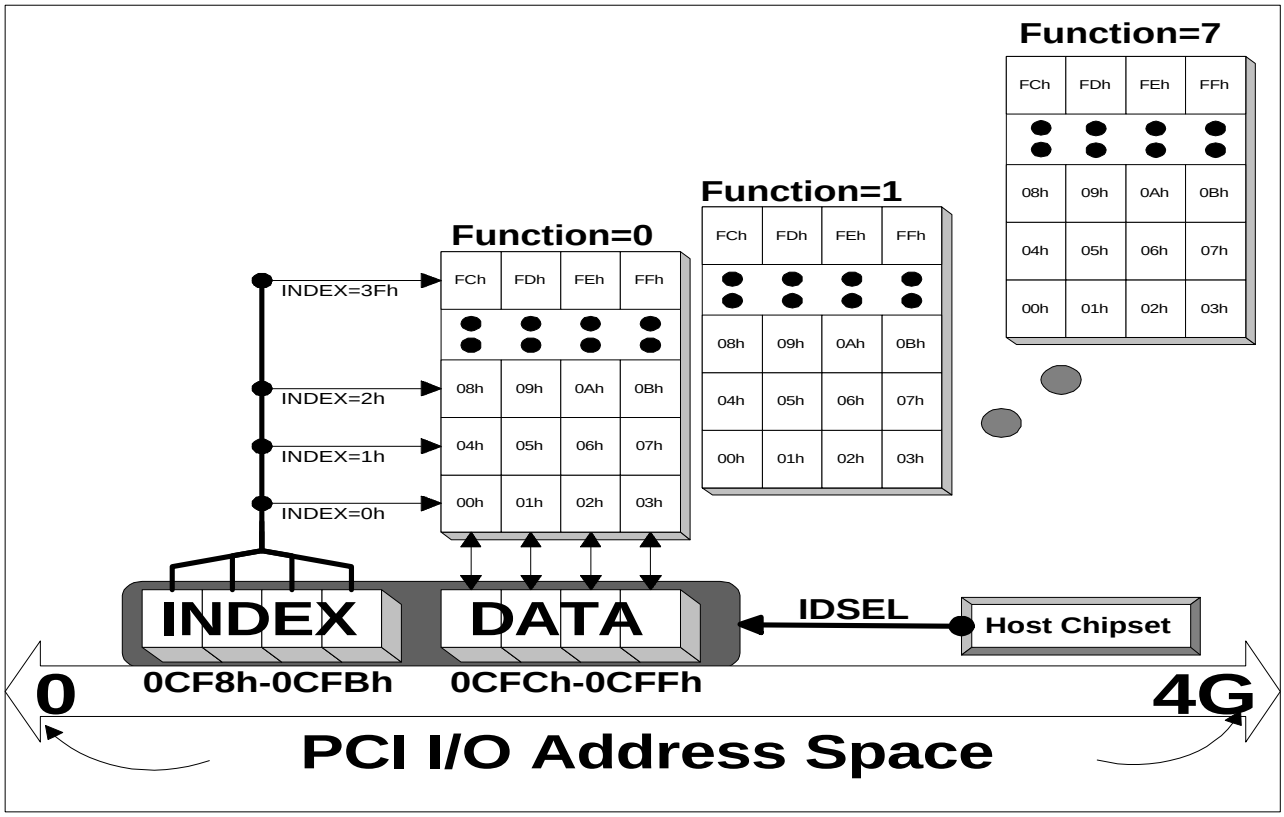


Figure 9-1. PCI Configuration Register Structure

Accessing any PCI configuration register is a two-step process:

Step 1: Perform I/O writes of the bus number, physical device number, function number, and register index number to the PCI Configuration Mechanism One INDEX Port. (The motherboard chipset will decode the bus number, device number and then generate the IDSEL signal to select the device. The device then decodes the function number to select which bank of the register is to be accessed and decodes the register index number to select which double-word register will be accessed.)

Step 2: Perform an I/O read from or write to the PCI Configuration Mechanism One DATA Port. The PCI Configuration Mechanism One INDEX & Data Port formats are illustrated below:

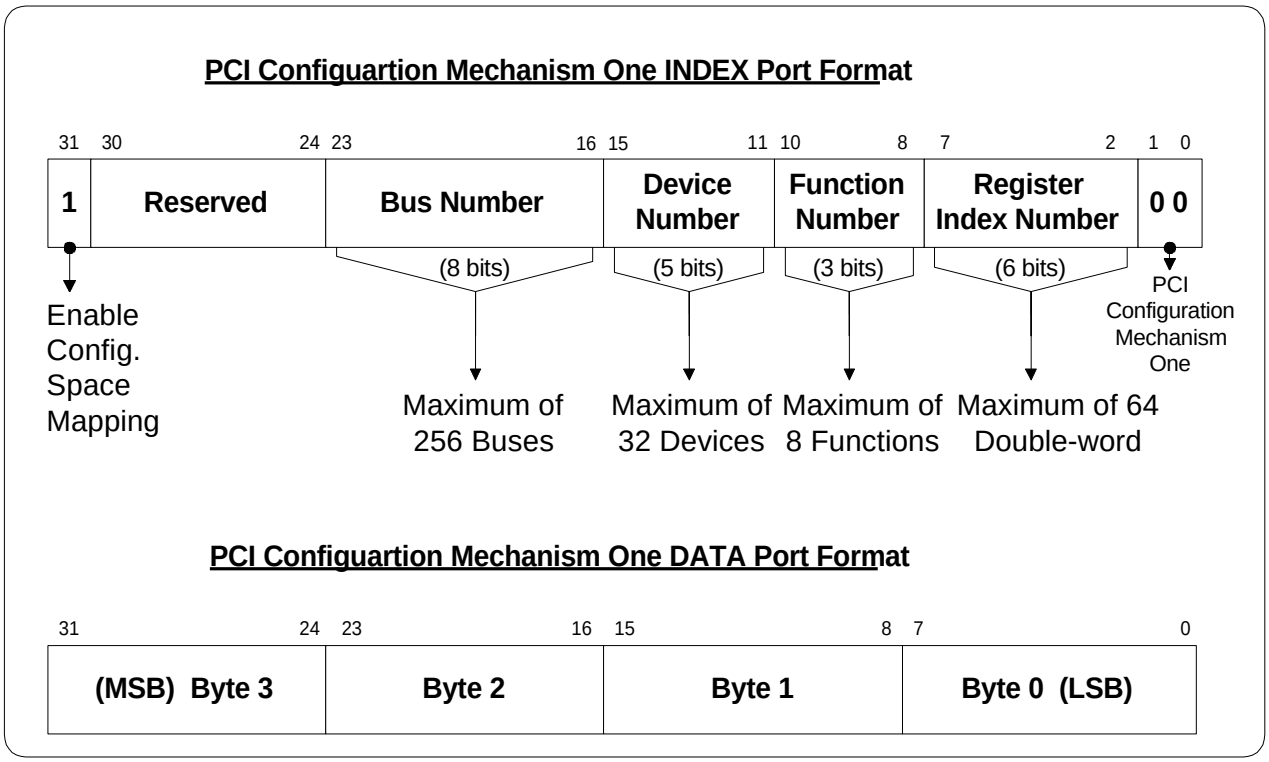


Figure 9-2. PCI Configuration Access Mechanism #1

9.3 Configuration Register Descriptions

9.3.1 Device/Vendor ID Register (IDR) – Offset 00h

Bit	R/W	Default	Description
31 - 16	R/L	8875h	**Device ID (DID)** The Device ID Register contains the device identification number for this chip - IT8875F.
15 - 0	R/L	1283h	**Vendor ID (VID)** The Vendor ID Register contains the vendor identification number for ITE.

9.3.2 Status / Command Register (SCR) – Offset 04h

Bit	R/W	Default	Description
31	R/W1C	0b	Set by IT8875F whenever it detects a parity error on PCI bus.
30	R/W1C	0b	Set by IT8875F whenever it asserts SERR#.
29	RO	0b	**Reserved**
28	RO	0b	**Reserved**
27	R/W1C	0b	Set by IT8875F whenever it, as a target, terminates a transaction by signaling a Target Abort.
26 - 25	R/L	01b	Medium DEVSEL# timing for IT8875F as a target to respond to an access on PCI bus.
24	R/W1C	0b	Set by IT8875F when two conditions are met: 1) asserting PERR# itself or observing PERR# being asserted; 2) Cfg_04h<6> is set.
23	RO	1b	Fast back-to-back capability (when IT8875F acts as a target).
22 - 16	RO	all zero	**Reserved**
15 - 10	RO	all zero	**Reserved**
9	RO	0b	**Fast Back-to-Back Control** IT8875F will not perform FBTB access to the target on PCI bus.
8	R/W/L	0b	**SERR# Drives Low Enable** A value of 1 enables IT8875F to drive SERR#. A value of 0 disables SERR# signal. **(Cfg_04_8)**
7	RO	0b	**AD Bus Stepping** IT8875F does not perform AD stepping.
6	R/W/L	0b	**Parity Error Response** When the bit is 0, IT8875F will ignore any parity error, which is detected on PCI bus interface. **(Cfg_04_6)**
5 - 2	RO	0000b	**Reserved**
1	R/W/L	0b	**Downstream memory transaction enabling (MEM_EN)**
0	R/W/L	0b	**Downstream I/O transaction enabling (IO_EN)**

9.3.3 Class Code/ Revision ID Register (CCRIDR) – Offset 08h

Bit	R/W	Default	Description
31 - 24	R/L	07h	**Base Class Code (BCC)** This register contains the Base Class Code for IT8875F. This Base Class code is 07h, indicating it is a "Simple Communication Device".
23 - 16	R/L	00h	**Sub-class Code (SCC)** This register contains the sub-class code for IT8875F. This Sub-class code is 00h, indicating it is an "Serial Port Controller." When the Sub-class code is 01h, it indicates it is an "Parallel Port Controller."
15 - 8	R/L	02h	**Programming Interface (PIF)** The PIF byte of the Class Code register indicates it is SPP or ECP, please refer to PCI Spec. 2.1, Appendix D.
7 - 0	R/L	01h	**Revision Identification (RID)** This register contains the device revision number for IT8875F device.

9.3.4 Header Type/ MLT/ Cache Line Size Register (HMCR) – Offset 0Ch

Bit	R/W	Default	Description
31 - 24	RO	00h	**Reserved**
23 - 16	RO	00h	**Header Type (HTR)** This register identifies the header layout of the configuration space.
15 - 8	RO	00h	**Reserved**
7 - 0	RO	00h	**Cache Line Size (CLS)** This register specifies the system cache-line size in the unit of 32-bit words.

9.3.5 PCI Space_0 Base Address Register (PS0BAR) – Offset 10h

Bit	R/W	Default	Description
31 - 4	R/W/L	0000000h	**PCI Space_0 Base Address Bits 31 - 4 (PS0BAR[31:4])** This PCI Space_0 Base Address, high bits are R/W/L for allocating PCI resources; low bits are Read Only as 0 for showing space size information.
3	R/W/L	0b	**PCI Space_0 Base Address Bit 3 (PS0BAR[3])** When PS0BAR<0>=0, this bit is memory prefetchable setting. When PS0BAR<0>=1, this bit is I/O space Base Address A[3].
2	R/W/L	0b	**PCI Space_0 Base Address Bit 2 (PS0BAR[2])** When PS0BAR<0>=0, this bit is must be written with 0. When PS0BAR<0>=1, this bit is I/O space Base Address A[2].
1	R/W/L	0b	**PCI Space_0 Base Address Bit 1 (PS0BAR[1])** When PS0BAR[0]>=0, this bit is memory addressing in 32-bit (set to 0) or below 1MB (set to 1). When PS0BAR[0]>=1, this bit must be written with 0.
0	R/L	1b	**PCI Space_0 Attribute (PS0BAR[0])** Set to 0 for memory space; Set to 1 for I/O space.

9.3.6 PCI Space_1 Base Address Register (PS1BAR) – Offset 14h

Bit	R/W	Default	Description
31 - 4	R/W/L	0000000h	**PCI Space_1 Base Address Bits 31 - 4 (PS1BAR[31:4])** This PCI Space_1 Base Address, high bits are R/W/L for allocating PCI resources; low bits are Read Only as 0 for showing space size information.
3	R/W/L	0b	**PCI Space_1 Base Address Bit 3 (PS1BAR[3])** When PS1BAR<0>=0, this bit is memory prefetchable setting. When PS1BAR<0>=1, this bit is I/O space Base Address A[3].
2	R/W/L	0b	**PCI Space_1 Base Address Bit 2 (PS1BAR[2])** When PS1BAR<0>=0, this bit is must be written with 0. When PS1BAR<0>=1, this bit is I/O space Base Address A[2].
1	R/W/L	0b	**PCI Space_1 Base Address Bit 1 (PS1BAR[1])** When PS1BAR[0]>=0, this bit is memory addressing in 32-bit (set to 0) or below 1MB (set to 1). When PS1BAR[0]>=1, this bit must be written with 0.
0	R/L	1b	**PCI Space_1 Attribute (PS1BAR[0])** Set to 0 for memory space; Set to 1 for I/O space.

9.3.7 PCI Space_2 Base Address Register (PS2BAR) – Offset 18h

Bit	R/W	Default	Description
31 - 4	R/W/L	0000000h	**PCI Space_2 Base Address Bits 31 - 4 (PS2BAR[31:4])** This PCI Space_2 Base Address, high bits are R/W/L for allocating PCI resources; low bits are Read Only as 0 for showing space size information.
3	R/W/L	0b	**PCI Space_2 Base Address Bit 3 (PS2BAR[3])** When PS2BAR<0>=0, this bit is memory prefetchable setting. When PS2BAR<0>=1, this bit is I/O space Base Address A[3].
2	R/W/L	0b	**PCI Space_2 Base Address Bit 2 (PS2BAR[2])** When PS2BAR<0>=0, this bit is must be written with 0. When PS2BAR<0>=1, this bit is I/O space Base Address A[2].
1	R/W/L	0b	**PCI Space_2 Base Address Bit 1 (PS2BAR[1])** When PS2BAR[0]>=0, this bit is memory addressing in 32-bit (set to 0) or below 1MB (set to 1). When PS2BAR[0]>=1, this bit must be written with 0.
0	R/L	1b	**PCI Space_2 Attribute (PS2BAR[0])** Set to 0 for memory space; Set to 1 for I/O space.

9.3.8 PCI Space_3 Base Address Register (PS3BAR) – Offset 1Ch

Bit	R/W	Default	Description
31 - 4	R/W/L	0000000h	**PCI Space_3 Base Address Bits 31 - 4 (PS3BAR[31:4])** This PCI Space_3 Base Address, high bits are R/W/L for allocating PCI resources; low bits are Read Only as 0 for showing space size information.
3	R/W/L	0b	**PCI Space_3 Base Address Bit 3 (PS3BAR[3])** When PS3BAR<0>=0, this bit is memory prefetchable setting. When PS3BAR<0>=1, this bit is I/O space Base Address A[3].
2	R/W/L	0b	**PCI Space_3 Base Address Bit 2 (PS3BAR[2])** When PS3BAR<0>=0, this bit is must be written with 0. When PS3BAR<0>=1, this bit is I/O space Base Address A[2].
1	R/W/L	0b	**PCI Space_3 Base Address Bit 1 (PS3BAR[1])** When PS3BAR[0]>=0, this bit is memory addressing in 32-bit (set to 0) or below 1MB (set to 1). When PS3BAR[0]>=1, this bit must be written with 0.
0	R/L	1b	**PCI Space_3 Attribute (PS3BAR[0])** Set to 0 for memory space; Set to 1 for I/O space.

9.3.9 PCI Space_4 Base Address Register (PS4BAR) – Offset 20h

Bit	R/W	Default	Description
31 - 4	R/W/L	0000000h	**PCI Space_4 Base Address Bits 31 - 4 (PS4BAR[31:4])** This PCI Space_4 Base Address, high bits are R/W/L for allocating PCI resources; low bits are Read Only as 0 for showing space size information.
3	R/W/L	0b	**PCI Space_4 Base Address Bit 3 (PS4BAR[3])** When PS4BAR<0>=0, this bit is memory prefetchable setting. When PS4BAR<0>=1, this bit is I/O space Base Address A[3].
2	R/W/L	0b	**PCI Space_4 Base Address Bit 2 (PS4BAR[2])** When PS4BAR<0>=0, this bit is must be written with 0. When PS4BAR<0>=1, this bit is I/O space Base Address A[2].
1	R/W/L	0b	**PCI Space_4 Base Address Bit 1 (PS4BAR[1])** When PS4BAR[0]>=0, this bit is memory addressing in 32-bit (set to 0) or below 1MB (set to 1); When PS4BAR[0]>=1, this bit must be written with 0.
0	R/L	1b	**PCI Space_4 Attribute (PS4BAR[0])** Set to 0 for memory space; Set to 1 for I/O space.

9.3.10 PCI Space_5 Base Address Register (PS5BAR) – Offset 24h

Bit	R/W	Default	Description
31 - 4	R/W/L	0000000h	**PCI Space_5 Base Address Bits 31 - 4 (PS5BAR[31:4])** This PCI Space_5 Base Address, high bits are R/W/L for allocating PCI resources; low bits are Read Only as 0 for showing space size information.
3	R/W/L	0b	**PCI Space_5 Base Address Bit 3 (PS5BAR[3])** When PS5BAR<0>=0, this bit is memory prefetchable setting. When PS5BAR<0>=1, this bit is I/O space Base Address A[3].
2	R/W/L	0b	**PCI Space_5 Base Address Bit 2 (PS5BAR[2])** When PS5BAR<0>=0, this bit is must be written with 0. When PS5BAR<0>=1, this bit is I/O space Base Address A[2].
1	R/W/L	0b	**PCI Space_5 Base Address Bit 1 (PS5BAR[1])** When PS5BAR[0]>=0, this bit is memory addressing in 32-bit (set to 0) or below 1MB (set to 1). When PS5BAR[0]>=1, this bit must be written with 0.
0	R/L	1b	**PCI Space_5 Attribute (PS5BAR[0])** Set to 0 for memory space; Set to 1 for I/O space.

9.3.11 Sub-system Device ID / Sub-system Vendor ID – Offset 2Ch

Bit	R/W	Default	Description
31 – 16	R/GW[1]/ L	0000h	**Sub-system Device ID (SDID)** This value is used to identify a particular sub-system. This register along with SVID register is used to uniquely identify the add-in board or sub-system where the PCI device resides.
15 – 0	R/GW/L	0000h	**Sub-system Vendor ID (SVID)** This value is used to identify the vendor of the sub-system. Sub-system Vendor IDs can be obtained from the PCI-SIG and are used to identify the vendor of the add-in board or sub-system.

9.3.12 Interrupt Pin/Line Register (INTR) – Offset 3Ch

Bit	R/W	Default	Description
31 - 16	RO	0000h	**Reserved**
15 - 8	R/L	00h/01h	**Interrupt Pin (INTPIN)** If SERIRQ pin function is selected, these bits default are then read as 00h; otherwise, read as 01h.
7 - 0	R/W/L	0Ah	**Interrupt Line (INTLINE)** Interrupt routine number of 8259x2.

[1] GW = Gated Write (controlled by GC1R<22>)

9.3.13 Global Control_1 Register (GC1R) – Offset 40h

Bit	R/W	Default	Description
31	R/W/L	0b	**Test SMB Interface (Test_SMB)** Reserved for IC test only.
30 - 23	R/W/L	All 0	**Reserved**
22	R/W/L	0b	**Allow PCI Configure Write Operation to Change the Content of Sub-system Device/Vendor ID Register (Sub_ID_W_EN)** 0: Disabled, only SMB_ROM Configuring can update it. 1: Enabled. It is generally provided for optional device BIOS to change sub-system ID for its device.
21	R/W/L	0b	**Enable Delayed Transaction in PIO Cycle (Delay_X_EN)** 0: Disabled. 1: Enabled.
20	RO	1b	**Reserved**
19	R/W/L	Reset Strap value of CSA1#	**Reserved**
18	RO	Reset Strap value of CSA2#	**SMB_In_Progress (SM_Cfg_Cycle)** It shows the status of SM Bus Boot ROM being in progress. If CSA2# is sampled high during reset, this bit will be set to 1, and the SM Bus Boot ROM Configuration will be initiated. Once the configuration is finished (get index= AAh), this bit will be cleared automatically.
17	R/W/L	0b	**Enable I/O Byte Lane Error to SERR# (SERR_IOBE_EN)** Enable checking PCI I/O Cycle Byte Lane Error and report to SERR#. 0: Disabled. 1: Enabled.
16	R/W1C	0b	**I/O Byte Error Status (IOBE_Status)** Read 1 as the PCI I/O Cycle Byte Lane Error occurred. Write 1 to clear.
15	R/W/L	0b	**Enable Discard Overflow Report to SERR# (SERR_Discard_EN)** 0: Disabled. 1: Enabled.
14	R/W1C	0b	Read 1 as the PCI Target interface can not receive the same retried transaction more than the time (overflow) defined in GC1R<13:8>. Write 1 to clear.
13 - 8	R/W/L	3Fh	**Discard Timer (Discard_Timer[5:0])** If the PCI Master still does not repeat the same transaction when timer expired (Value x256 PCI clocks) for the PCI Target interface that issued the retry cycle, the PCI Target interface will then stop waiting and set status bit (GC1R<14>). 00h: Never expire; 01h: 256T; FFh: 255*256T.
7	R/W/L	0b	**Enable Retry Overflow Report to SERR# (SERR_Retry_EN)** 0: Disabled. 1: Enabled.
6	R/W1C	0b	Read 1 as the PCI Master interface can not complete its transaction within the time (overflow) defined in GC1R<5:0>. Write 1 to clear.
5 - 0	R/W/L	3Fh	**Retry Timer (Retry_Timer[5:0])** PCI Master interface repeats retried transactions and if the retry counts exceed the Retry Timer value (x 8 times), the PCI Master interface will then give up more retry and set status bit (Cfg_54h<6>). 00h:Not check retry; 01h: 8 times; FFh: 255*8 times.

9.3.14 Global Control_2 Register (GC2R) – Offset 44h

Bit	R/W	Default	Description
31	R/W/L	Reset Strap value of CSA0#	**Pin # 121 Function Select (INTA_SEL)** 0: SERIRQ. 1: INTA#.
30-20	R/W/L	6BFh	**Reserved**
19 – 16	RO	0000b	**Reserved**
15 - 14	RO	10b	**Reserved**
13 - 12	R/W/L	00b	**8-bit I/O Access Recovery Time (Recovery_8[1:0])** 00b: 3.5 BCLK; 01b: 5.5 BCLK; 10b: 7.5 BCLK: 11b: 11.5 BCLK.
11	R/W/L	1b	**24M Oscillator Enable Control (OSC_En)** 1: Enabled. 0: Disabled. This Oscillator provides clocks for two internal UARTs.
10	R/W/L	1b	**24M Oscillator Pad Feedback Resistor Enable Control (OSC_R_En_)** 0: Enabled. 1: Disabled.
9 - 8	RO	11b	**Reserved**
7 - 6	R/W/L	11b	**Wait State Control of External I/O Devices (WS_XIO[1:0])** 00b: 3T (No wait state); 01b: 4T; 10b: 5T; 11b: 6T (Standard ISA 8-bit I/O).
5 - 4	RO	00b	**Reserved**
3 - 2	R/W/L	00b	**Wait State Control of Internal Parallel Port Controller (WS_IPP[1:0])** 00b: 3T (No wait state); 01b: 4T; 10b: 5T; 11b: 6T (Standard ISA 8-bit I/O).
1 - 0	RO	00b	**Reserved**

9.3.15 PCI Space_1/0 Remap Register (RMP10R) – Offset 50h

Bit	R/W	Default	Description
31 - 17	R/W/L	0000h	**Remap PCI Space_1 (RMP1[15:1])** If PCI Space_1<0> is: 0: Access to the memory space defined in PCI Space_1 will be remapped to the space of {A[31:20]=ignore, A[19:6]=RMP1[15:2], A[5:0]= same} if the space claimed is not greater than 64 bytes; otherwise {A[31:20]=ignore, A[19:(Size_bit +1)]=RMP1[15: (Size_bit – 3)], A[Size_bit:0]= same} where the Size_bit depends on the PCI Space_1 size. 1: Access to the I/O space defined in PCI Space_1 will be remapped to the space of {A[31:16]=ignore, A[15:(Size_bit+1)]=RMP1[15:(Size_bit+1)], A[Size_bit:0]=same} where the Size_bit depends on the PCI Space_1 size.
16	R/W/L		**Enable Remap PCI Space_1 (RMP1_En):** 0: Disable remapping. 1: Enable remapping.
15 - 1	R/W/L	0000h	**Remap PCI Space_0 (RMP0[15:1]).** If PCI Space_0<0> is: 0: Access to the memory space defined in PCI Space_0 will be remapped to the space of {A[31:20]=ignore, A[19:6]=RMP1[15:2], A[5:0]= same} if the space claimed is not greater than 64 bytes; otherwise {A[31:20]=ignore, A[19:(Size_bit +1)]=RMP1[15: (Size_bit – 3)], A[Size_bit:0]= same} where the Size_bit depends on the PCI Space_10 size. 1: Access to the I/O space defined in PCI Space_0 will be remapped to the space of {A[31:16]=ignore, A[15:(Size_bit+1)]=RMP0[15:(Size_bit+1)], A[Size_bit:0]=same} where the Size_bit depends on the PCI Space_0 size.
0	R/W/L		**Enable Remap PCI Space_0 (RMP0_En)** 0: Disable remapping. 1: Enable remapping.

9.3.16 PCI Space_3/2 Remap Register (RMP32R) – Offset 54h

Bit	R/W	Default	Description
31 - 17	R/W/L	0000h	**Remap PCI Space_3 (RMP3[15:1])** If PCI Space_3<0> is: 0: Access to the memory space defined in PCI Space_3 will be remapped to the space of {A[31:20]=ignore, A[19:6]=RMP1[15:2], A[5:0]= same} if the space claimed is not greater than 64 bytes; otherwise {A[31:20]=ignore, A[19:(Size_bit +1)]=RMP1[15: (Size_bit – 3)], A[Size_bit:0]= same} where the Size_bit depends on the PCI Space_3 size. 1: Access to the I/O space defined in PCI Space_3 will be remapped to the space of {A[31:16]=ignore, A[15:1]=RMP3[15:1], A[Size_bit:0]=same} where the Size_bit depends on the PCI Space_3 size.
16	R/W/L		**Enable Remap PCI Space_3 (RMP3_En)** 0: Disable remapping. 1: Enable remapping.
15 - 1	R/W/L	0000h	**Remap PCI Space_2 (RMP2[15:1])** If PCI Space_2<0> is: 0: Access to the memory space defined in PCI Space_2 will be remapped to the space of {A[31:20]=ignore, A[19:6]=RMP1[15:2], A[5:0]= same} if the space claimed is not greater than 64 bytes; otherwise {A[31:20]=ignore, A[19:(Size_bit +1)]=RMP1[15: (Size_bit – 3)], A[Size_bit:0]= same} where the Size_bit depends on the PCI Space_2 size. 1: Access to the I/O space defined in PCI Space_2 will be remapped to the space of {A[31:16]=ignore, A[15:1]=RMP2[15:1], A[Size_bit:0]=same} where the Size_bit depends on the PCI Space_2 size.
0	R/W/L		**Enable Remap PCI Space_2 (RMP2_En)** 0: Disable remapping. 1: Enable remapping.

9.3.17 PCI Space_5/4 Remap Register (RMP54R) – Offset 58h

Bit	R/W	Default	Description
31 - 17	R/W/L	0000h	**Remap PCI Space_5 (RMP5[15:1])** If PCI Space_5<0> is: 0: Access to the memory space defined in PCI Space_5 will be remapped to the space of {A[31:20]=ignore, A[19:6]=RMP1[15:2], A[5:0]= same} if the space claimed is not greater than 64 bytes; otherwise {A[31:20]=ignore, A[19:(Size_bit +1)]=RMP1[15: (Size_bit – 3)], A[Size_bit:0]= same} where the Size_bit depends on the PCI Space_5 size. 1: Access to the I/O space defined in PCI Space_5 will be remapped to the space of {A[31:16]=ignore, A[15:1]=RMP5[15:1], A[Size_bit:0]=same} where the Size_bit depends on the PCI Space_5 size.
16	R/W/L		**Enable Remap PCI Space_5 (RMP5_En)** 0: Disable remapping. 1: Enable remapping.
15 - 1	R/W/L	0000h	**Remap PCI Space_4 (RMP4[15:1])** If PCI Space_4<0> is: 0: Access to the memory space defined in PCI Space_4 will be remapped to the space of {A[31:20]=ignore, A[19:6]=RMP1[15:2], A[5:0]= same} if the space claimed is not greater than 64 bytes; otherwise {A[31:20]=ignore, A[19:(Size_bit +1)]=RMP1[15: (Size_bit – 3)], A[Size_bit:0]= same} where the Size_bit depends on the PCI Space_4 size. 1: Access to the I/O space defined in PCI Space_4 will be remapped to the space of {A[31:16]=ignore, A[15:1]=RMP4[15:1], A[Size_bit:0]=same} where the Size_bit depends on the PCI Space_4 size.
0	R/W/L		**Enable Remap PCI Space_4 (RMP4_En)** 0: Disable remapping. 1: Enable remapping.

9.3.18 Positively Decoded I/O_Space_0 Register (POSIO0R) – Offset 60h

Bit	R/W	Default	Description
31	R/W/L	0b	**I/O_Space_0 Enable (IO_0_EN)** 0: No response. 1: IT8875F will respond to I/O_Space_0.
30 - 29	R/W/L	00b	**Decoding Speed for I/O_Space_0 (IO_0_Speed[1:0])** 00b: Reserved; 10b: Medium speed; 01b: Slow speed; 11b: Fast speed.
28	R/W/L	0b	**Alias Enable for I/O_Space_0 (Alias_0_EN)** 0: Fully decode. 1: Don't care A[15:10].
27	RO	0b	**Reserved**
26 - 24	R/W/L	000b	**I/O_Space_0 Size (IO_0_Size[2:0])** 000b: 1 bytes; 010b: 4 bytes; 100b: 16 bytes; 110b: 64 bytes; 001b: 2 bytes; 011b: 8 bytes; 101b: 32 bytes; 111b: 128 bytes.
23 - 16	RO	00h	**Reserved**
15 - 0	R/W/L	0000h	**Base Address of I/O_Space_0 (IO_0_BA[15:0])** A[15:0], with A[31:16]=0000h.

9.3.19 Positively Decoded I/O_Space_1 Register (POSIO1R) – Offset 64h

Bit	R/W	Default	Description
31	R/W/L	0b	**I/O_Space_1 Enable (IO_1_EN)** 0: No response. 1: IT8875F will respond to I/O_Space_1.
30 - 29	R/W/L	00b	**Decoding Speed for I/O_Space_1 (IO_1_Speed[1:0])** 00b: Reserved; 10b: Medium speed; 01b: Slow speed; 11b: Fast speed.
28	R/W/L	0b	**Alias Enable for I/O_Space_1 (Alias_1_EN)** 0: Fully decode. 1: Don't care A[15:10].
27	RO	0b	**Reserved**
26 - 24	R/W/L	000b	**I/O_Space_1 Size (IO_1_Size[2:0])** 000b: 1 bytes; 010b: 4 bytes; 100b: 16 bytes; 110b: 64 bytes; 001b: 2 bytes; 011b: 8 bytes; 101b: 32 bytes; 111b: 128 bytes.
23 - 16	RO	00h	**Reserved**
15 - 0	R/W/L	0000h	**Base Address of I/O_Space_1 (IO_1_BA[15:0])** A[15:0], with A[31:16]=0000h.

9.3.20 Positively Decoded I/O_Space_2 Register (POSIO2R) – Offset 68h

Bit	R/W	Default	Description
31	R/W/L	0b	**I/O_Space_2 Enable (IO_2_EN)** 0: No response. 1: IT8875F will respond to I/O_Space_2.
30 - 29	R/W/L	00b	**Decoding Speed for I/O_Space_2 (IO_2_Speed[1:0])** 00b: Reserved; 10b: Medium speed; 01b: Slow speed; 11b: Fast speed.
28	R/W/L	0b	**Alias Enable for I/O_Space_2 (Alias_2_EN)** 0: Fully decode. 1: Don't care A[15:10].
27	RO	0b	**Reserved**
26 – 24	R/W/L	000b	**I/O_Space_2 Size (IO_2_Size[2:0])** 000b: 1 bytes; 010b: 4 bytes; 100b: 16 bytes;110b: 64 bytes; 001b: 2 bytes; 011b: 8 bytes; 101b: 32 bytes;111b: 128 bytes.
23 – 16	RO	00h	**Reserved**
15 – 0	R/W/L	0000h	**Base Address of I/O_Space_2 (IO_2_BA[15:0])** A[15:0], with A[31:16]=0000h.

9.3.21 Positively Decoded I/O_Space_3 Register (POSIO3R) – Offset 6Ch

Bit	R/W	Default	Description
31	R/W/L	0b	**I/O_Space_3 Enable (IO_3_EN)** 0: No response. 1: IT8875F will respond to I/O_Space_3.
30 - 29	R/W/L	00b	**Decoding Speed for I/O_Space_3 (IO_3_Speed[1:0])** 00b: Reserved; 10b: Medium speed; 01b: Slow speed; 11b: Fast speed.
28	R/W/L	0b	**Alias Enable for I/O_Space_3 (Alias_3_EN)** 0: Fully decode. 1: Don't care A[15:10].
27	RO	0b	**Reserved**
26 - 24	R/W/L	000b	**I/O_Space_3 Size (IO_3_Size[2:0])** 000b: 1 bytes; 010b: 4 bytes; 100b: 16 bytes;110b: 64 bytes; 001b: 2 bytes; 011b: 8 bytes; 101b: 32 bytes;111b: 128 bytes.
23 - 16	RO	00h	**Reserved**
15 - 0	R/W/L	0000h	**Base Address of I/O_Space_3 (IO_3_BA[15:0])** A[15:0], with A[31:16]=0000h.

9.3.22 Positively Decoded I/O_Space_4 Register (POSIO4R) – Offset 70h

Bit	R/W	Default	Description
31	R/W/L	0b	**I/O_Space_4 Enable (IO_4_EN)** 0: No response. 1: IT8875F will respond to IO_Space_4.
30 - 29	R/W/L	00b	**Decoding Speed for I/O_Space_4 (IO_4_Speed[1:0])** 00b: Reserved; 10b: Medium speed; 01b: Slow speed; 11b: Fast speed.
28	R/W/L	0b	**Alias Enable for I/O_Space_4 (Alias_4_EN)** 0: Fully decode. 1: Don't care A[15:10].
27	RO	0b	**Reserved**
26 - 24	R/W/L	000b	**I/O_Space_4 Size (IO_4_Size[2:0])** 000b: 1 bytes; 010b: 4 bytes; 100b: 16 bytes; 110b: 64 bytes; 001b: 2 bytes; 011b: 8 bytes; 101b: 32 bytes; 111b: 128 bytes.
23 - 16	RO	00h	**Reserved**
15 - 0	R/W/L	0000h	**Base Address of I/O_Space_4 (IO_4_BA[15:0])** A[15:0], with A[31:16]=0000h.

9.3.23 INTC Base Address Register (INTCBAR) – Offset 78h

Bit	R/W	Default	Description
31 - 16	-	-	**Reserved**
15 - 0	R/W/L	02A0h	**INTC Base Address (INTC_BA[15:0])** This value specifies the INTC Base Address (16-bytes space).

9.3.24 Internal Parallel Port Base Address Register (IPPBAR) – Offset 80h

Bit	R/W	Default	Description
31 - 16	R/W/L	0778h	**Internal Parallel Port Base Address for ECP Mode (IPPH_BA[15:0])** The last two bits are not used.
15 - 0	R/W/L	0378h	**Internal Parallel Port Base Address for SPP/EPP Mode (IPPL_BA[15:0])** The last two bits are not used.

9.3.25 External Devices Base Address Register 1 (XDBA1R) – Offset 88h

Bit	R/W	Default	Description
31 - 16	RO	01A0h	**Reserved**
15 - 0	R/W/L	0180h	**External CSA[3:0]# Base Address(CSA_BA[15:0])** Each one of CSA[3:0]# spaces is 8 bytes, and the CSA_BA[2:0] are not used in address comparator. The CSA_BA[0] is recommended to set to 0. **Active Signal** — **Address Region** CSA[0]# — CSA_BA[15:0] to CSA_BA[15:0]+7h CSA[1]# — CSA_BA[15:0]+8h to CSA_BA[15:0]+15h CSA[2]# — CSA_BA[15:0]+16h to CSA_BA[15:0]+23h CSA[3]# — CSA_BA[15:0]+24h to CSA_BA[15:0]+31h

9.3.26 Miscellaneous Control Register (MISCR) – Offset 9Ch

Bit	R/W	Default	Description
31 – 30	R/W/L	11b	**Internal Parallel Port Operation Mode (IPP_Mode[1:0])** 00: SPP; 01: SPP & EPP 10: SPP & ECP 11: SPP, EPP & ECP
29 – 27	RO	011b	**Reserved**
26 - 24	RO	001b	**Reserved**
23 - 22	RO	00b	**Reserved**
21	R/W/L	0b	**Internal Parallel Port Function Enable Control (IPP_En)** 0: Disabled. 1: Enabled.
20	R/W/L	0	**Writes To Auto Addressing Enable Control (WTAA_En)** 0: Disabled. 1: Enabled. If this bit is enabled, IT8875 would allow PCI configuration read/write to configuration space address 10h, 14h, 18h, 1Ch, 20h, 24h, 30h to control the size registers corresponding to the normal base address register (if this bit is disabled). If this bit is 1, it indicates the corresponding base address register is read/write; otherwise it is read only. If this bit is disabled, PCI configuration read/write operations will access the configuration space address 10h, 14h, 18h, 1Ch, 20h, 24h, 30h to read/write the real PCI base address registers. This bit is for IC verification usage only, and is not intended for the real application.
19 - 16	RO	0101b	**Reserved**
15 - 12	RO	0100b	**Reserved**
11 - 8	RO	0011b	**Reserved**
7 – 4	R/W/L	0111b	**Internal Parallel Port Interrupt Routing Register to SERIRQ Slot (IPP_Routing[3:0])** 0000, 1101: No interrupt; 0001: IRQ1 slot; 0010: SMI# slot; 0011-1100: IRQ3-IRQ12 slots; 1110-1111: IRQ14-IRQ15 slots.
3 - 0	RO	1010b	**Reserved**

9.3.27 Undefined Register

Bit	R/W	Default	Description
31 - 0	RO	00000000h	**Reserved**

10. Interrupt Controller (INTC)

The interrupts are issued from the modules of internal Parallel port, GPIO and ISA interrupts. Users can route the internal Parallel port, GPIO and one ISA interrupt (pin IRQ0) to the corresponding interrupt. After the host detects the interrupt, it reads the interrupt request register to check which module generated the interrupt. As the controller provides the feature of gathering interrupts from all modules into one register, it will help to simplify the interrupt processing.

10.1 Features

- All interrupts issued from the internal modules are gathered into one register
- Only one external interrupt output pin INTA# is used to request the interrupt service
- Interrupt request lines from each module are high active, and the trigger modes could be set as edge or level mode. For IRQ0, the software interrupt bit of IRQ0 is used to XOR with the input to generate the real interrupt to generate the high active signal to the interrupt module
- Each module provides an interrupt mask bit. An interrupt mask register, which is able to perform masking for each module interrupt, is also included

10.2 Block Diagram

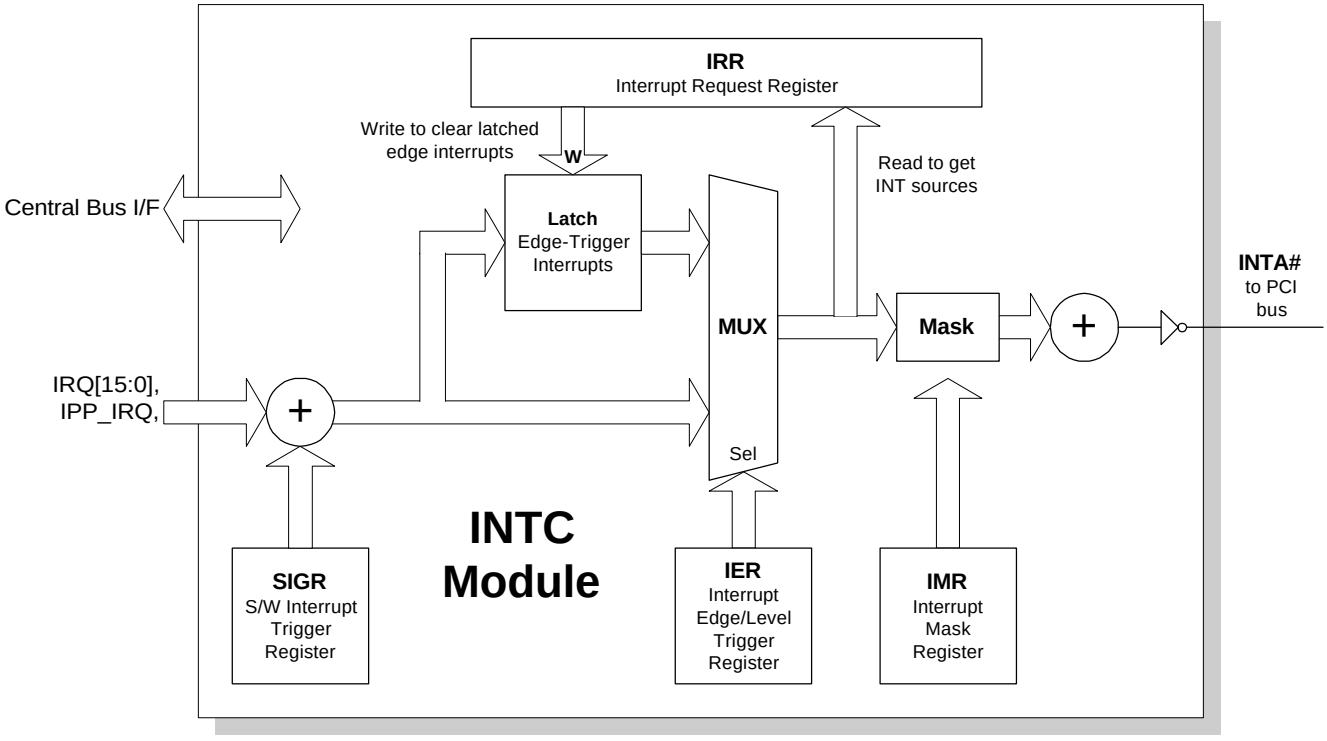


Figure 10-1. Block Diagram of the Interrupt Controller

10.3 Register Descriptions

Table 10-1. List of INTC Registers

Name	Address	Register Size	Access Size
Interrupt Request Registers (IRR)	INTC_Base + 0~2h	3	1
Interrupt Mask Registers (IMR)	INTC_Base + 4~6h	3	1
Interrupt Trigger Mode (Edge/Level) Registers (IER)	INTC_Base + 8~Ah	3	1
S/W Interrupt Trigger Registers (ITR)	INTC_Base + C~Eh	3	1

10.3.1 Interrupt Request Register 1 (IRR1R) – Offset INTC_Base + 0h

Bit	R/W	Default	Description
7 - 0	R/W1C	00h	**External IRQ[7:0] Status (Status_IRQ[7:0])** 0: No interrupts request. 1: Interrupt in service or pending.

10.3.2 Interrupt Request Register 2 (IRR2R) – Offset INTC_Base + 1h

Bit	R/W	Default	Description
7 – 0	R/W1C	00h	**External IRQ[15:8] Status (Status_IRQ[15:8])** 0: No interrupts request. 1: Interrupt in service or pending.

10.3.3 Interrupt Request Register 3 (IRR3R) – Offset INTC_Base + 2h

Bit	R/W	Default	Description
7 - 4	RO	0000b	**Reserved.**
3	R/W1C	0b	**Reserved**
2	R/W1C	0b	**Reserved**
1	R/W1C	0b	**Internal Parallel Port Interrupt Request Status (Status_IPP)** 0: No IPP interrupt request. 1: IPP interrupt in service or pending.
0	R/W1C	0b	**GPIO Interrupt Request Status (Status_GPIO)** 0: No GPIO interrupt request. 1: GPIO interrupt in service or pending.

10.3.4 Interrupt Mask Register 1 (IMR1R) – Offset INTC_Base + 4h

Bit	R/W	Default	Description
7 - 0	R/W	00h	**External IRQ[7:0] Mask (Mask_IRQ[7:0])** 0: Interrupts is unmasked. 1: Interrupt is masked.

10.3.5 Interrupt Mask Register 2 (IMR2R) – Offset INTC_Base + 5h

Bit	R/W	Default	Description
7 - 0	R/W	00h	**External IRQ[15:8] Mask (Mask_IRQ[15:8])** 0: Interrupts is unmasked. 1: Interrupt is masked.

10.3.6 Interrupt Mask Register 3 (IMR3R) – Offset INTC_Base + 6h

Bit	R/W	Default	Description
7 - 4	RO	0000b	**Reserved**
3	R/W	0b	**Reserved**
2	R/W	0b	**Reserved**
1	R/W	0b	**Internal Parallel Port Interrupt Mask (Mask_IPP)** 0: IPP interrupt is unmasked. 1: IPP interrupt is masked.
0	R/W	0b	**Reserved**

10.3.7 Interrupt Edge/Level Trigger Mode Register 1 (IER1R) – Offset INTC_Base + 8h

Bit	R/W	Default	Description
7 - 0	R/W	00h	**External IRQ[7:0] Interrupt Trigger Mode (Edge_IRQ[7:0])** 0: Interrupt is Edge Trigger. 1: Interrupt is Level Trigger.

10.3.8 Interrupt Edge/Level Trigger Mode Register 2 (IER2R) – Offset INTC_Base + 9h

Bit	R/W	Default	Description
7 - 0	R/W	00h	**External IRQ[15:8] Interrupt Trigger Mode (Edge_IRQ[15:8])** 0: Interrupt is Edge Trigger. 1: Interrupt is Level Trigger.

10.3.9 Interrupt Edge/Level Trigger Mode Register 3 (IER3R) – Offset INTC_Base + Ah

Bit	R/W	Default	Description
7 - 4	RO	0000b	**Reserved**
3	R/W	0b	**Reserved**
2	R/W	0b	**Reserved**
1	R/W	0b	**Internal Parallel Port Interrupt Trigger Mode (Edge_IPP)** 0: IPP interrupt is Edge Trigger. 1: IPP interrupt is Level Trigger.
0	R/W	0b	**Reserved**

10.3.10 S/W Interrupt Generate Register 1 (SIGR1R) – Offset INTC_Base + Ch

Bit	R/W	Default	Description
7 - 0	R/W	00h	**Generate S/W interrupt on IRQ[7:0] Path (SW_IRQ[7:0])** 0: No S/W Iinterrupt. 1: Generate S/W interrupt.

10.3.11 S/W Interrupt Generate Register 2 (SIGR2R) – Offset INTC_Base + Dh

Bit	R/W	Default	Description
7 - 0	R/W	00h	**Generate S/W interrupt on IRQ[15:8] Path (SW_IRQ[15:8])** 0: No S/W Interrupt. 1: Generate S/W interrupt.

10.3.12 S/W Interrupt Generate Register 3 (SIGR3R) – Offset INTC_Base + Eh

Bit	R/W	Default	Description
7 - 4	RO	0000b	**Reserved**
3	R/W	0b	**Reserved**
2	R/W	0b	**Reserved**
1	R/W	0b	**Generate S/W Interrupt on Path IPP Interrupt Path (SW_IPP)** 0: No S/W interrupt. 1: Generates S/W interrupt.
0	R/W	0b	**Reserved**

11. Parallel Port

11.1 Overview

The IT8875F incorporates one multi-mode high performance parallel port, which supports the IBM AT, PS/2 compatible bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP). Please refer to the IT8875F Configuration registers and Configuration Description for information on enabling/ disabling, changing the base address of the parallel port, and selecting the mode of operation.

Table 11-1. Parallel Port Connector in Different Modes

Host Connector	Pin No.	SPP	EPP	ECP
1	76	STB#	WRITE#	nStrobe
2-9	71-68,66-63	PD0 - 7	PD0 - 7	PD0 - 7
10	62	ACK#	INTR	nAck
11	61	BUSY	WAIT#	Busy PeriphAck(2)
12	60	PE	(NU) (1)	PError nAckReverse(2)
13	59	SLCT	(NU) (1)	Select
14	77	AFD#	DSTB#	nAutoFd HostAck(2)
15	75	ERR#	(NU) (1)	nFault nPeriphRequest(2)
16	73	INIT#	(NU) (1)	nInit nReverseRequest(2)
17	74	SLIN#	ASTB#	nSelectIn

Notes: 1. NU: Not used
2. Fast mode
3. For more information, please refer to the IEEE 1284 standard.

11.2 SPP and EPP Modes

Table 11-2. Address Map and Bit Map for SPP and EPP Modes

Register	Address	I/O	D0	D1	D2	D3	D4	D5	D6	D7	Mode
Data Port	Base 1+0H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	SPP/EPP
Status Port	Base 1+1H	RO	TMOUT	1	1	ERR#	SLCT	PE	ACK#	BUSY#	SPP/EPP
Control Port	Base 1+2H	R/W	STB	AFD	INIT	SLIN	IRQE	PDDIR	1	1	SPP/EPP
EPP Address Port	Base 1+3H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port0	Base 1+4H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port1	Base 1+5H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port2	Base 1+6H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP
EPP Data Port3	Base 1+7H	R/W	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	EPP

Note 1. The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

(1) Data Port (Base Address 1 + 00h)

This is a bi-directional 8-bit data port. The direction of data flow is determined by the bit 5 of the logic state of the control port register. It forwards directions when the bit is low and reverses when the bit is high.

(2) Status Port(Base Address 1 + 01h)

This is a read only register. Writing to this register has no effects. The contents of this register are latched during an IOR cycle.

Bit 7 - BUSY#: Inverse of printer BUSY signal, a logic "0" means that the printer is busy and cannot accept another character. A logic "1" means that it is ready to accept the next character.
Bit 6 - ACK#: Printer acknowledge, a logic "0" means that the printer has received a character and is ready to accept another. A logic "1" means that it is still processing the last character.
Bit 5 - PE: Paper end, a logic "1" indicates the paper end.
Bit 4 - SLCT: Printer selected, a logic "1" means that the printer is on line.
Bit 3 - ERR#: Printer error signal, a logic "0" means an error has been detected.
Bits 1, 2: Reserved, these bits are always "1" when read.
Bit 0 - TMOUT: This bit is valid only in EPP mode and indicates that a 10-msec timeout has occurred in EPP operation. A logic "0" means no timeout occurred and a logic 1 means that a timeout error has been detected. This bit is cleared by a LRESET# or by writing a logic "1" to it. When the IT8875F is selected to non-EPP mode (SPP or ECP), this bit is always logic "a" when read.

(3) Control Port (Base Address 1 + 02h)

This port provides all output signals to control the printer. The register can be read and written.
Bits 6, 7: Reserved, these two bits are always "1" when read.
Bit 5 PDDIR: Data port direction control, this bit determines the direction of the data port. Set this bit "0" to output the data port to PD bus and "1" to input from PD bus.
Bit 4 IRQE: Interrupt request enable, setting this bit "1" enables the interrupt requests from the parallel port to the Host. An interrupt request is generated by a "0" to "1" transition of the ACK# signal.
Bit 3 SLIN: Inverse of SLIN# pin, setting this bit to "1" selects the printer.
Bit 2 INIT: Initiate printer, setting this bit to "0" initializes the printer.
Bit 1 AFD: Inverse of the AFD# pin, setting this bit to "1" causes the printer to automatically feed after each line is printed.
Bit 0 STB: Inverse of the STB# pin. This pin controls the data strobe signal to the printer.

(4) EPP Address Port (Base Address 1 + 03h)

The EPP Address Port is only available in the EPP mode. When the Host writes to this port, the contents of D0 -D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when I/O WRITE cycle is on this address) causes an EPP ADDRESS WRITE cycle. When the Host reads from this port, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when I/O read cycle is on this address) causes an EPP ADDRESS read cycle.

(5) EPP Data Ports 0-3 (Base Address 1 + 04-07h)

The EPP Data Ports are only available in the EPP mode. When the Host writes to these ports, the contents of D0 - D7 are buffered and output to PD0 - PD7. The leading edge of IOW (Internal signal, active when I/O WRITE cycle is on this address) causes an EPP DATA WRITE cycle. When the Host reads from these ports, the contents of PD0 - PD7 are read. The leading edge of IOR (Internal signal, active when I/O read cycle is on this address) causes an EPP DATA read cycle.

11.3 EPP Mode Operation

When the parallel port of the IT8875F is set in the EPP mode, the SPP mode is also available. If no EPP Address/Data Port address is decoded (Base address + 03h- 07h), the PD bus is in the SPP mode, and the output signals such as STB#, AFD#, INIT#, and SLIN# are set by the SPP control port. The direction of the data port is controlled by the bit 5 of the control port register. There is a 10-msec time required to prevent the system from lockup. The time has elapsed from the beginning of the IOCHRDY (Internal signal: When active, the IT8875F will issue Long Wait in SYNC field) high (EPP read/write cycle) to WAIT# being de-asserted. If a timeout occurs, the current EPP read/write cycle is aborted and a logic "1" will be read in the bit 0 of the status port register. The Host must write 0 to bits 0, 1, 3 of the control port register before any EPP read/write cycle (EPP spec.) The pins STB#, AFD# and SLIN# are controlled by hardware for the hardware handshaking during EPP read/write cycle.

(1) EPP ADDRESS WRITE

The Host writes a byte to the EPP Address Port (Base address + 03h). The chip drives D0 - D7 onto PD0 - PD7. The chip drives IOCHRDY low and asserts WRITE# (STB#) and ASTB# (SLIN#) after IOW becomes active.

Peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from D0 - D7 to PD bus and releases IOCHRDY, allowing the Host to complete the I/O WRITE cycle. Peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(2) EPP ADDRESS READ

The Host reads a byte from the EPP Address Port. The chip drives PD bus to tri-state for peripheral to drive. The chip drives IOCHRDY low and asserts ASTB# after IOR becomes active. Peripheral drives the PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts ASTB#, latches the address from PD bus to D0 -D7 and releases IOCHRDY, allowing the Host to complete the I/O read cycle. Peripheral drives the PD bus to tri-state and then asserts WAIT#, indicating that it acknowledges the termination of the cycle

(3) EPP DATA WRITE

The host writes a byte to the EPP Data Port (Base address +04H - 07H). The chip drives D0- D7 onto PD0 -PD7. The chip drives IOCHRDY low and asserts WRITE# (STB#) and DSTB (AFD#) after IOW becomes active.

Peripheral de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from D0 - D7 to the PD bus and releases IOCHRDY, allowing the Host to complete the I/O write cycle. Peripheral asserts WAIT#, indicating that it acknowledges the termination of the cycle. Then, the chip de-asserts WRITE to terminate the cycle.

(4) EPP DATA READ

The Host reads a byte from the EPP DATA Port. The chip drives PD bus to tri-state for peripheral to drive. The chip drives IOCHRDY low and asserts DSTB# after IOR becomes active. Peripheral drives PD bus valid and de-asserts WAIT#, indicating that the chip may begin the termination of this cycle. Then, the chip de-asserts DSTB#, latches the data from PD bus to D0 - D7 and releases IOCHRDY, allowing the host to complete the I/O read cycle. Peripheral tri-states the PD bus and then asserts WAIT#, indicating that it acknowledges the termination of the cycle.

11.4 ECP Mode Operation

This mode is both software and hardware compatible with that of the existing parallel ports, allowing ECP to be used as a standard LPT port when the ECP mode is not required. Due to the variation of system platform, DMA mode is **NOT** supported in IT8875 ECP mode, only PIO mode can be operated. A 16-byte FIFO is implemented in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The port supports automatic handshaking for the standard parallel port to improve compatibility and expedite the mode transfer. It also supports run-length encoded (RLE) decompression in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times a byte has been repeated. The IT8875F does not support hardware compression. For a detailed description, please refer to "Extended Capabilities Port Protocol and ISA Interface Standard".

Table 11-3. Bit Map of the ECP Registers

Register	D7	D6	D5	D4	D3	D2	D1	D0
Data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
EcpAFifo	Addr/RLE	Address or RLE field						
dsr	nBusy	nAck	PError	Select	NFault	1	1	1
dcr	1	1	PDDIR	IRQE	SelectIn	nInit	AutoFd	Strobe
CFifo	Parallel Port Data FIFO							
EcpDFifo	ECP Data FIFO							
TFifo	Test FIFO							
CnfgA	0	0	0	1	0	0	0	0
CnfgB	0	intrValue	0	0	0	0	0	0
ecr	mode			nErrIntrEn	0	ServiceIntr	full	empty

(1) ECP Register Definitions

Table 11-4. ECP Register Definitions

Name	Address	Attribute	ECP Mode	Function
data	Base 1 +000H	R/W	000-001	Data Register
ecpAFifo	Base 1 +000H	R/W	011	ECP FIFO (Address)
dsr	Base 1 +001H	R/W	All	Status Register
dcr	Base 1 +002H	R/W	All	Control Register
cFifo	Base 2 +000H	R/W	010	Parallel Port Data FIFO
ecpDFifo	Base 2 +000H	R/W	011	ECP FIFO (DATA)
tFifo	Base 2 +000H	R/W	110	Test FIFO
cnfgA	Base 2 +000H	RO	111	Configuration Register A
cnfgB	Base 2 +001H	R/W	111	Configuration Register B
ecr	Base 2 +002H	R/W	All	Extended Control Register

Notes 1: The Base address 1 depends on the Logical Device configuration registers of Parallel Port (0X60, 0X61).

2: The Base address 2 depends on the Logical Device configuration registers of Parallel Port (0X62, 0X63).

(2) ECP Mode Descriptions

Table 11-5. ECP Mode Descriptions

Mode	Description
000	Standard Parallel Port Mode
001	PS/2 Parallel Port Mode
010	Parallel Port FIFO Mode
011	ECP Parallel Port Mode
110	Test Mode
111	Configuration Mode

Note: Please refer to the ECP Register Description on pages 53-54 for a detailed description of the mode selection.

(3) ECP Pin Descriptions

Table 11-6. ECP Pin Descriptions

Name	Type	Description
nStrobe (HostClk)	O	Used for handshaking with Busy to write data and addresses into the peripheral device
PD0~PD7	I/O	Address or data or RLE data
nAck (PeriphClk)	I	Used for handshaking with nAutoFd to transfer data from the peripheral device to the Host.
Busy (PeriphACK)	I	The peripheral uses this signal for flow control in the forward direction (hand-shaking with nStrobe). In the reverse direction, this signal is used to determine whether a command or data information is present on PD0~PD7.
PError (nAckReverse)	I	Used to acknowledge nInit from the peripheral which drives this signal low, allowing the host to drive the PD bus.
Select	I	Printer On-Line indication
nAutoFd (HostAck)	O	In the reverse direction, it is used for handshaking between the nACK and the Host. When it is asserted, a peripheral data byte is requested. In the forward direction, this signal is used to determine whether a command or data information is present on PD0 ~ PD7.
nFault (nPeriphRequest)	I	In the forward direction (only), the peripheral is allowed (but not required) to assert this signal (low) to request a reverse transfer while in ECP mode. The signal provides a mechanism for peer-to-peer communication. It is typically used to generate an interrupt to host, which has the ultimate control over the transfer direction.
nInit (nReverseRequest)	O	The host may drive this signal low to place the PD bus in the reverse direction. In the ECP mode, the peripheral is permitted to drive the PD bus when nInit is low, and nSelect is high
nSelectIn (1284 Active)	O	Always inactive (high) in the ECP mode.

(4) Data Port (Base 1+00h, Modes 000 and 001)

Its contents will be cleared by a RESET. In a WRITE operation, the contents of the data fields are latched by the Data Register. The contents are then sent without being inverted to PD0~ PD7. In a read operation, the contents of data ports are read and sent to the host.

(5) ecpAFifo Port (Address/RLE) (Base 1 +00h, Mode 011)

Any data byte written to this port are placed in the FIFO and tagged as an ECP Address/RLE. The hardware then automatically sends this data to the peripheral. Operation of this port is valid only in the forward direction (dcr(5)=0).

(6) Device Status Register (dsr) (Base 1 +01h, Mode All)

Bits 0, 1 and 2 of this register are not implemented. These bit states are remained at high in a read operation of the Printer Status Register.

dsr(7): This bit is the inverted level of the Busy input.
dsr(6): This bit is the state of the nAck input.
dsr(5): This bit is the state of the PError input.
dsr(4): This bit is the state of the Select input.
dsr(3): This bit is the state of the nFault input.
dsr(2)~dsr(0): These bits are always 1.

(7) Device Control Register (dcr) (Base 1+02h, Mode All)

Bits 6 and 7 of this register have no function. They are set high during the read operation, and cannot be written. Contents in bits 0~5 are initialized to 0 when the RESET pin is active.

dcr(7)~dcr(6): These two bits are always high.
dcr(5): Except in the modes 000 and 010, setting this bit low means that the PD bus is in output operation; setting it high, in input operation. This bit will be forced to low in mode 000.
dcr(4): Setting this bit high enables the interrupt request from peripheral to the host due to a rising edge of the nAck input.
dcr(3): It is inverted and output to SelectIn.
dcr(2): It is output to nInit without inversion.
dcr(1): It is inverted and output to nAutoFd.
dcr(0): It is inverted and output to nStrobe.

(8) Parallel Port Data FIFO (cFifo) (Base 2+00h, Mode 010)

Bytes written to this FIFO are sent by a hardware handshake to the peripheral according to the standard parallel port protocol. This operation is only defined for the forward direction.

(9) ECP Data FIFO (ecpDFifo) (Base 2+00h, Mode 011)

When the direction bit dcr(5) is 0, bytes written to this FIFO are sent by hardware handshaking to the peripheral according to the ECP parallel port protocol. When dcr(5) is 1, data bytes from the peripheral to this FIFO are read in an automatic hardware handshaking. The Host can receive these bytes by performing read operations from this FIFO.

(10) Test FIFO (tFifo) (Base 2+00h, Mode 110)

The Host may operate read/write to this FIFO in any direction. Data in this FIFO will be displayed on the PD bus without using hardware protocol handshaking. The tFifo will not accept new data after it is full. Making a read from an empty tFifo causes the last data byte to be returned.

(11) Configuration Register A (cnfgA) (Base 2+00h, Mode 111)

This read only register indicates to the system that interrupts are ISA-Pulses compatible. This is an 8-bit implementation by returning a 10h.

(12) Configuration Register B (cnfgB) (Base 2+01h, Mode 111)

This register is read only.

cnfgB(7): Logic 0 read indicates that the chip does not support hardware RLE compression.
cnfgB(6): Reserved.
cnfgB(5)~cnfg(3): A value 000 read indicates that the interrupt must be selected with jumpers.
cnfgB(2)~cnfg(0): Reserved

(13) Extended Control Register (ecr) (Base 2+02h, Mode All)

ECP function control register.
ecr(7)~ecr(5): These bits are used for read/write and mode selection.

Table 11-7. Extended Control Register (ECR) Mode and Description

ECR	Mode and Description
000	Standard Parallel Port Mode. The FIFO is reset and the direction bit dcr(5) is always 0 (forward direction) in this mode.
001	PS/2 Parallel Port Mode. It is similar to the SPP mode, except that the dcr(5) is read/write. When dcr(5) is 1, the PD bus is tri-state. Reading the data port returns the value on the PD bus instead of the value of the data register.
010	Parallel Port Data FIFO Mode. This mode is similar to the 000 mode, except that the Host writes the data bytes to the FIFO. The FIFO data is then transmitted to the peripheral using the standard parallel port protocol automatically. This mode is only valid in the forward direction (dcr(5)=0).
011	ECP Parallel Port Mode. In the forward direction, bytes placed into the ecpDFifo and ecpAFifo are placed in a single FIFO and automatically transmitted to the peripheral under the ECP protocol. In the reverse direction, bytes are transmitted to the ecpDFifo from the ECP port.
100, 101	Reserved, not defined
110	Test mode. In this mode, the FIFO may be read from or written to, but it cannot be sent to peripheral.
111	Configuration mode. In this mode, the cnfgA and cnfgB registers are accessible at 0x400 and 0x401.

ecr(4): nErrIntrEn, READ/WRITE, Valid in ECP(011) Mode

1: Disable the interrupt generated on the asserting edge of the nFault input.
0: Enable the interrupt pulse on the asserting edge of the nFault. An interrupt pulse will be generated if nFault is asserted, or if this bit is written from 1 to 0 in the low-level nFault.
ecr(3): Reserved
ecr(2): ServiceIntr, READ/WRITE
1: Disable all service interrupts
0: Enable the service interrupts. This bit will be set to "1" by hardware when one of the three service interrupts has occurred.
Writing "1" to this bit will not generate an interrupt.

Case 1: dcr(5)=0
This bit is set to 1 (a service interrupt generated) whenever there are writeIntrThreshold or more bytes space free in the FIFO.

Case 2: dcr(5)=1
This bit is set to 1 (a service interrupt generated) whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.
ecr(1): full, read-only
1: The FIFO is full and cannot accept another byte.
0: The FIFO has at least 1 free data byte space.
ecr(0): empty, READ only
1: The FIFO is empty.
0: The FIFO contains at least 1 data byte.

(14) Mode Switching Operation

In programmed I/O control (mode 000 or 001), P1284 negotiation and all other tasks that happen before data is transferred is software-controlled. Setting mode to 011 or 010 will cause the hardware to perform an automatic control-line handshaking, transferring information between the FIFO and the ECP port.

From the mode 000 or 001, any other mode may be immediately switched to from another mode. To change direction, the mode must first be set to 001.

In the extended forward mode, the FIFO must be cleared and all the signals must be de-asserted before returning to mode 000 or 001. In ECP reverse mode, all data must be read from the FIFO before returning to mode 000 or 001. Usually, unneeded data is accumulated during ECP reverse handshaking, when the mode is changed during a data transfer. In such conditions, nAutoFd will be de-asserted regardless of the transfer state. To avoid bugs during handshaking signals, these guidelines must be followed.

(15) Software Operation (ECP)

Before the ECP operation can begin, it is first necessary for the Host to switch the mode to 000 in order to negotiate with the parallel port. During this process, the Host determines whether peripheral supports the ECP protocol.

After this negotiation is completed, the mode is set to 011 (ECP). To enable the drivers, direction must be set to 0. Both strobe and autoFd are set to 0, causing nStrobe and nAutoFd signals to be de-asserted.

All FIFO data transfers are PWord wide and PWord aligned. Permitted only in the forward direction, address/RLE transfers are byte-wide. The ECP address/RLE bytes may be automatically sent by writing to the ecpAFifo. Similarly, data PWords may be automatically sent via the ecpDFifo.

To change directions, the Host switches mode to 001. It then negotiates either the forward or reverse channel, sets direction to 1 or 0, and finally switches mode to 001. If the direction is set to 1, the hardware performs handshaking for each ECP data byte read, then tries to fill the FIFO. At this time, PWords may be read from the ecpDFifo while it retains data. It is also possible to perform the ECP transfers by handshaking with individual bytes under programmed control in mode = 001, or 000, even though this is a comparatively time-consuming approach.

(16) Interrupts

It is necessary to generate an interrupt when any of the following states are reached.

serviceIntr = 0, direction = 0, and the number of PWords in the FIFO is greater than or equal to writeIntrThreshold.

serviceIntr = 0, direction = 1, and the number of full PWords in the FIFO is greater than or equal to readIntrThreshold.

nErrIntrEn = 0 and nFault goes from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.

ackIntEn = 1. In current implementations of using existing parallel ports, the interrupt generated may be either edge or level type.

(17) Interrupt Driven Programmed I/O

It is also possible to use an interrupt-driven programmed I/O to execute either ECP or parallel port FIFOs. An interrupt will occur in the forward direction when serviceIntr is 0 and the number of free PWords in the FIFO is equal to or greater than writeIntrThreshold. If either of these conditions is not met, it may be filled with writeIntrThreshold PWords. An interrupt will occur in the reverse direction when serviceIntr is 0 and the number of available PWords in the FIFO is equal to readIntrThreshold. If it is full, the FIFO can be completely emptied in a single burst. If it is not full, only a number of PWords equal to readIntrThreshold may be read from the FIFO in a single burst. In the test mode, software can determine the values of writeIntrThreshold, readIntrThreshold, and FIFO depth while accessing the FIFO.

12. DC Characteristics

Absolute Maximum Ratings

Power Supply (V_{CC}) .....-0.3V to 3.6/6.0V

Input Voltage ..... -0.3V to VCC + 0.3V

Output Voltage..... -0.3V to VCC + 0.3V

Storage Temperature.....-40°C to 125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied, and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

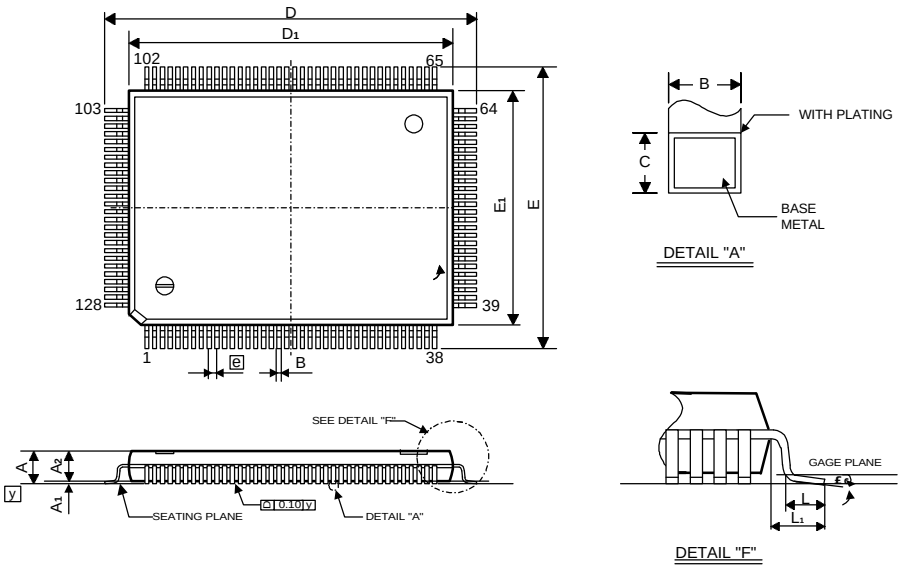
DC Electrical Characteristics (Operation Condition Vcc = 4.75V~5.25V, Vcc3=3.0V~3.6V, Tj=0°C~70°C)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{IL}	Input Low Voltage for 5V cell	TTL	-	-	0.8	V
V_{IL}	Input Low Voltage for 3.3V cell	CMOS	-	-	0.3*Vcc	V
V_{IH}	Input High Voltage for 5V cell	TTL	2.2	-	-	V
V_{IH}	Input High Voltage for 3.3V cell	CMOS	0.7*Vcc	-	-	V
Vt-	Schmitt trigger negative going threshold voltage	TTL	-	1.10	-	V
Vt+	Schmitt trigger positive going threshold voltage	TTL	-	1.90	-	V
V_{OL}	Output Low Voltage		-	-	0.4	V
V_{OH}	Output High Voltage for 5V cell (for all Parallel Port outputs)	TTL	2.4	-	-	V
V_{OH}	Output High Voltage for 5V cell		3.5	-	-	V
V_{OH}	Output High Voltage for 3.3V cell		2.3	-	-	V
Rl	Input Pull-up resistance	V_{IL}=0V or V_{IH}=Vcc	-	50	-	KΩ
I_{IL}	Input Leakage current	no pull-up	-1	-	1	μA
I_{OZ}	Tri-state leakage current		-1	-	1	mA
C_{IN}	Input capacity		-	5	-	pF
COUT	Output capacity		-	10	-	pF
CBID	Bi-directional buffer capacity		-	10	-	pF

13. Package Information

PQFP 128L Outline Dimensions

unit: inches/mm



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.134	-	-	3.40
A1	0.010	-	-	0.25	-	-
A2	0.107	0.112	0.117	2.73	2.85	2.97
B	0.007	0.009	0.011	0.17	0.22	0.27
C	0.004	-	0.008	0.09	-	0.20
D	0.906	0.913	0.921	23.00	23.20	23.40
D_1	0.783	0.787	0.791	19.90	20.00	20.10
E	0.669	0.677	0.685	17.00	17.20	17.40
E_1	0.547	0.551	0.555	13.90	14.00	14.10
e	0.020 BSC			0.5 BSC		
L	0.029	0.035	0.041	0.73	0.88	1.03
L_1	0.063 BSC			1.60 BSC		
y	-	-	0.004	-	-	0.10
θ	0¢ X	-	7¢ X	0¢ X	-	7¢ X

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion, but mold mismatch is included.
2. Dimension B does not include dambar protrusion.
3. Controlling dimension: millimeter.

14. Ordering Information

Part No.	Package
IT8875F	128 PQFP