19-0690; Rev 0; 1/07

Dual Driver/Comparator/Load with Internal DACs

General Description

The MAX9973/MAX9974 fully integrated, high-performance, dual-channel pin electronics driver/comparator/load (DCL) with built-in level-setting digital-to-analog converters (DACs) are ideally suited for memory and SOC automatic test equipment (ATE) applications. Each channel includes a three-level pin driver, a window comparator, dynamic clamps, a 1kΩ load, and seven independent level-setting DACs.

The driver features a wide voltage range and high-speed operation, includes high-impedance and active-termination (3rd-level drive) modes, and is highly linear even at low voltage swings. Additionally, the driver provides high-speed differential multiplexer control inputs, with internal termination resistors that are compatible with ECL, LVPECL, LVDS, and GTL. The window comparators provide extremely low timing variation over changes in slew rate, pulse width, or overdrive voltage, and have open-collector outputs. When high-impedance mode is selected, the dynamic clamps provide damping of high-speed device-under-test (DUT) waveforms. The load facilitates fast contact testing when used in conjunction with the comparators, and functions as a pullup for open-drain/collector DUT_ outputs. The MAX9973/MAX9974 are configured through a serial interface.

The MAX9973/MAX9974 differ in two aspects: the position of the exposed heat slug and the pin arrangement. The MAX9973G/MAX9974G comparator outputs sink 8mA (typ), while the MAX9973H/MAX9974H comparator outputs sink 16mA (typ). The devices are available in a 64-pin (10mm x 10mm x 1.00mm) TQFP-EP package with an exposed paddle on top (MAX9973) or bottom (MAX9974) for heat removal. Power dissipation is only 700mW per channel. The full operating voltage range is -1.5V to +6.5V. Operation is specified at an internal die temperature of +40°C to +100°C, and features a temperature monitor output.

Applications

Memory Testers

SOC Testers

SPI is a trademark of Motorola Inc.

Features

- ♦ **600Mbps at 3V High Speed**
- ♦ **700mW per Channel Extremely Low Power Dissipation**
- ♦ **-1.5V to +6.5V Wide Voltage Range**
- ♦ **200mV to 8V Wide Voltage Swing Range**
- ♦ **10nA (max) Low-Leakage Mode**
- ♦ **Integrated Termination On-the-Fly (3rd-Level Drive)**
- ♦ **Integrated Voltage Clamps**
- ♦ **Passive Load or Pullup**
- ♦ **Very Low Timing Dispersion**
- ♦ **Minimal External Component Count**
- ♦ **SPI™-Compatible Serial Control Interface**

Ordering Information

PART	PIN-PACKAGE	PKG CODE	OUTPUT SINK CURRENT
MAX9973GCCB	64 TQFP-EP-IDP** (10mm x 10mm x 1.00mm)	C64E-13R	8mA
MAX9973HCCB*	64 TQFP-EP-IDP** (10mm x 10mm x 1.00mm)	C64E-13R	16mA
MAX9974GCCB*	64 TQFP-EP† (10mm x 10mm x 1.00mm)	—	8mA
MAX9974HCCB*	64 TQFP-EP† (10mm x 10mm x 1.00mm)	—	16mA

Note: *Devices are available in both leaded and lead-free packages. Specify lead free by adding a + symbol at the end of the part number when ordering.*

**Future product—contact factory for availability.*

***EP-IDP = Exposed paddle (inverted die paddle).*

†EP = Exposed paddle.

Pin Configuration appears at end of data sheet.

Dual Driver/Comparator/Load with Internal DACs

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +11V
V_{EE} to GND.....-6V to +0.3V
V_{CC} - V_{EE}.....-0.3V to +17V
V_{DD} to GND .....-0.3V to +5V
V_{T0}, V_{T1} to GND .....-0.3V to +5V
DGS to GND .....±0.7V
DUT_ to GND.....-2.5V to +7.5V
DATA_, NDATA_, RCV_, NRCV_ to GND .....-2.5V to +5V
DATA_ to NDATA_, RCV_ to NRCV_ .....±1V
DATA_, NDATA_, RCV_, NRCV_ to VTERM_.....±1.5V
SCLK, DIN, $\overline{CS}$, $\overline{RST}$, $\overline{LOAD}$ to GND .....-0.3V to (V_{DD} + 0.3V)
TEMP to GND .....-0.2V to +5V
All Other Pins to GND .....(V_{EE} - 0.3V) to (V_{CC} + 0.3V)
DUT_ Short Circuit to -1.5V to +6.5V.....Continuous
Power Dissipation (T_A = +70°C)
MAX997_GCCB (derate 125mW/°C above +70°C).....10.0W*
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

**Dissipation wattage values are based on still air with no heat sink. Actual maximum power dissipation is a function of heat extraction technique and may be substantially higher.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER						
DC CHARACTERISTICS (R_L ≥ 10MΩ, unless otherwise noted; includes DAC error)						
Output Voltage Range	$V_{DHV\_}$	$V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = +1.5V	-1.45		+6.50	V
	$V_{DLV\_}$	$V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = +1.5V	-1.50		+6.45	
	$V_{DTV\_}$	$V_{DHV\_}$ = +6.5V, $V_{DLV\_}$ = -1.5V	-1.50		+6.50	
Output Offset Voltage	$V_{DHV\_}$	$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = +1.5V			±50	mV
	$V_{DLV\_}$	$V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = +1.5V			±50	
	$V_{DTV\_}$	$V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +6.5V, $V_{DLV\_}$ = -1.5V			±50	
Output-Voltage Temperature Coefficient (Notes 2, 3)		DHV_, DLV_, DTV_		±75	±400	µV/°C
Gain	$V_{DHV\_}$	$V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = 0 and +4.5V	0.998	1	1.002	V/V
	$V_{DLV\_}$	$V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0 and +4.5V	0.998	1	1.002	
	$V_{DTV\_}$	$V_{DHV\_}$ = +6.5V, $V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = 0 and +4.5V	0.998	1	1.002	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Linearity Error		0 to 3V relative to calibration points at 0 and 3V	$V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = 0, +0.75V, +1.5V, +2.25V, +3V			±5	mV
			$V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0, +0.75V, +1.5V, +2.25V, +3V			±5	
			$V_{DLV\_}$ = -1.5V, $V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = 0, +0.75V, +1.5V, +2.25V, +3V			±5	
		Full range relative to calibration points at 0 and 3V	$V_{DLV\_}$ = -1.5V, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = -1.25V and +6.5V			±5	
			$V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V and +6.25V			±5	
			$V_{DLV\_}$ = -1.5V, $V_{DHV\_}$ = +6.5V, $V_{DTV\_}$ = -1.5V and +6.5V			±5	
Crosstalk		$V_{DHV\_}$ to V_{DLV}, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, $V_{DHV\_}$ = 0.2V and 6.5V				±2	mV
		$V_{DLV\_}$ to V_{DHV}, $V_{DHV\_}$ = +5V, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = -1.5V and +4.8V				±2	
		$V_{DTV\_}$ to $V_{DLV\_}$ and V_{DHV}, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = -1.5V and +6.5V				±2	
		$V_{DHV\_}$ to V_{DTV}, $V_{DTV\_}$ = +1.5V, $V_{DLV\_}$ = 0, $V_{DHV\_}$ = +1.6V and +3.0V				±3	
		$V_{DLV\_}$ to V_{DTV}, $V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0 and +1.4V				±3	
Term Voltage Dependence on DATA_		$V_{DTV\_}$ = +1.5V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, DATA_ = 0 and 1				±2	mV
DC Power-Supply Rejection		$V_{DHV\_}$, $V_{DHV\_}$ = 3V, V_{CC} and V_{EE} independently varied over full range		40			dB
		$V_{DLV\_}$, $V_{DLV\_}$ = 0, V_{CC} and V_{EE} independently varied over full range		40			
		$V_{DTV\_}$, $V_{DTV\_}$ = 1.5V, V_{CC} and V_{EE} independently varied over full range		40			
DC Drive Current Limit		$V_{DLV\_}/V_{DUT\_}$ = -1.5V/+6.5V, DATA_ = 0		-120		-60	mA
		$V_{DHV\_}/V_{DUT\_}$ = +6.5V/-1.5V, DATA_ = 1		+60		+120	
		$V_{DTV\_}/V_{DUT\_}$ = -1.5V/+6.5V, RCV_ = 1		-120		-60	
		$V_{DTV\_}/V_{DUT\_}$ = +6.5V/-1.5V, RCV_ = 1		+60		+120	
DC Output Resistance		(Note 4)		48	50	52	Ω

Dual Driver/Comparator/Load with Internal DACs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC Output Resistance Variation		DATA_ = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, $I_{DUT\_}$ = 1mA to 40mA		1	2	Ω
		DATA_ = 0, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, $I_{DUT\_}$ = -1mA to -40mA		1	2	
AC CHARACTERISTICS ($R_{DUT\_}$ = 50Ω to ground) (Note 5)						
Dynamic Drive Current		(Note 6)		60		mA
Drive-Mode Overshoot		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 0.1V		30		mV
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 1V (Note 2)		40	75	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 3V (Note 2)		50	175	
		$V_{DLV\_}$ = 0, $V_{DHV\_}$ = 5V (Note 2)		50	275	
Termination-Mode Overshoot		(Note 7)		0		mV
Settling Time (Note 8)		To within 100mV, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0		0.25		ns
		To within 50mV, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0		0.25		
		To within 25mV, $V_{DHV\_}$ = 0.5V, $V_{DLV\_}$ = 0		0.25		
TIMING CHARACTERISTICS (Notes 5, 9)						
Prop Delay (Note 2)		Data to output; $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0		2	3	ns
		Drive to high impedance, high impedance to drive (Note 10); $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = -1V		1.7	4	
		Drive to term		2.7	4	
		Term to drive		1.7	4	
Prop Delay Match (Note 2)		t_{LH} vs. t_{HL}		50	100	ps
		Drivers within package; same edge		40	100	
Prop-Delay Temperature Coefficient		(Note 2)		1	5	ps/°C
Prop Delay Change vs. Pulse Width (Note 2)		$V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0, 2ns to 23ns pulse width		10	100	ps
		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 3ns to 22ns pulse width		10	100	
		$V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0, 4ns to 21ns pulse width		20	100	
Prop Delay Change vs. Common Mode		$V_{DHV\_}$ - $V_{DLV\_}$ = 1V, $V_{DHV\_}$ = 0 to 6V, (using a DC block)		25		ps
Delay Match		Drive to high impedance vs. high impedance to drive; $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = -1V (Note 11)		0.2		ns
		High impedance vs. data (Note 2)		0.4		
		Drive to term vs. term to drive; $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V (Note 12)		1		
		Terminate vs. data		0.7		

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Rise and Fall Time		$0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0, 20% to 80%			0.20		ns
		$1V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0, 10% to 90%		0.35	0.50	0.75	
		$3V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 10% to 90%, trim condition		1.0	1.2	1.5	
		$5V_{P-P}$ programmed $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0, 10% to 90%			2.0		
Rise and Fall Time Matching		$0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0, 20% to 80%			40		ps
		$1V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0, 10% to 90%				150	
		$3V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 10% to 90				200	
		$5V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0, 10% to 90% (Note 2)				250	
Slew Rate		Relative to SC1 = SC0 = 0	SC1 = 0, SC0 = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 20% to 80%		75		%
			SC1 = 1, SC0 = 0, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 20% to 80%		50		
			SC1 = 1, SC0 = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, 20% to 80%		25		
Minimum Pulse Width (Note 13)		Positive or negative	$0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0		0.4		ns
			$1V_{P-P}$ programmed $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0 (Note 2)		0.7	2	
			$3V_{P-P}$ programmed $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0 (Note 2)		1.5	2.5	
			$5V_{P-P}$ programmed $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0 (Note 2)		2.4	3.5	
Data Rate (Note 14)		$0.2V_{P-P}$ programmed, $V_{DHV\_}$ = 0.2V, $V_{DLV\_}$ = 0			2900		Mbps
		$1V_{P-P}$ programmed, $V_{DHV\_}$ = 1V, $V_{DLV\_}$ = 0			1300		
		$3V_{P-P}$ programmed, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0			600		
		$5V_{P-P}$ programmed, $V_{DHV\_}$ = 5V, $V_{DLV\_}$ = 0			400		
Rise and Fall Time, Drive to Term		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, measured 10% to 90% of waveform			1.6		ns
Rise and Fall Time, Term to Drive		$V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, measured 10% to 90% of waveform			0.7		ns

Dual Driver/Comparator/Load with Internal DACs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
COMPARATOR						
DC CHARACTERISTICS						
Input Voltage Range			-1.5		+6.5	V
Differential Input Voltage					±8	V
Minimum Hysteresis		RHYST_ = open		0		mV
Maximum Hysteresis		$R_{RHYST\_}$ = 2.5kΩ		10		mV
Input Offset Voltage		$V_{DUT\_}$ = 1.5V			±50	mV
Input-Voltage Temperature Coefficient		(Notes 2, 15)		±75	±400	µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = -1.5V, +6.5V	50	70		dB
Linearity Error, 0 to 3V		$V_{DUT\_}$ = 0, 1.5V, 3V (Note 16)		±1	±5	mV
Linearity Error, Full Range		$V_{DUT\_}$ = -1.5V, 0, +1.5V, +3V, +6.5V (Note 16)		±1	±10	mV
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = -1.5V and +6.5V	50	75		dB
AC CHARACTERISTICS (Notes 17–20)						
Minimum Pulse Width		(Note 21)		0.85		ns
Prop Delay				1.2	2	ns
Prop-Delay Temperature Coefficient		(Note 2)		2.6	5	ps/°C
Prop Delay Match		High/low vs. low/high; absolute value of delta for each comparator (Note 2)		40	100	ps
Prop Delay Dispersion vs. Common-Mode Input		Common-mode input -1.4V to +6.4V (Note 22)		20		ps
Prop Delay Dispersion vs. Pulse Width (Note 2)		3ns to 22ns pulse width, 500ps t_{RISE}, positive and negative pulses		10	60	ps
		2ns to 23ns pulse width		10	100	
Prop Delay Dispersion vs. Slew Rate		Slew rate = 0.5V/ns to 2V/ns		10		ps
Waveform Tracking (Note 23)		100mV < $V_{C\_V\_}$ < 900mV, driver in term mode, peak-to-peak within this window		40		ps
		50mV < $V_{C\_V\_}$ < 950mV, driver in term mode, peak-to-peak within this window		60		
		100mV < $V_{C\_V\_}$ < 900mV, driver in high impedance, peak-to-peak within this window		100		
LOGIC OUTPUTS (CH_, NCH_, CL_, NCL_)						
Termination Voltage	$V_{T\_}$		0		3.5	V
Output Voltage Compliance		Set by I_{OUT}, R_{TERM}, and $V_{T\_}$	-0.5		$V_{T\_}$	V
Differential Rise Time		20% to 80% (Note 2)		200	400	ps
Differential Fall Time		20% to 80% (Note 2)		200	400	ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Termination Resistor Value		$V_{T\_}$ to CH_, NCH_, CL_, NCL_	48		52	Ω
Output High Voltage		$V_{T\_}$ = 0, 3.5V	$V_{T\_}$ - 0.1	$V_{T\_}$ - 0.02	$V_{T\_}$	V
Output Low Voltage		$V_{T\_}$ = 0, 3.5V	$V_{T\_}$ - 0.55	$V_{T\_}$ - 0.4	$V_{T\_}$ - 0.35	V
Output Voltage Swing		$V_{T\_}$ = 0, 3.5V	350	400	450	mV
DYNAMIC CLAMPS						
Functional Clamp Range		CPHV_; $I_{DUT\_}$ = -1mA, CPHV_ = -0.4V and +6.6V, CPLV_ = -1.5V	-0.3		+6.5	V
		CPLV_; $I_{DUT\_}$ = 1mA, CPLV_ = -1.6V and +5.4V, CPHV_ = +6.5V	-1.5		+5.3	
Maximum Programmable CPHV_		$I_{DUT\_}$ = 0mA (Note 24)	7.2	7.5		V
Minimum Programmable CPLV_		$I_{DUT\_}$ = 0mA (Note 24)		-2.5	-2.2	V
Offset Voltage		$I_{DUT\_}$ = -1mA, CPHV_ = +1.5V, CPLV_ = -1.5V			±50	mV
		$I_{DUT\_}$ = +1mA, CPLV_ = +1.5V, CPHV_ = +6.5V			±50	
Offset-Voltage Temperature Coefficient				0.5		mV/°C
Power-Supply Rejection		$I_{DUT\_}$ = -1mA, CPHV_ = +1.5V, CPLV_ = -1.5V	40			dB
		$I_{DUT\_}$ = +1mA, CPLV_ = +1.5V, CPHV_ = +6.5V	40			
High-Clamp Voltage Gain		CPHV_ = 0, +6.5V, CPLV_ = -1.5V	0.99		1.01	V/V
Low-Clamp Voltage Gain		CPLV_ = -1.5V, +5.3V, CPHV_ = +6.5V	0.99		1.01	V/V
Voltage Gain Matching					1	%
Voltage-Gain Temperature Coefficient				100		ppm/°C
Linearity		$I_{DUT\_}$ = -1mA, CPHV_ = 0, +1.5V, +3.25V, +5V, +6.5V			±30	mV
		$I_{DUT\_}$ = +1mA, CPLV_ = -1.5V, +0.5V, +2.25V, +4V, +5.3V			±30	
Static Output Current		CPHV_ = 0, CPLV_ = -1.5V, $R_{L\_}$ = 0Ω to +6.5V	-120		-60	mA
		CPLV_ = +5V, CPHV_ = +6.5V, $R_{L\_}$ = 0Ω to -1.5V	60		120	
DC Impedance		High clamp, $V_{CPHV\_}$ = 2.5V, $I_{DUT\_}$ = -5mA and -15mA	48		55	Ω
		Low clamp, $V_{CPLV\_}$ = 2.5V, $I_{DUT\_}$ = 5mA and 15mA	48		55	
DC Impedance Variation (Note 25)		High clamp, $I_{DUT\_}$ = -20mA and -30mA, CPHV_ = +2.5V, CPLV_ = -1.5V		±5		Ω
		Low clamp, $I_{DUT\_}$ = 20mA and 30mA, CPLV_ = 2.5V, CPHV_ = 6.5V		±5		

Dual Driver/Comparator/Load with Internal DACs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overshoot and Undershoot		(Note 26)		650		mV
LEVEL-SETTING DACs						
Resolution	N	DHV_, DLV_, DTV_, CHV_, CLV_		16		Bits
		CPLV_, CPHV_		12		
Differential Nonlinearity	DNL				±1	mV
Voltage Settling Time		Full-scale change to ±2.5mV		20		µs
GROUND SENSE (DGS)						
Input Range	V_{GS}	Relative to AGND_, verified by functional test	-250		+250	mV
Gain				1		V/V
Input Resistance			1			MΩ
Reference Input		(Note 27)		2.5		V
1k TRI-STATE LOAD (PULLUP/PULLDOWN)						
Source Impedance When Enabled		Tested at -5mA, 0, +5mA using a 0.5mA step	950		1050	Ω
Maximum Source Current		$V_{DUT\_}$ = +6.1V, $V_{DTV\_}$ = -1.1V	6.9	7.2		mA
Maximum Sink Current		$V_{DUT\_}$ = -1.1V, $V_{DTV\_}$ = +6.1V	6.9	7.2		mA
Turn-On Time				60		ns
Turn-Off Time				60		ns
Offset Voltage		Output with no load, $V_{DTV\_}$ = 0 and 3V			±50	mV
Linearity Error		No load, $V_{DTV\_}$ = -1.5V to +6.5V			±25	mV
TEMPERATURE MONITOR						
Nominal Voltage		T_J = +70°C, R_L ≥ 10MΩ		3.43		V
Temperature Coefficient				10		mV/°C
Output Resistance				15		kΩ
DIFFERENTIAL CONTROL INPUTS (DATA_, NDATA_, RCV_, NRCV_)						
Input High Voltage			-1.6		+3.5	V
Input Low Voltage			-2.0		+3.1	V
Differential Input Voltage			±0.15		±1.00	V
Termination Resistor		50Ω to VTERM_	48		52	Ω
VTERM_ Voltage Range		Verified by functional test	-2.0		+3.5	V
SERIAL PORT INPUTS ($\overline{CS}$, SCLK, DIN, $\overline{RST}$, $\overline{LOAD}$, V_{DD} = 3.3V)						
Input High			2/3 (V_{DD})		V_{DD}	V
Input Low			-0.1		1/3 (V_{DD})	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL PORT TIMING (Note 28)						
SCLK Frequency					50	MHz
SCLK Pulse-Width High	t_1		8			ns
SCLK Pulse-Width Low	t_2		8			ns
$\overline{CS}$ Low to SCLK High Setup	t_3		3.5			ns
SCLK High to $\overline{CS}$ Low Hold	t_4		3.5			ns
$\overline{CS}$ High to SCLK High Setup	t_5		3.5			ns
SCLK High to $\overline{CS}$ High Hold	t_6		3.5			ns
DIN to SCLK High Setup	t_7		3.5			ns
DIN to SCLK High Hold	t_8		3.5			ns
$\overline{CS}$ High Pulse Width	t_9		20			ns
$\overline{LOAD}$ Low Pulse Width	t_{10}		20			ns
$\overline{RST}$ Low Pulse Width	t_{11}		20			ns
$\overline{CS}$ High to $\overline{LOAD}$ Low Hold Time	t_{12}		20			ns
COMMON FUNCTIONS						
Operating Voltage Range		(Note 29)	-1.5		+6.5	V
DUT_ High-Impedance Leakage		0 < $V_{DUT\_}$ < 3V			±2	µA
		$V_{CLV\_}$ = $V_{CHV\_}$ = +6.5V, $V_{DUT\_}$ = -1.5V			±5	
		$V_{CLV\_}$ = $V_{CHV\_}$ = -1.5V, $V_{DUT\_}$ = +6.5V			±5	
DUT_ Low-Leakage Mode Leakage		LEAK = 1, 0 < $V_{DUT\_}$ < 3V, T_J < +90°C	-10		+10	nA
		LEAK = 1, $V_{CLV\_}$ = $V_{CHV\_}$ = +6.5V, $V_{DUT\_}$ = -1.5V, T_J < +90°C	-10		+10	
		LEAK = 1, $V_{CLV\_}$ = $V_{CHV\_}$ = -1.5V, $V_{DUT\_}$ = +6.5V, T_J < +90°C	-10		+10	
DUT_ Combined Capacitance		Driver in terminate mode		2		pF
		Driver in high impedance		4		
POWER SUPPLY						
Positive Supply Voltage	V_{CC}		9.5	9.75	10.5	V
Negative Supply Voltage	V_{EE}		-5.2	-4.75	-4.5	V
Logic Supply Voltage	V_{DD}		2.7	3.3	5.0	V
Positive Supply Current	I_{CC}	(Note 30)		70	85	mA
Negative Supply Current	I_{EE}	(Note 30)		150	180	mA
Logic Supply Current	I_{DD}	(Note 30)		1.2	2	mA
Power Dissipation		(Notes 30, 31)		1.4	1.7	W
Power Dissipation per Channel		(Notes 30, 31)		700		mW

Note 1: All minimum and maximum specifications are 100% production tested, unless otherwise noted. All other test limits are guaranteed by design. Tests are performed at nominal supply voltages, unless otherwise noted. Tested with T_J = +70°C with accuracy of ±15°C.

Note 2: Guaranteed by design and characterization.

Dual Driver/Comparator/Load with Internal DACs

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +9.75V, V_{EE} = -4.75V, V_{DD} = 3.3V, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = +1.5V, SC1 = SC0 = 0, $V_{CHV\_}$ = +2.0V, $V_{CLV\_}$ = +1.0V, $V_{CPHV\_}$ = +7.2V, $V_{CPLV\_}$ = -2.2V, V_{VTERM} = $V_{T\_}$ = +1.8V, R_T = 50Ω ll 1pF, T_J = +70°C, unless otherwise noted. All temperature coefficients are measured at T_J = +40°C to +100°C, unless otherwise noted.) (Note 1)

Note 3: Change in any voltage over operating range. Includes both gain and offset temperature effects. Simulated over entire operating range. Verified at worst-case points, which are the endpoints. $V_{DHV\_}$ - $V_{DLV\_}$ > 250mV.

Note 4: DATA_ = 1, $V_{DHV\_}$ = 3V, $V_{DLV\_}$ = 0, $V_{DTV\_}$ = 1.5V, I_{OUT} = ±30mA. Different values within the range of 48Ω to 52Ω are available by custom trimming (contact factory).

Note 5: Rise time of the differential inputs DATA_ and RCV_ is 250ps (10% to 90%). SC1 = SC0 = 0, 40MHz, unless otherwise specified.

Note 6: 0 to 6V step, current supplied for a minimum of 10ns.

Note 7: $V_{DTV\_}$ = 1.5V, R_S = 50Ω external signal driven into a transmission line to produce a 0/3V edge at the comparator input with ≤ 1.0ns rise time (10% to 90%). Measurement point is at comparator input.

Note 8: Measured from the 90% point of the driver output (relative to its final value) to the waveform settling to within the specified limit.

Note 9: Propagation delays are measured from the crossing point of the differential input signals to the 50% point of expected output swing.

Note 10: Measured from crossing point of RCV_/NRCV_ to 50% point of the output waveform.

Note 11: Four measurements are made: DHV_ to high impedance, DLV_ to high impedance, high impedance to DHV_, high impedance to DLV_. The worst difference is specified.

Note 12: Four measurements are made: DHV_ to DTV_, DLV_ to DTV_, DTV_ to DHV_, DTV_ to DLV_. The worst difference is specified.

Note 13: At this pulse width, the output reaches at least 95% of its nominal (DC) amplitude. The pulse width is measured at DATA_ and NDATA_.

Note 14: Maximum data rate in transitions/second. A waveform that reaches at least 95% of its programmed amplitude may be generated at one-half of this frequency.

Note 15: Change in offset at any voltage over operating range. Includes both gain (CMRR) and offset temperature effects.

Note 16: Relative to straight line between 0 and 3V.

Note 17: All propagation delays measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to crossing point of differential outputs.

Note 18: Load is a 500ps transmission line terminated with 1pF and 50Ω.

Note 19: All AC specifications are measured with DUT_ (comparator input) as the reference.

Note 20: 40MHz, 0 to 2V input to comparator, reference = 1V, 50% duty cycle, 1ns rise/fall time, Z_S = 50Ω, driver in term mode with $V_{DTV\_}$ = 0, unless otherwise noted.

Note 21: At this pulse width, the output reaches at least 90% of its nominal peak-to-peak swing. The pulse width is measured at the crossing points of the differential outputs. 500ps rise and fall time. Timing specs are not guaranteed.

Note 22: $V_{DUT\_}$ = 200mV_{P-P}, rise/fall time = 150ps, overdrive = 100mV, $V_{DTV\_}$ = V_{CM}. Valid for common-mode ranges where the signal does not exceed the operating range. Specification is worst case (slowest to fastest) over the specified range.

Note 23: Input to comparator is 40MHz at 0 to 1V, 50% duty cycle, 1ns rise time.

Note 24: This specification is implicitly tested, by meeting the high-impedance leakage specification.

Note 25: Resistance measurements are made using small-signal voltage changes in the loading instrument. Absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity.

Note 26: Ripple in the DUT_ signal after one round-trip delay. Stimulus is 0 to 3V, 2.5V/ns square wave from far end of 3ns transmission line with R_S = 25Ω, clamps set to 0 and 3V.

Note 27: Any deviation from 2.5V affects offset and gain of all levels.

Note 28: Serial port timing specifications are measured at a logic supply voltage (V_{DD}) of +3.3V, ensuring operation of the serial port at rated speed for V_{DD} from +3.3V to +5.5V.

Note 29: The maximum usable output operating voltage is limited to -1.5V to +6.5V. Externally forced voltages may exceed this range without damage to the device, provided that they are limited per the *Absolute Maximum Ratings*. External clamps must be provided to limit voltages in this range, or damage to the device is likely.

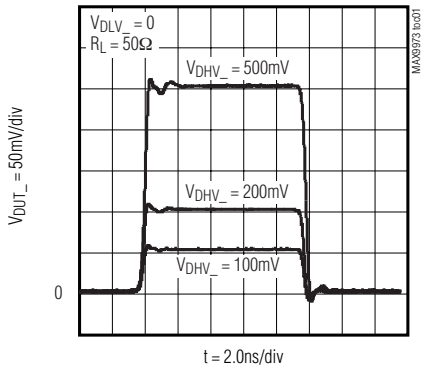
Note 30: Total for dual device. R_L ≥ 10MΩ. Worst case of the following conditions: driver enabled, LLEAK = 0; driver disabled, LLEAK = 0; driver enabled, RCV_ = 1; driver disabled, LLEAK = 1.

Note 31: Excludes dissipation of comparator output supply. A typical output configuration and V+ = 1.8V adds 30mW (typ) per channel to device power.

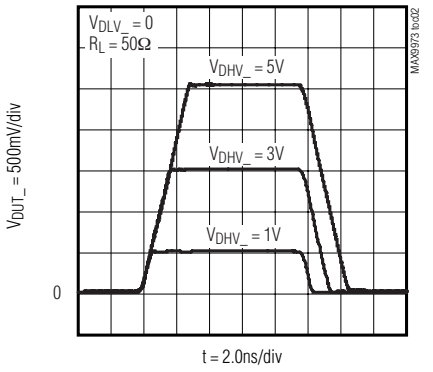
Typical Operating Characteristics

(T_J = +70°C, unless otherwise noted.)

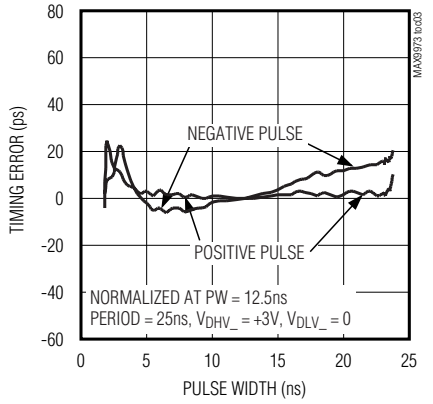
DRIVER SMALL-SIGNAL RESPONSE



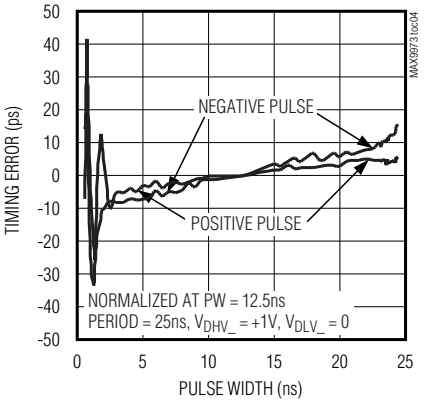
DRIVER LARGE-SIGNAL RESPONSE



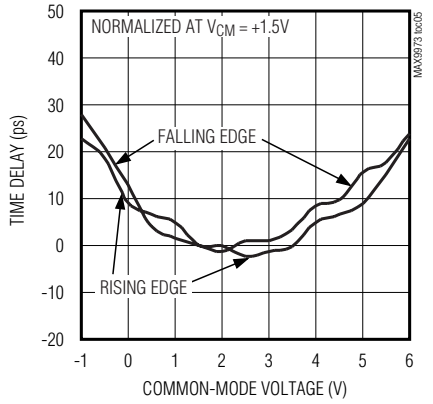
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



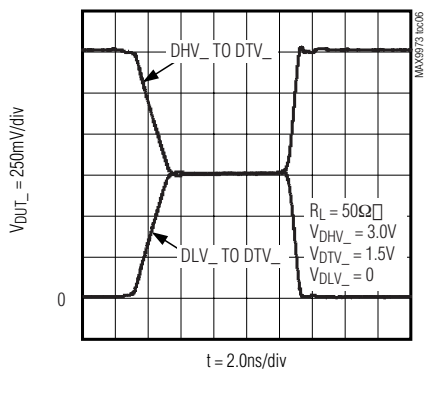
DRIVER 1V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



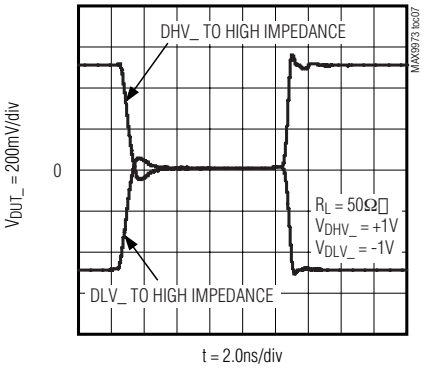
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



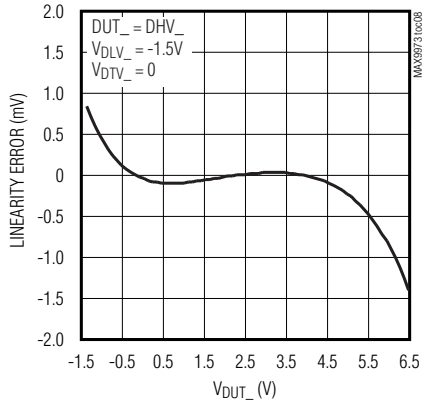
DRIVE TO TERM TRANSITION



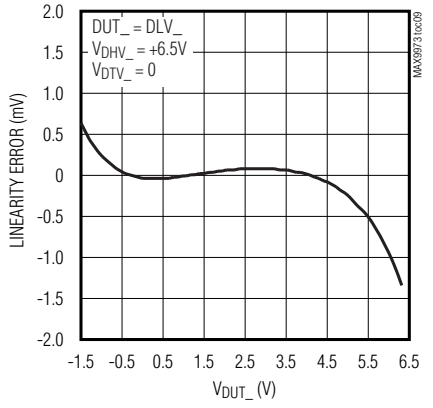
DRIVE TO HIGH IMPEDANCE TRANSITION



DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE

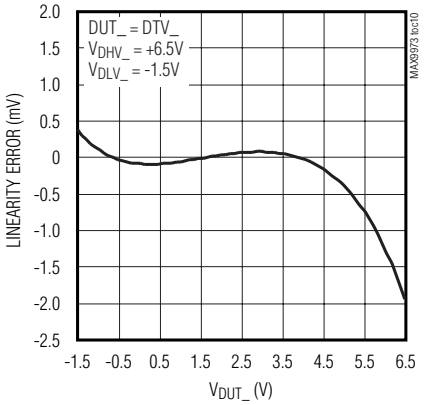


Dual Driver/Comparator/Load with Internal DACs

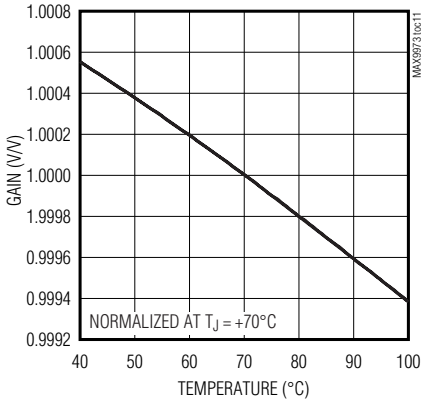
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

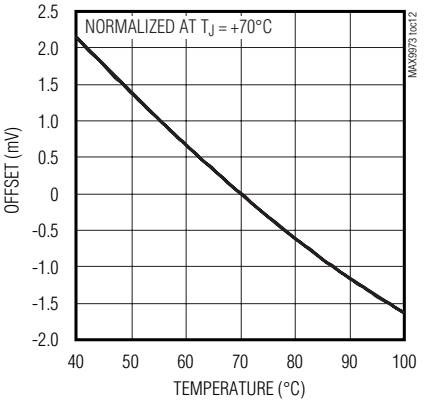
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



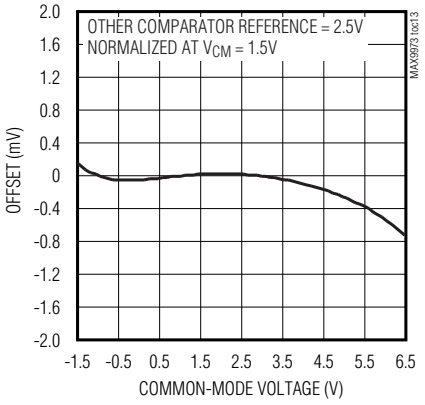
DRIVER GAIN vs. TEMPERATURE



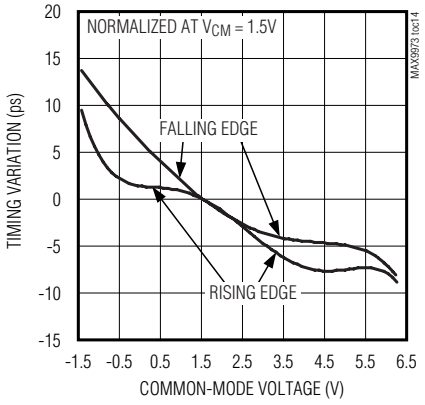
DRIVER OFFSET vs. TEMPERATURE



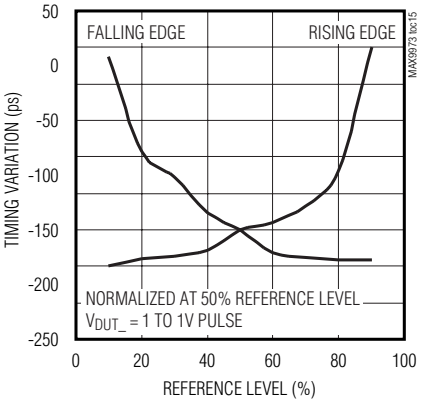
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



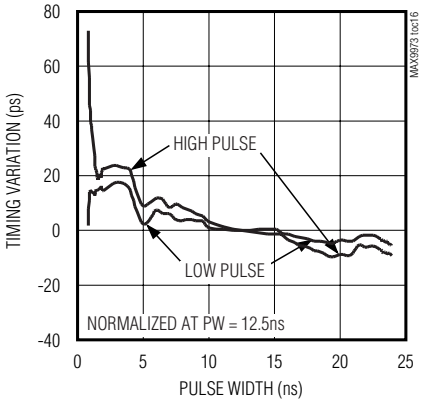
COMPARATOR TIMING VARIATION vs. COMMON-MODE VOLTAGE



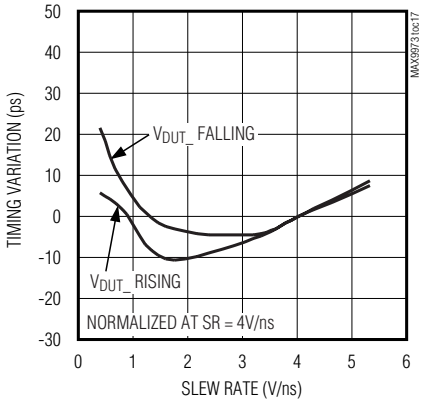
COMPARATOR WAVEFORM TRACKING



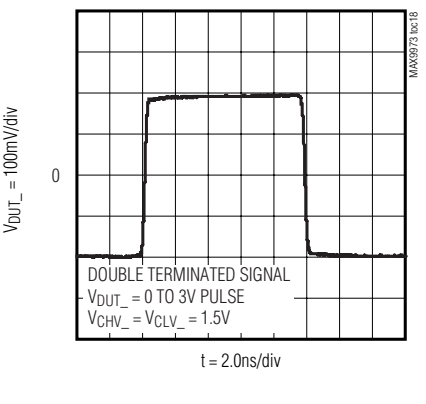
COMPARATOR TRAILING-EDGE TIMING VARIATION vs. PULSE WIDTH



COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



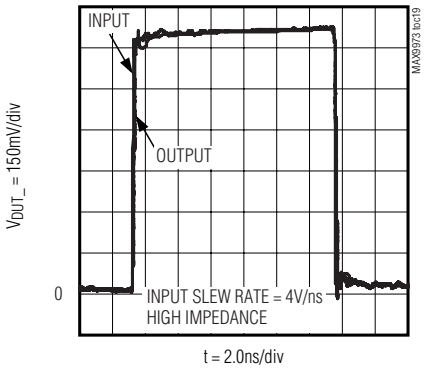
COMPARATOR DIFFERENTIAL OUTPUT RESPONSE



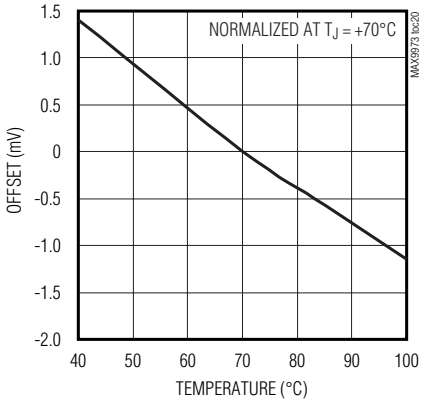
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

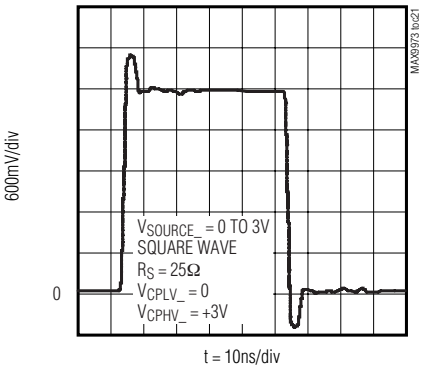
COMPARATOR RESPONSE TO HIGH SLEW-RATE OVERDRIVE



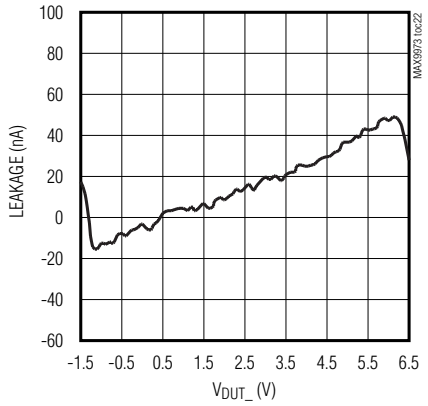
COMPARATOR OFFSET vs. TEMPERATURE



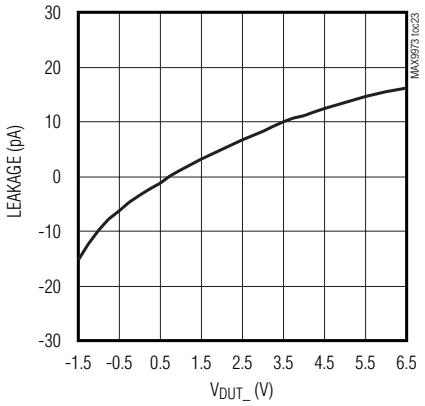
CLAMP RESPONSE AT SOURCE



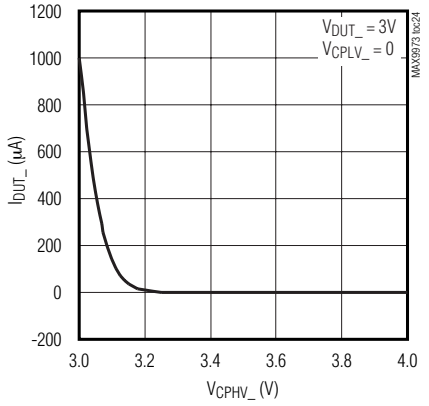
HIGH-IMPEDANCE LEAKAGE CURRENT vs. DUT_ VOLTAGE



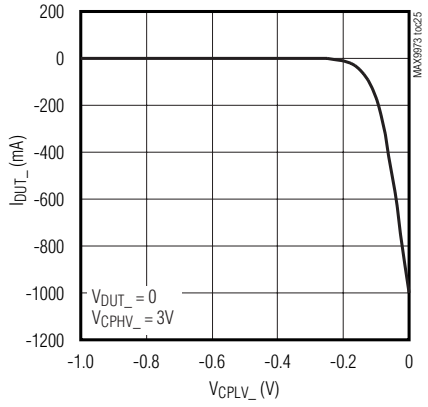
LOW LEAKAGE CURRENT vs. DUT_ VOLTAGE



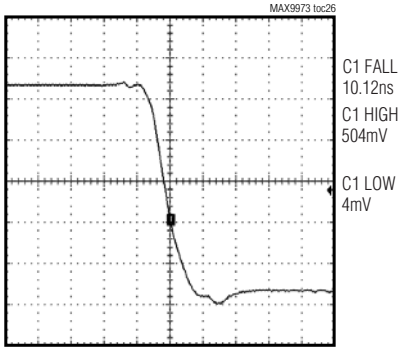
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



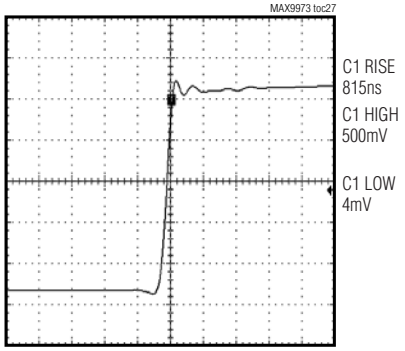
CLAMP CURRENT vs. DIFFERENCE VOLTAGE



DRIVE 1V TO LOW LEAKAGE TRANSITION



LOW LEAKAGE TO DRIVE 1V TRANSITION

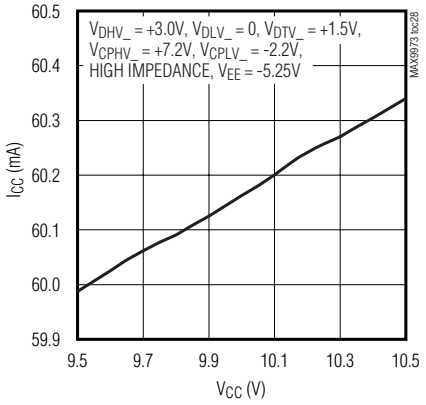


Dual Driver/Comparator/Load with Internal DACs

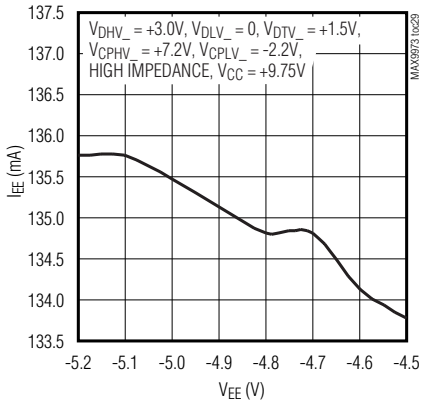
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

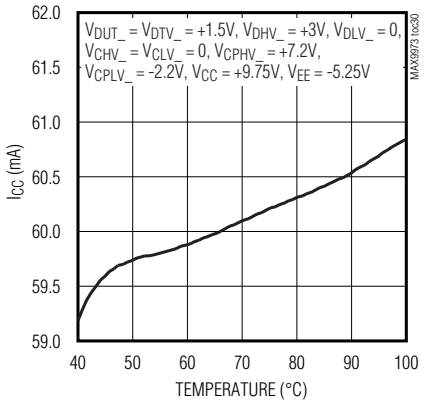
POSITIVE SUPPLY CURRENT vs. POSITIVE SUPPLY VOLTAGE



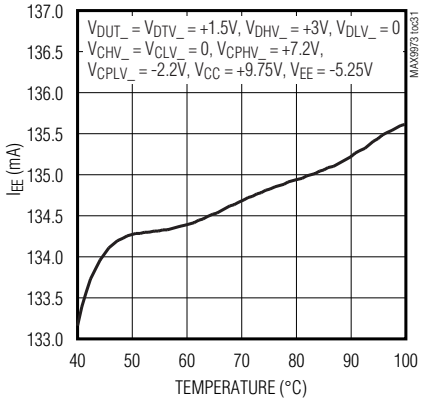
NEGATIVE SUPPLY CURRENT vs. NEGATIVE SUPPLY VOLTAGE



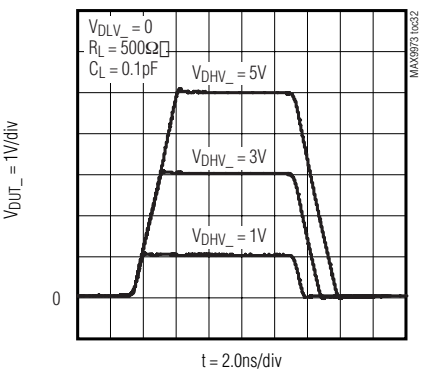
POSITIVE SUPPLY CURRENT vs. TEMPERATURE



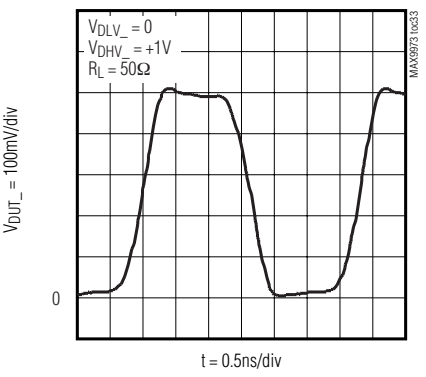
NEGATIVE SUPPLY CURRENT vs. TEMPERATURE



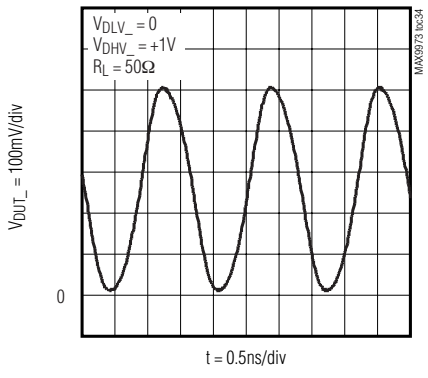
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



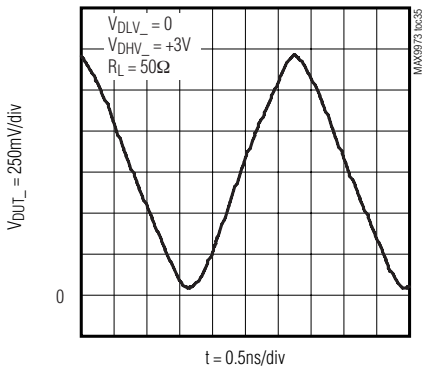
DRIVER 1V 600Mbps SIGNAL RESPONSE



DRIVER 1V 1200Mbps SIGNAL RESPONSE



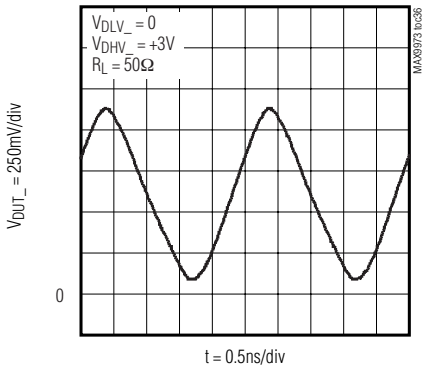
DRIVER 3V 600Mbps SIGNAL RESPONSE



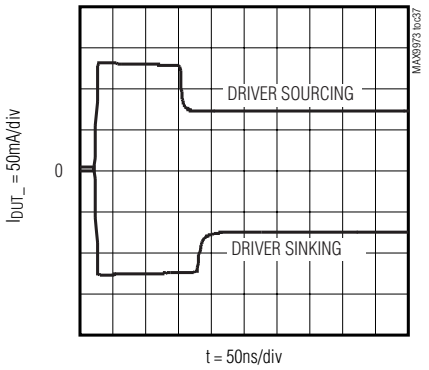
Typical Operating Characteristics (continued)

(T_J = +70°C, unless otherwise noted.)

DRIVER 3V 800Mbps SIGNAL RESPONSE



DRIVER DYNAMIC CURRENT-LIMIT RESPONSE



Pin Description

PIN (MAX9973)	NAME	FUNCTION	
1, 16, 18, 33, 36, 39, 42, 45, 48, 63	V_{EE}	Negative Power-Supply Input	
2, 15, 24, 35, 37, 44, 46, 57	V_{CC}	Positive Power-Supply Input	
3, 14	AGND	Analog Ground Connection	
4	REF	DAC Reference Input. Set to 2.5V with respect to DGS.	
5	DGS	DUT Ground Sense. DGS is the ground reference for the DACs. Connect DGS to ground of the device-under-test.	
6	TEMP	Temperature Monitor Output	
7, 17, 32, 40, 41, 49, 64	GND	Ground	
8	$\overline{CS}$	Chip-Select Input. Serial port activation input.	
9	SCLK	Serial-Clock Input. Clock for serial port.	
10	DIN	Data Input. Serial port data input.	
11	V_{DD}	Digital Interface Power-Supply Input	
12	$\overline{LOAD}$	Load Input. Latches serial register data into DACs.	
13	$\overline{RST}$	Reset Input. Asynchronous reset input for the serial register.	
19	NDATA1	Channel 1 Multiplexer Control Input N	Differential controls DATA1 and NDATA1 select driver 1's input from DHV1 or DLV1. Drive DATA1 above NDATA1 to select DHV1. Drive NDATA1 above DATA1 to select DLV1.
20	DATA1	Channel 1 Multiplexer Control Input	
21	VTERM1	Channel 1 RCV/NRCV and DATA/NDATA Termination Voltage Input. Termination voltage input for the RCV1, NRCV1, DATA1, and NDATA1 differential inputs.	

Dual Driver/Comparator/Load with Internal DACs

Pin Description (continued)

PIN (MAX9973)	NAME	FUNCTION	
22	NRCV1	Channel 1 Multiplexer Control Input N	Differential controls RCV1 and NRCV1 place channel 1 in receive mode. Drive RCV1 above NRCV1 to place channel 1 into receive mode. Drive NRCV1 above RCV1 to place channel 1 into drive mode.
23	RCV1	Channel 1 Multiplexer Control Input	
25, 34, 47, 56	N.C.	No Connection. Make no connection.	
26	NCL1	Channel 1 Low Comparator Output N	Differential outputs of channel 1 low comparator.
27	CL1	Channel 1 Low Comparator Output	
28	V_{T1}	Comparator Termination Voltage Input. Termination voltage for the comparator output pullup resistors for channel 1.	
29	NCH1	Channel 1 High Comparator Output N	Differential outputs of channel 1 high comparator.
30	CH1	Channel 1 High Comparator Output	
31	RHYST1	Comparator Hysteresis Programming Input for Channel 1	
38	DUT1	Channel 1 Device-Under-Test Input/Output. Combined I/O for driver, comparator, clamp, and load.	
43	DUT0	Channel 0 Device-Under-Test Input/Output. Combined I/O for driver, comparator, clamp, and load.	
50	RHYST0	Comparator Hysteresis Programming Input for Channel 0	
51	CH0	Channel 0 High Comparator Output	Differential outputs of channel 0 high comparator.
52	NCH0	Channel 0 High Comparator Output N	
53	V_{T0}	Comparator Termination Voltage Input. Termination voltage for the comparator output pullup resistors for channel 0.	
54	CL0	Channel 0 Low Comparator Output	Differential outputs of channel 0 low comparator.
55	NCL0	Channel 0 Low Comparator Output N	
58	RCV0	Channel 0 Multiplexer Control Input	Differential controls RCV0 and NRCV0 place channel 0 in receive mode. Drive RCV0 above NRCV0 to place channel 0 into receive mode. Drive NRCV0 above RCV0 to place channel 0 into drive mode.
59	NRCV0	Channel 0 Multiplexer Control Input N	
60	VTERM0	Channel 0 RCV/NRCV and DATA/NDATA Termination Voltage Input. Termination voltage input for the RCV0, NRCV0, DATA0, and NDATA0 differential inputs.	
61	DATA0	Channel 0 Multiplexer Control Input	Differential controls DATA0 and NDATA0 select driver 0's input from DHV0 or DLV0. Drive DATA0 above NDATA0 to select DHV0. Drive NDATA0 above DATA0 to select DLV0.
62	NDATA0	Channel 0 Multiplexer Control Input N	
—	EP	Exposed Heat Removal Paddle. The paddle is electrically isolated from the die. Make no electrical connection to EP.	

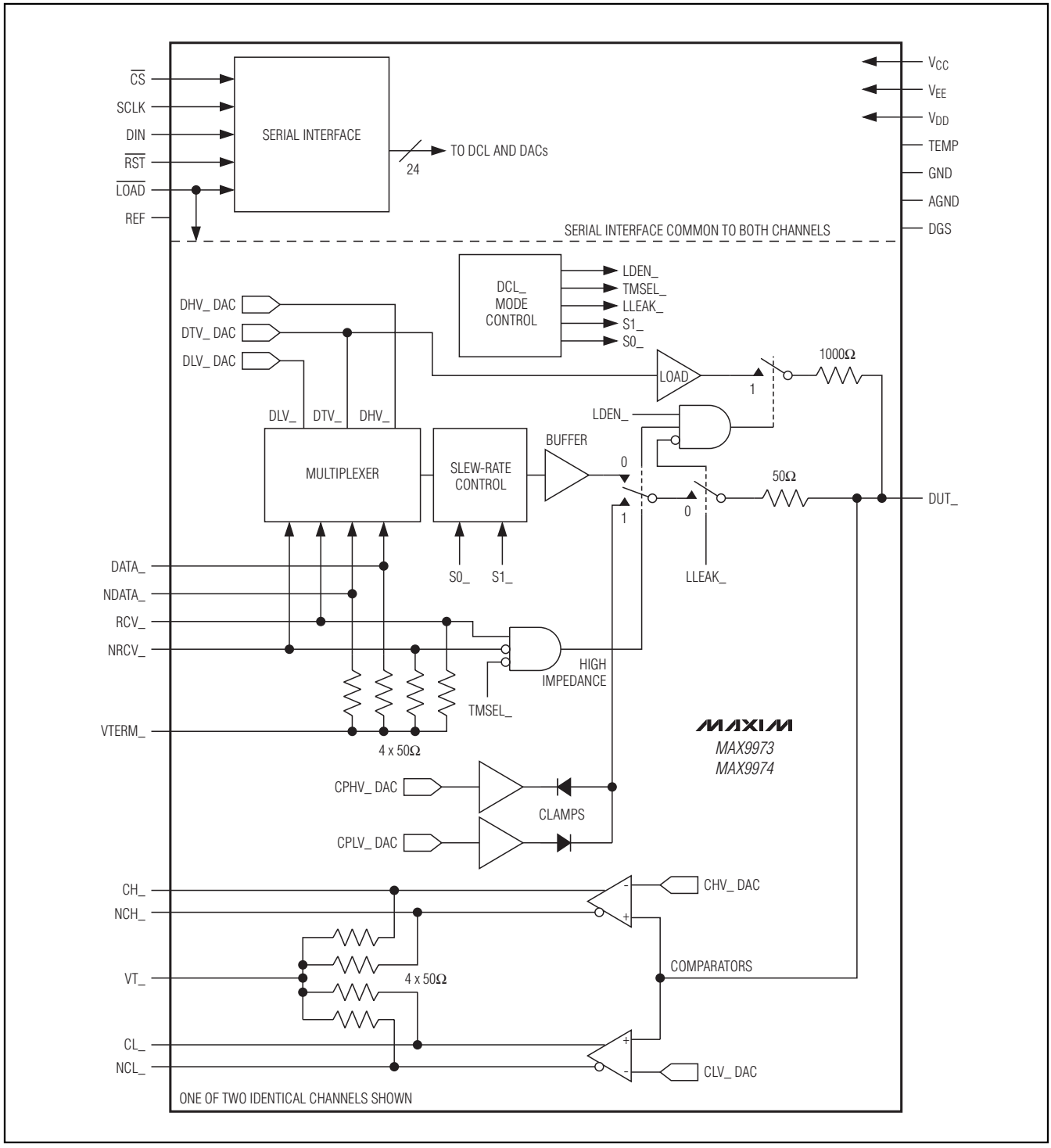


Figure 1. Functional Diagram

Dual Driver/Comparator/Load with Internal DACs

Detailed Description

The MAX9973/MAX9974 are fully integrated, high-performance, dual-channel pin electronics driver/comparator/load (DCL) with built-in level-setting DACs. Each channel includes a three-level pin driver with three level-setting DACs, a window comparator with two level-setting DACs, two dynamic clamps with two level-setting DACs, and a 1kΩ load driven by the driver's DTV_ DAC. Figure 1 shows a functional diagram of the MAX9973/MAX9974.

The three-level pin driver features a wide -1.5V to +6.5V voltage range and includes high-impedance and active-termination (3rd-level drive) modes. High-speed differential multiplexer control inputs DATA and RCV with internal termination resistors switch the driver between the three input levels. Figure 2 shows a block diagram of the simplified driver channel.

The window comparators provide extremely low timing variation. The MAX9973G/MAX9974G comparator open-collector outputs sink 8mA (typ), while the MAX9973H/MAX9974H comparator outputs sink 16mA (typ). Figure 3 shows the comparator function.

The dynamic clamps provide damping of high-speed DUT waveforms when high-impedance receive mode is selected.

The loads facilitate fast contact testing when used in conjunction with the comparators. Loads also function as pullups for a device-under-test that has open-drain/collector outputs.

A serial interface configures the device and its functions. The MAX9973/MAX9974 are available in a 64-pin (10mm x 10mm x 1.00mm) TQFP-EP package with an exposed paddle on top (MAX9973) or bottom (MAX9974) for heat removal. Power dissipation is only 700mW per channel. The full operating voltage range is -1.5V to +6.5V. Operation is specified with an internal die temperature of +40°C to +100°C. The devices feature a temperature monitor output.

Output Driver

The driver input is a high-speed multiplexer that selects one of three DAC voltages: DHV_, DLV_, or DTV_. The high-speed differential inputs DATA_/NDATA_ and RCV_/NRVC_, and mode-control bit TMSEL_ control the

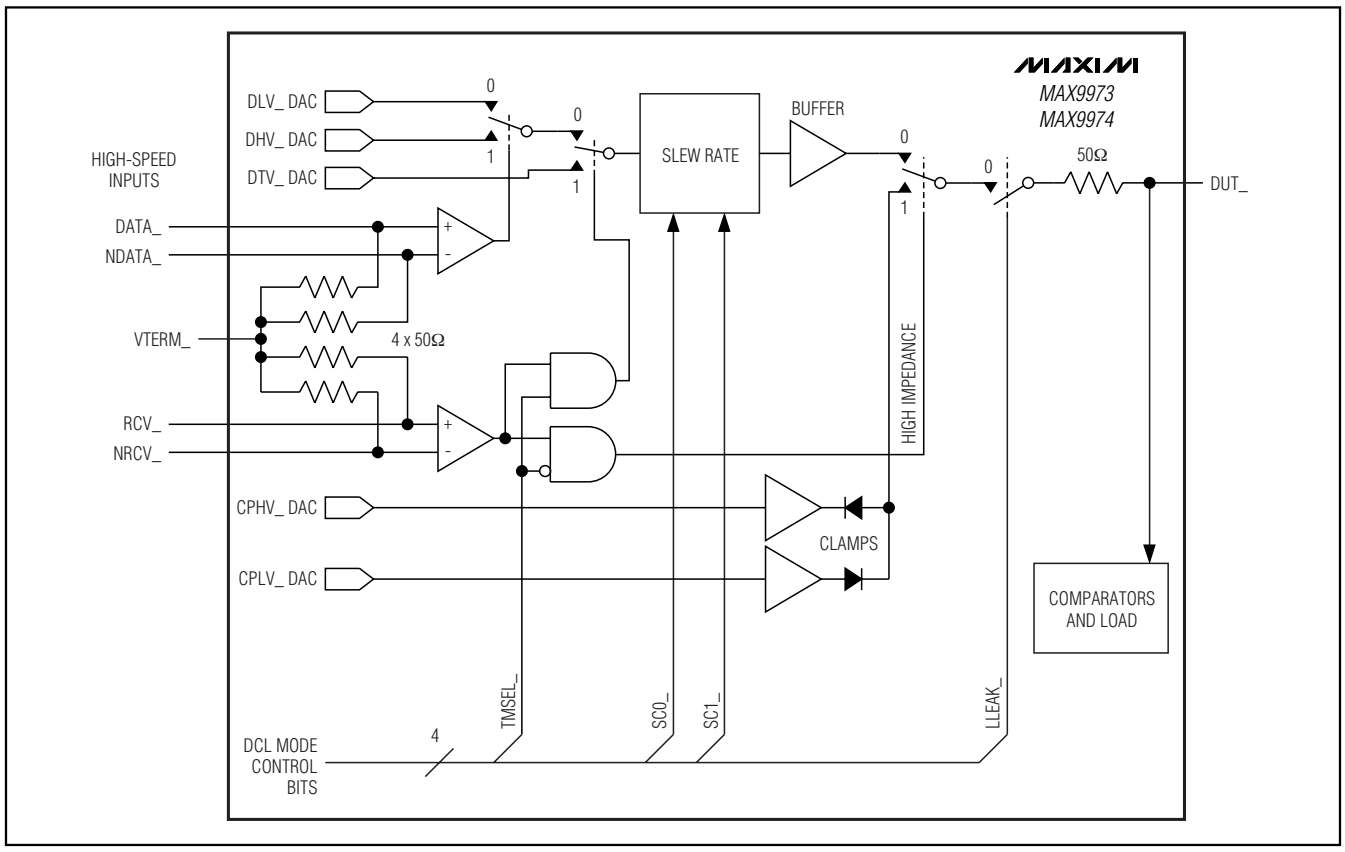


Figure 2. Simplified Driver Channel

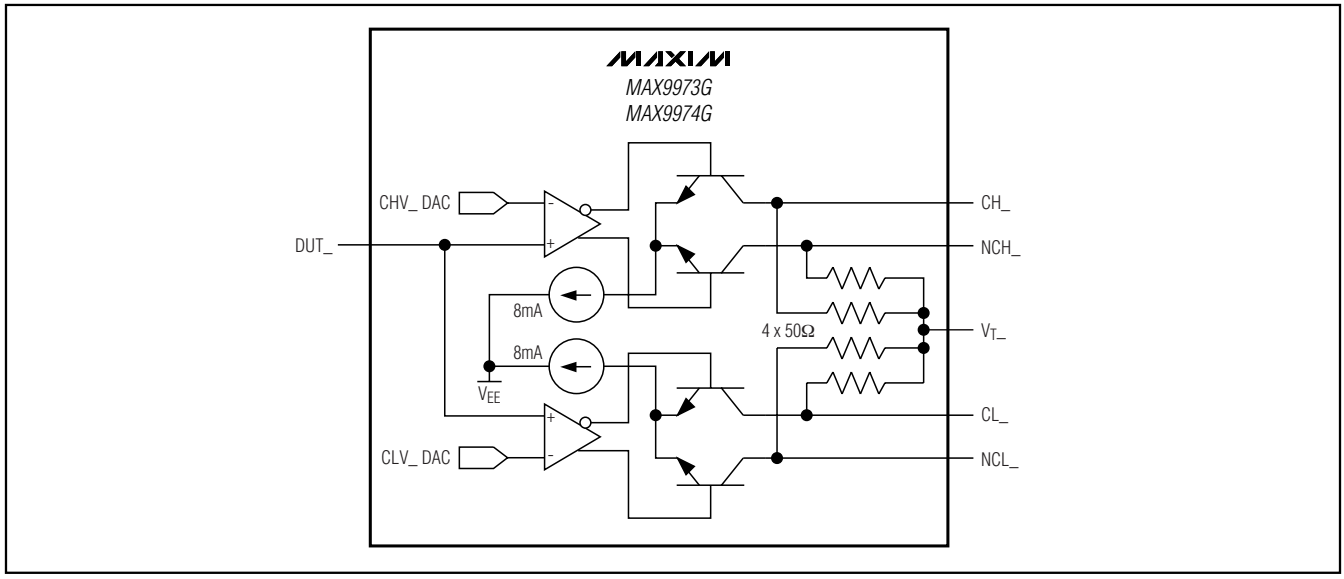


Figure 3. Comparator Functional Diagram

Table 1. Driver Channel Logic

HIGH-SPEED INPUTS		MODE CONTROL BITS		DUT_
DATA_/NDATA_	RCV_/NRCV_	TMSEL_ (D3)	LLEAK_ (D2)	
DATA_ > NDATA_	RCV_ < NRCV_	X	0	DHV_
DATA_ < NDATA_	RCV_ < NRCV_	X	0	DLV_
X	RCV_ > NRCV_	1	0	DTV_
X	RCV_ > NRCV_	0	0	High impedance (clamps engaged)
X	X	X	1	Low leakage

X = Don't care.

Table 2. Driver Slew-Rate Logic

MODE CONTROL BITS		DRIVER SLEW RATE (%)
S1_ (D1)	S0_ (D0)	
0	0	100 (fastest)
0	1	75
1	0	50
1	1	25 (slowest)

Table 3. Comparator Logic

COMPARATOR INPUTS		COMPARATOR OUTPUTS			
DUT_ > CHV_	DUT_ > CLV_	HIGH COMPARATOR		LOW COMPARATOR	
		CH_	NCH_	CL_	NCL_
0	0	0	1	0	1
0	1	0	1	1	0
1	0	1	0	0	1
1	1	1	0	1	0

switching between the DAC voltages (Table 1). A slew-rate circuit controls the slew rate of the buffer input with one of four possible slew rates selectable (Table 2). The 100% slew rate is a function of the inherent speed of the multiplexer (see the Driver Large-Signal Response graph in the *Typical Operating Characteristics*). DUT_ can be toggled at high speed between driver and high-impedance modes, or can be placed into low-leakage mode

Dual Driver/Comparator/Load with Internal DACs

using mode control bit LLEAK_ (Figure 2, Table 1). In high-impedance mode, the bias current at DUT_ is less than 5µA over the -1.5V to +6.5V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than ±10nA, and signal tracking slows. See the *Low-Leakage Mode* section for more details.

The nominal driver output resistance is 50Ω. Contact the factory for different resistance values within the 48Ω to 52Ω range.

Clamps

The voltage clamps (high and low) limit the voltage at DUT_ and suppress reflections when the channel is configured as a high-impedance receiver. The clamps behave as diodes with series 50Ω resistors connected to the outputs of high-current buffers. Internal circuitry compensates for the diode drop at 1mA clamp current. Set the clamp voltages using DACs CPHV_ and CPLV_. The clamps are enabled only when the driver is in high-impedance mode (Figure 2). For transient suppression, set the clamp voltages to approximately the minimum and maximum expected DUT_ voltage range. The optimal clamp voltages are application-specific and must be empirically determined. If clamping is not desired, set the clamp voltages at least 0.7V outside the expected DUT_ voltage range; overvoltage protection remains active without loading DUT_.

Comparators

The MAX9973/MAX9974 provide two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either DAC CHV_ or DAC CLV_ (see Figures 1 and 3). Comparator outputs are a logical result of the input conditions, as indicated in Table 3. The comparator differential outputs are open-collector to ease interfacing with a wide variety of logic families. The MAX9973G/MAX9974G switch an 8mA current sink between the two outputs, while the

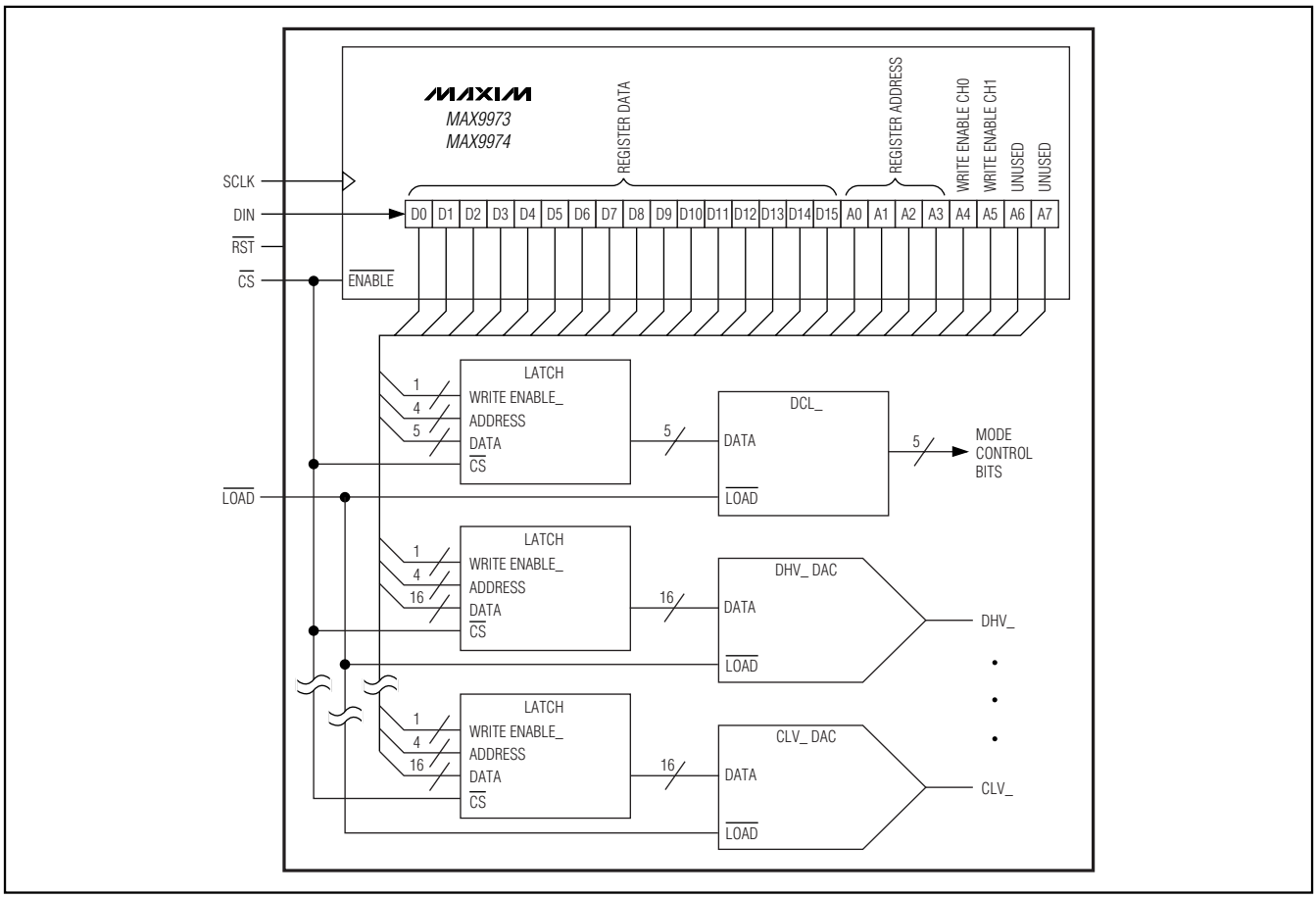


Figure 4. Serial Interface Block Diagram

Table 4. Load Logic

HIGH-SPEED INPUT	MODE CONTROL BITS			LOAD
RCV_/NRCV_	LLEAK_ (D2)	TMSEL_ (D3)	LDEN_ (D4)	
RCV_ < NRCV_	0	X	X	Off
X	0	X	0	Off
RCV_ > NRCV_	0	0	1	On
RCV_ > NRCV_	0	1	1	Off
X	1	X	X	Off

X = Don't care.

Table 5. Serial Interface Data Bit Definitions

DIN BIT	BIT FUNCTION
A7	Not used
A6	Not used
A5	Write enable channel 1
A4	Write enable channel 0
A3	Register address (Table 6)
A2	
A1	
A0	
D15–D0	Register data

MAX9973H/MAX9974H switch 16mA. The 50Ω output termination resistors connect to voltage input $V_{T\_}$. Each output provides a nominal 400mV$_{P-P}$ swing and 50Ω source termination.

1kΩ Load

The 1kΩ load is a resistor connected to DUT_ from the output of an internal buffer. The buffer's input is DAC DTV_ (Figure 1). The buffer sinks and sources at least 6.9mA. A switch separates the resistor from the buffer. Operate the switch with serial control bits LDEN_, LLEAK_, and TMSEL_, and through high-speed differential input RCV_/NRCV_. Table 4 shows the truth table for the load-switch operation.

DUT Ground-Sense Input

The DUT ground-sense input (DGS) senses the ground potential of the device-under-test and allows the output and DAC levels of the MAX9973/MAX9974 to be set relative to that ground potential. Connect DGS to the ground of the device-under-test.

Table 6. Register Addresses

REGISTER ADDRESS BITS				REGISTER FUNCTION
A3	A2	A1	A0	
0	0	0	0	DCL mode
0	0	0	1	DHV_ level
0	0	1	0	DLV_ level
0	0	1	1	DTV_ level
0	1	0	0	CHV_ level
0	1	0	1	CLV_ level
0	1	1	0	CPHV_ level
0	1	1	1	CPLV_ level
1	X	X	X	Not used

Table 7. DCL Mode Control Bits

BIT	NAME	FUNCTION	POWER-UP STATE
D4	LDEN	Load enable	0
D3	TMSEL	Terminate select	0
D2	LLEAK	Low-leakage enable	1
D1	S1	Slew-rate control (Table 2)	0
D0	S0		0

Low-Leakage Mode

Asserting LLEAK_ through the serial interface or with the digital input $\overline{RST}$ places the MAX9973/MAX9974 in a very low-leakage state (see the *Electrical Characteristics* table). With LLEAK_ asserted, the comparators, driver, clamps, and active load are disabled. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK_ is programmed independently for each channel, while $\overline{RST}$ acts on both channels simultaneously.

Serial Interface and Device Control

A CMOS-compatible serial interface controls the MAX9973/MAX9974 modes (Figure 4, Table 5). Control data flow into a 24-bit shift register and is latched when $\overline{CS}$ is taken high, as shown in Figure 5. The first eight bits, A7–A0, determine which of the two channels is being commanded, and which DAC or DCL the following 16 bits program. The 16 bits, D15–D0, set the DAC voltage or control the setup of the MAX9973/MAX9974 through the mode control bits, as shown in Tables 5, 6, 7, and Figure 6.

Dual Driver/Comparator/Load with Internal DACs

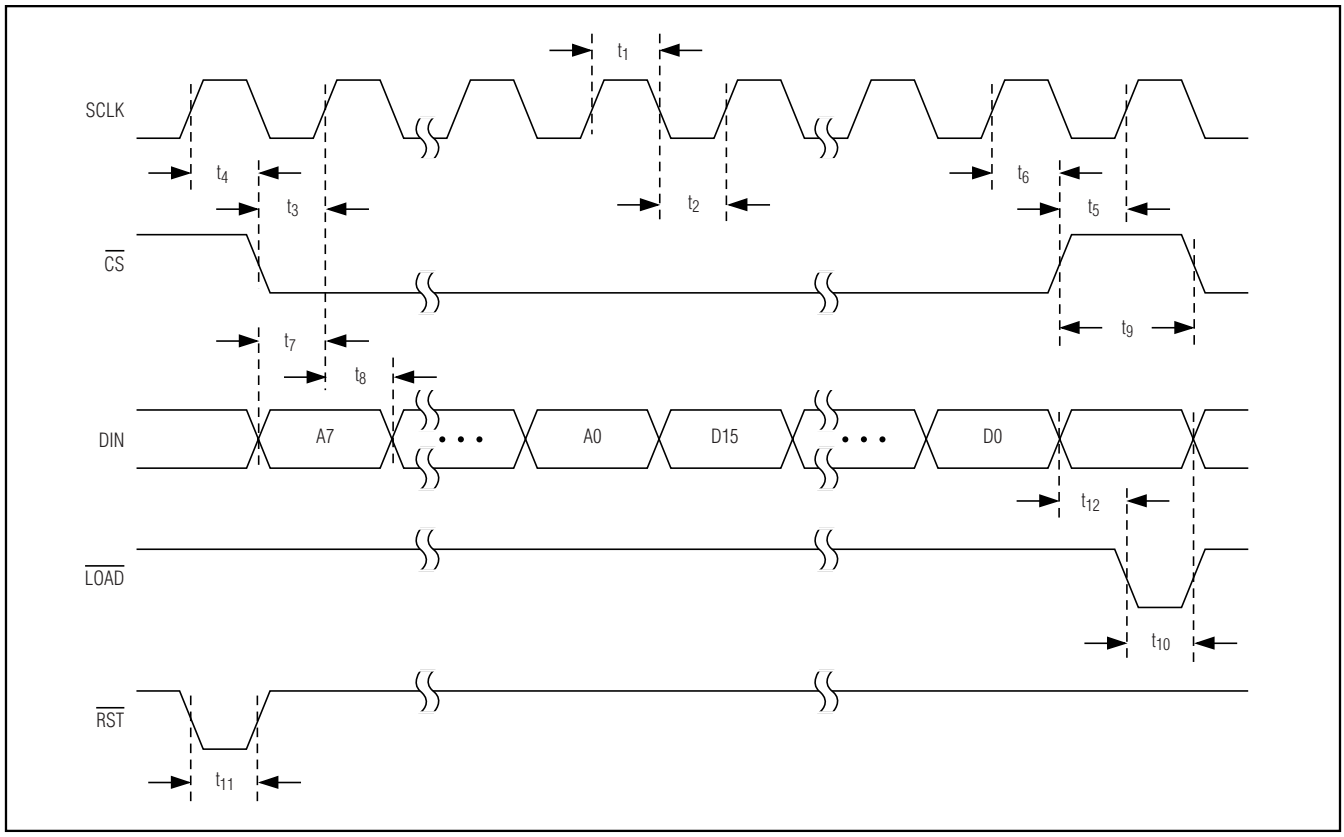


Figure 5. Serial-Interface Timing

High-speed differential inputs RCV_/NRCV_ and DATA_/NDATA_, in conjunction with control bits TMSEL_, LLEAK_, and LDEN_, manage the features of each channel. $\overline{RST}$ sets LLEAK = 1 for both channels, forcing both channels into low-leakage mode; all other bits are unaffected. At power-up, hold $\overline{RST}$ low until V_{CC} and V_{EE} have stabilized.

Serial Communication

Figure 5 and the serial port timing section of the *Electrical Characteristics* table show the serial interface timing requirements. Note that the first rising clock edge, after $\overline{CS}$ goes low, shifts in bit A7, and the last rising clock edge latches in bit D0. Forcing $\overline{LOAD}$ low then transfers the data from the serial input register to the DACs and DCLs.

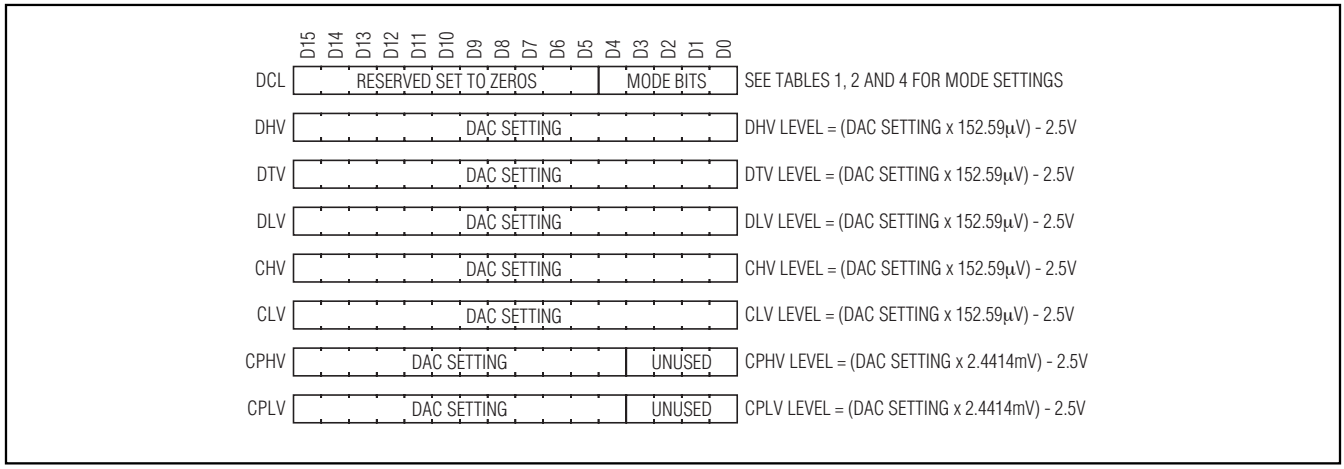


Figure 6. Register Data for DCL and DAC Programming

DACs as Driver Channel Inputs

Digital-to-analog converters, programmed through the serial interface, provide input voltages to the three input multiplexers (DHV_, DTV_, and DLV_), the clamps (CPHV_ and CPLV_), the comparators (CHV_ and CLV_), and the load (DTV_ doubles as the load input voltage source). Set the DAC output voltages as detailed in Figure 6.

Temperature Monitor

The MAX9973 supplies a temperature output signal, TEMP, that asserts a nominal output voltage of 3.43V at a die temperature of +70°C (343K). The output voltage changes proportionally with temperature at 10mV/°C, but is not calibrated.

Heat Removal

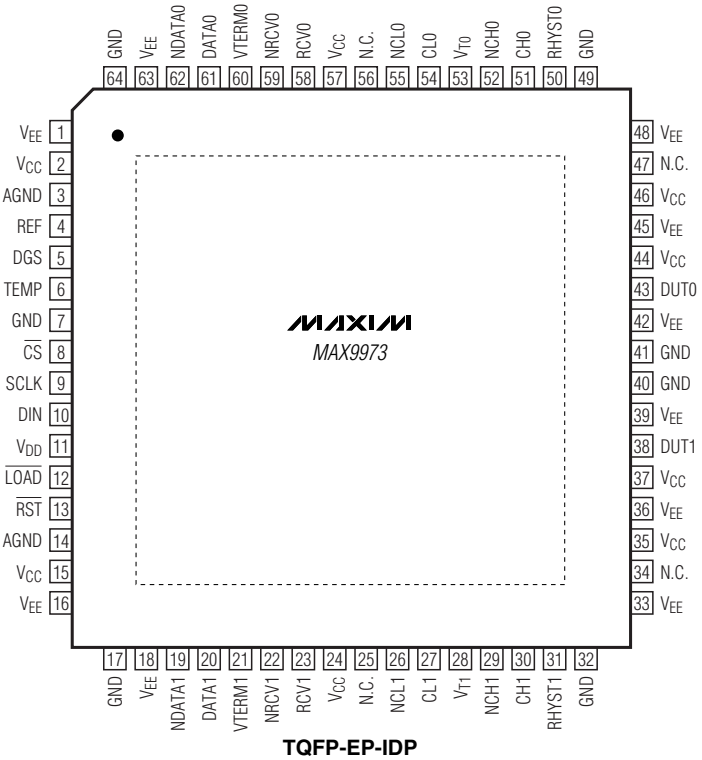
Under normal circumstances, the MAX9973 requires heat removal through the exposed paddle through the use of an external heat sink. The exposed paddle is electrically isolated from the die. Make no electrical connection to the exposed paddle.

Power-Supply Considerations

Bypass all V_{CC} and V_{EE} power pins each with a 0.01µF capacitor, and use bulk bypassing of at least 10µF on each supply.

Dual Driver/Comparator/Load with Internal DACs

Pin Configuration



TQFP-EP-IDP

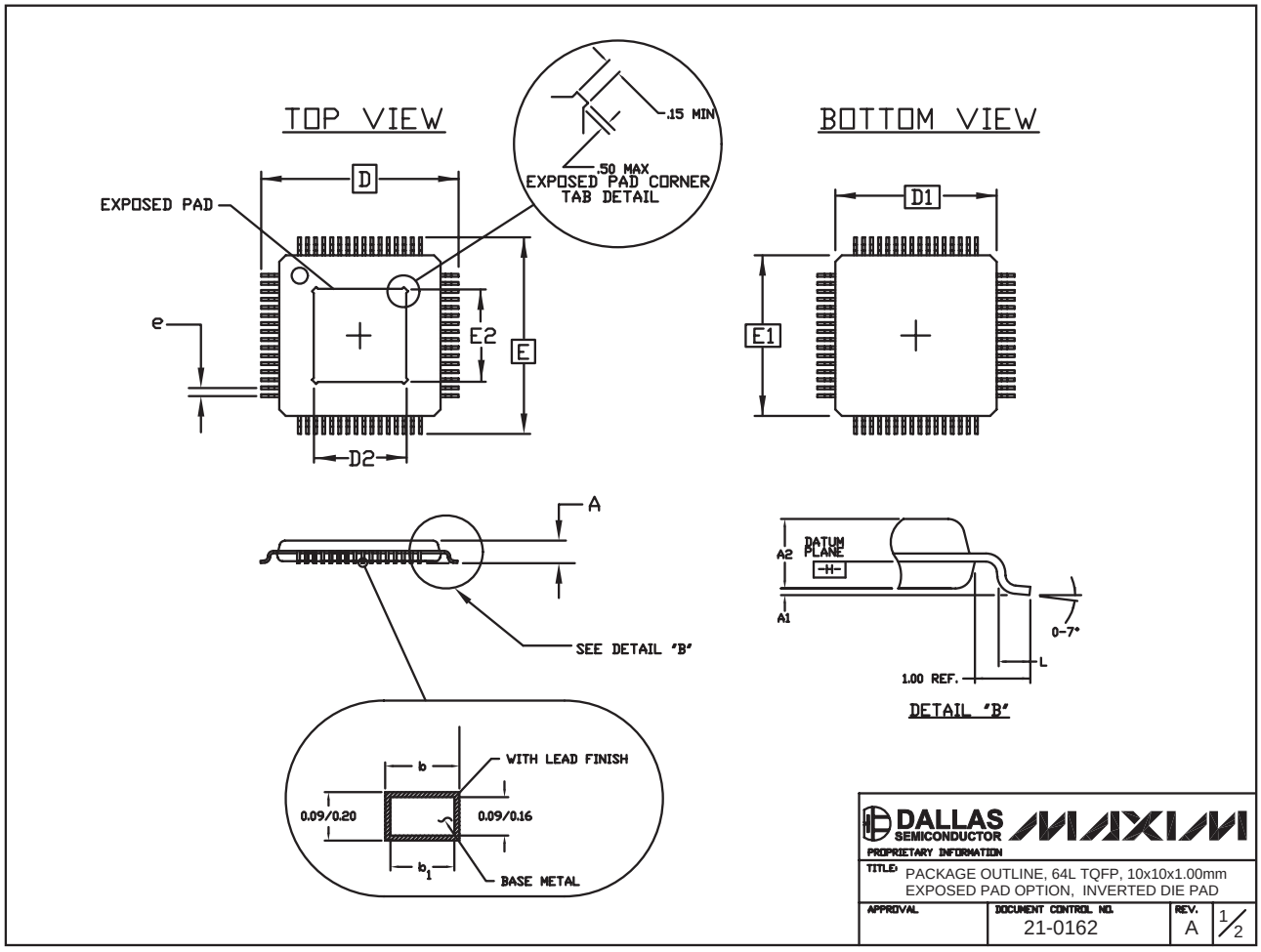
Chip Information

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

64L TQFP.EPS



Dual Driver/Comparator/Load with Internal DACs

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

NOTES:
1. ALL DIMENSIONS AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE [-H-] IS LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 MM ON D1 AND E1 DIMENSIONS.
4. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY AS MUCH AS 0.15 MILLIMETERS.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. CONTROLLING DIMENSION: MILLIMETER.
7. MEET JEDEC MS-026 EXCEPT FOR COPLANARITY (SEE NOTE 8).
8. LEADS SHALL BE COPLANAR WITHIN 0.10 MM.
9. EXPOSED DIE PAD SHALL BE COPLANAR WITH BOTTOM OF PACKAGE WITHIN 2 MILS (.05 MM).
10. REFER TO PRODUCT DATA SHEET FOR PACKAGE CODE.

SYMBOL	COMMON DIMENSIONS ALL DIMENSIONS IN MILLIMETERS JEDEC VARIATION ACD	
	MIN.	MAX.
A		1.20
A_1	0.05	0.15
A_2	0.95	1.05
D	12.00 BSC.	
D_1	10.00 BSC.	
E	12.00 BSC.	
E_1	10.00 BSC.	
L	0.45	0.75
N	64	
e	0.50 BSC.	
b	0.17	0.27
b1	0.17	0.23

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
C64E-4R	4.7	5.0	5.3	4.7	5.0	5.3
C64E-9R	5.7	6.0	6.3	5.7	6.0	6.3

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 64L TQFP, 10x10x1.00mm EXPOSED PAD OPTION, INVERTED DIE PAD			
APPROVAL	DOCUMENT CONTROL NO. 21-0162	REV. A	2/2