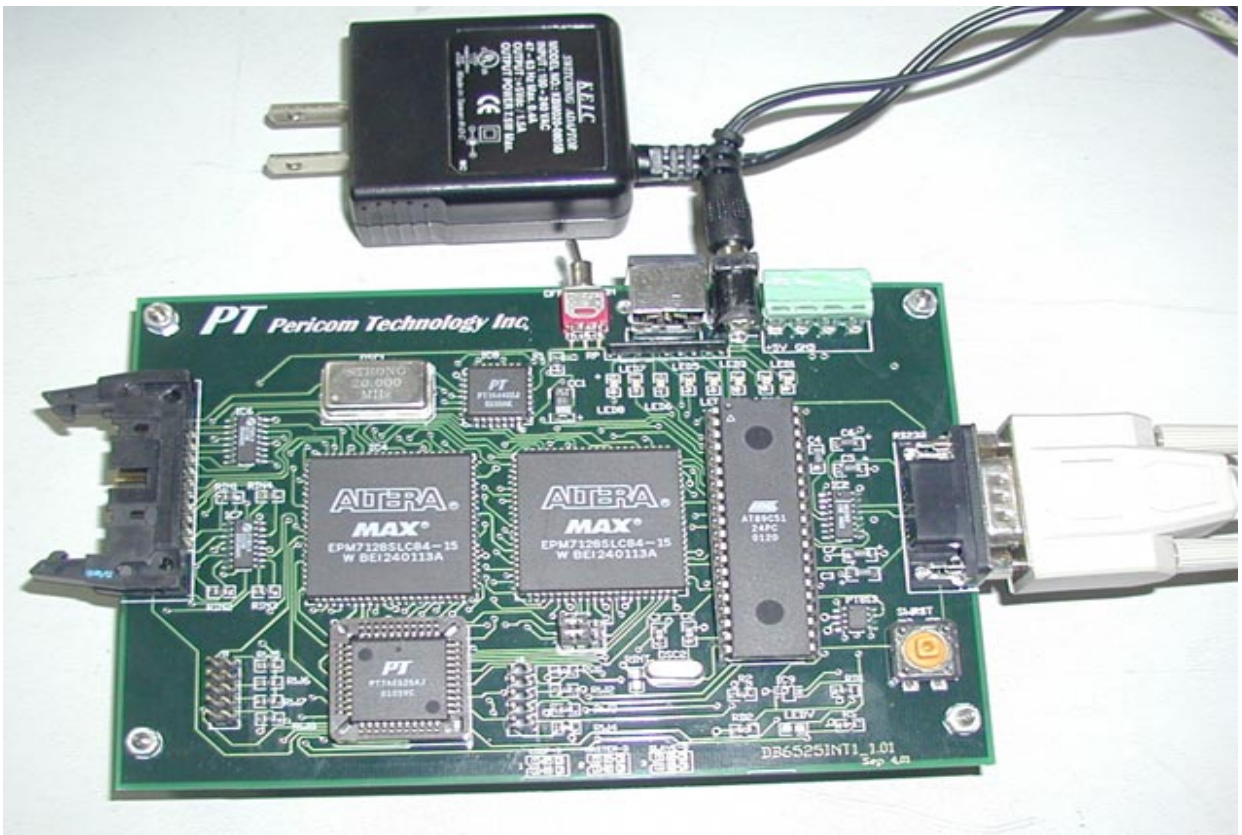
PT7A6525/6526 Demo Board Instruction



Brief

This application note describes a simple application demonstration for serial communication interface consisting of PT7A6525, AT89C51 (CPU) and PT7A4401 (clock circuit), etc. Since there is no long- distance driving circuit available, it only adapts to short-distance data communication with transfer rate up to 4Mbps. It demonstrates three typical functions of PT7A6525 in connection with AT89C51 and PT7A4401 consist of synchronous or asynchronous communications system in different clock modes, such as Clock Mode 1 and Clock Mode 5 for synchronous communications, and Clock Mode 3 for asynchronous communications.

This demo board adopts LVDS as its serial interface driver, it is suitable for flat-wire transmission and back-board driving, and it can be used at Point-to-Point configuration. The system utilizes PT7A4401's phase locked loop to operate in the synchronous communication mode, thus the master station supplies only one reference to the slave station. The slave station recovers the main clock and the synchronous signal from the reference clock.

The schematics and 89C51 Assemble Supervision Program of Demo Board are list in **Sch and Pro.pdf**.

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Introduction

This application note describes a simple application demo system for serial communication interface by using PT7A6525, AT89C51 and PT7A4401 (clock circuit). This combination system can operate in Clock Mode 1, Clock Mode 3, and Clock Mode 5 of PT7A6525/6526 by revising EPLD's internal logic and setting software. It can also operate in the address recognition mode and the non-address recognition mode by rewriting the mode register of PT7A6525/6526.

This application note also describes how to set registers of PT7A6525 for adapting to the different operation modes, and how to observe the status of the PT7A6525/6526 via PC.

Functional Description

Refer to the functional block diagram in Figure 1.

The computer (PC) communicates with the monolithic processor (AT89C51) via RS232, and AT89C51 accesses directly HDLC (PT7A6525/6526) according to instructions from PC, i.e., PC can control PT7A6525 indirectly, receiving/transmitting message from/to PT7A6525/6526 via AT89C51. In other word, PC can reliably communicate with each other via HDLC (PT7A6525) serial interface, the serial data meets with HDLC protocol. The reliabilityof serial communication is improved by the HDLC, and the software cost is greatly reduced.

Figure 1. Functional Block Diagram of Demonstration System

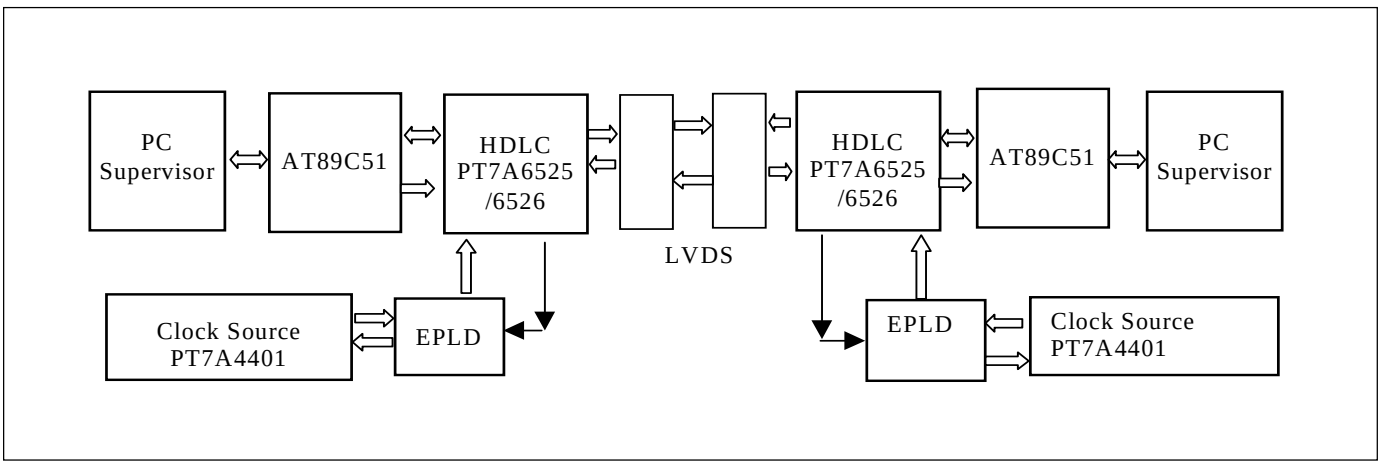


Figure 2. HDLC data format

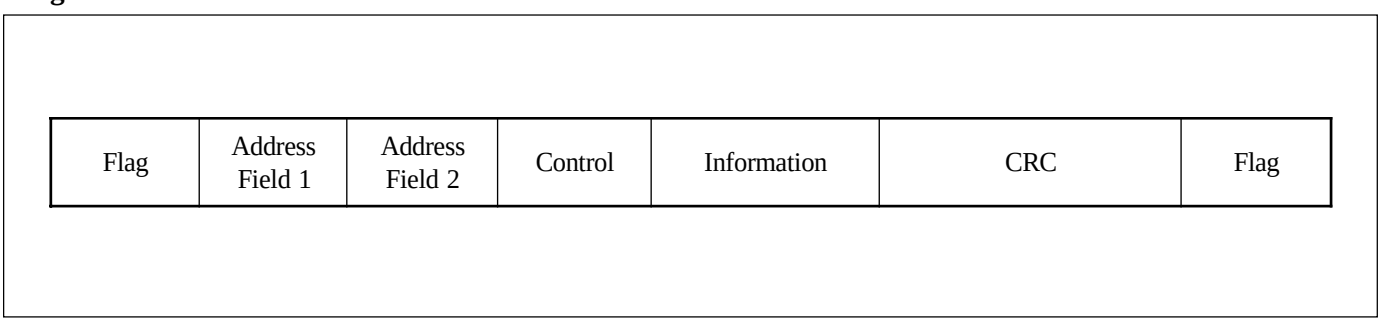
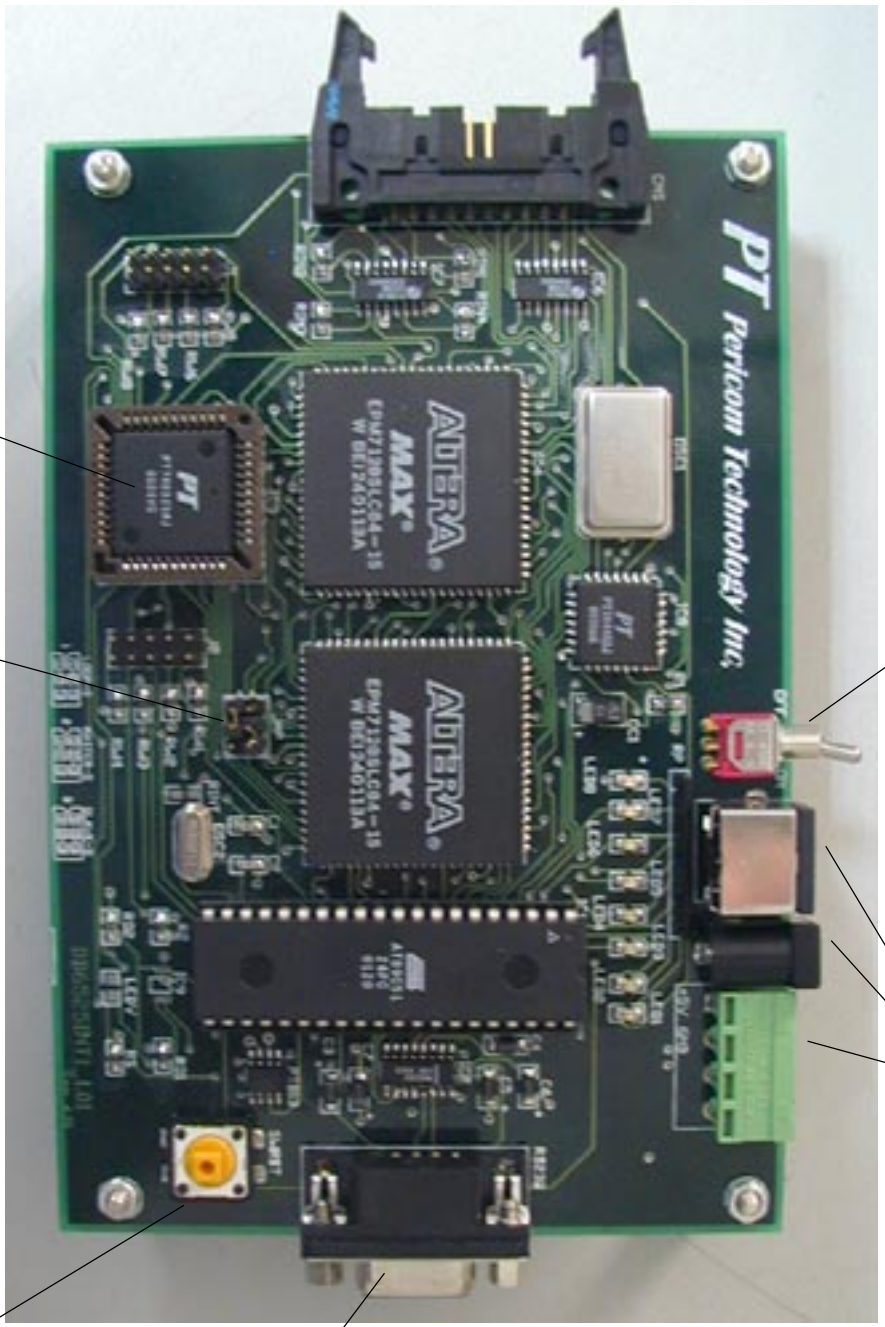


Figure 3. Overview of Demonstration Board for PT7A6525/6526

LVDS Driver Interface For HDLC Serial Link



PT7A6525/PT7A6526

PT7A6525/6526 is the key part in this system. Its functions are introduced in the following paragraphs.

The demonstration system can operate in the different clock modes. These operation modes are changeable by revising EPLD and rewriting the register contents of PT7A6525/6526.

For Clock Mode 1, Master clock (4.1MHz) is applied to RxCLK, transmission strobe signal is applied to TxCLK, receive strobe signal is applied to AxCLK. The binary data "10011001" should be written into channel configuration register 1 (CCR1). Thus TxD pin is a push-pull outputs; continuous flag sequence ("01111110" pattern) is output during the interframe fill. Data rate up to 8.192MHz can be performanced via modifying EPLD.

For Clock Mode 3, Master clock(4.1MHz) is applied to RxCLK, this mode is an asynchronous communication, it can recover the receive clock from the received data stream. CCR1 register should be initialized as "10011011".

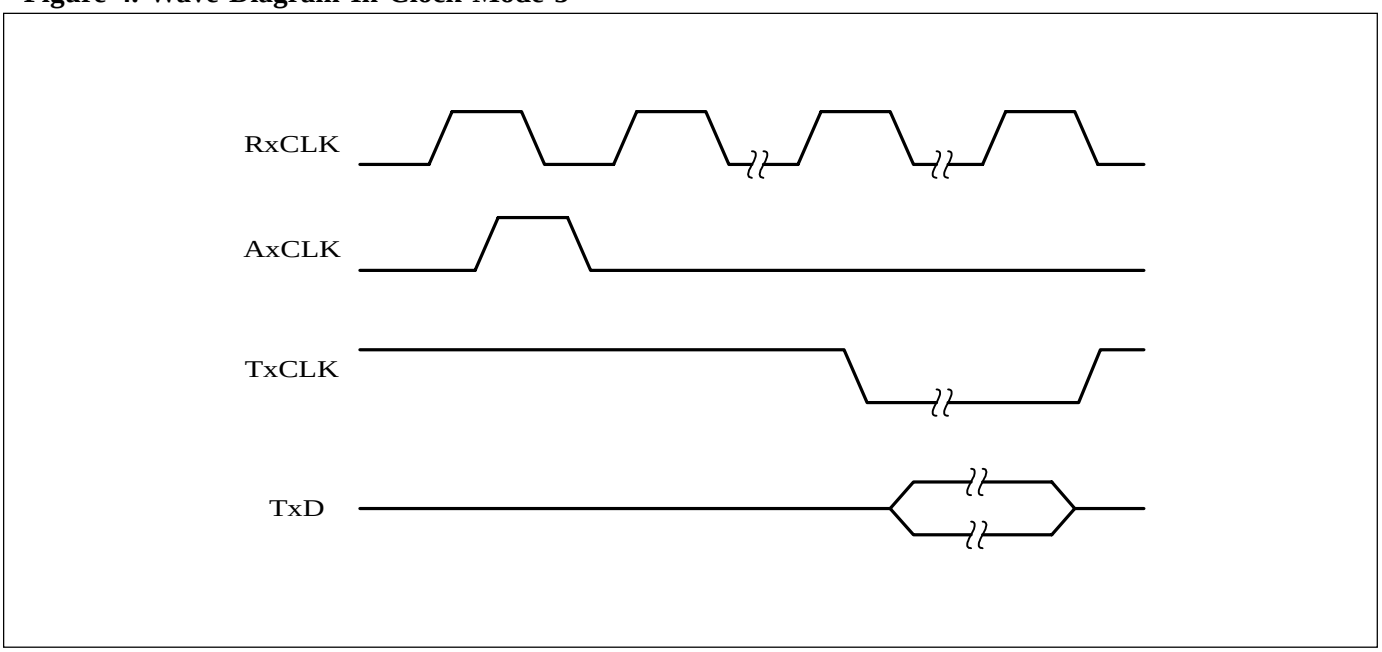
For Clock Mode 5, Master clock(4.1MHz) should applied to RxCLK, a frame SYNC signal(8kHz) is applied to AxCLK. CCR1 should be initialized as "10011101", and TIO bit in channel configuration register 2 should be set.

In Clock Mode 5, one of up to 64 time-slots can be programmed independently for transmit and receive directions via transmit time-slot assignment register (TTSA) and receive time-slot assignment register (RTSA). The time-slot width (1 to 256 bit) of receive and transmit directions can be programmed via transmit channel capacity register and receive channel capacity register. But transmit and receive location with respect to the frame synchronization signal is decided by the combination of TTSA, RTSA and CCR2 (details see datasheet), i.e., start of transmit and receive are delayed with respect to the frame synchronization signal by programming TTSA, RTSA and CCR2 registers.

When TIO in CCR2 is set, TxCLK output (active low) indicates transmit time-slot.

Figure 4 shows link signal timing in Clock Mode 5.

Figure 4. Wave Diagram In Clock Mode 5



Principle of Demo System

PC transmits address/data message of registers to the AT89C51 via RS232 serial interface, and then AT89C51 writes these data to the registers or XFIFO of PT7A6525 according to the instructions from PC, thus PT7A6525 can be initialized indirectly, and the information is sent to opposite HDLC via HDLC. In turn, the local computer can receive message from the opposite computer.

The link operation principle is described in the following paragraphs.

There are several link operation modes-- Auto Mode, Non-auto mode, Transparent mode, Extended Transparent mode. The operation mode is selected via initializing bit "MDS1, MDS0 and ADM" in mode register (MODE) of PT7A6525.

Auto-Mode

When MDS1 MDS0 ADM = 000, it is in Auto Mode with 8-bit address field recognition, i.e., the first received address field is compared with register RAL1 (receive address low 1) and RAL2 (receive address low 2). If the address is recognized as valid, this frame information will be accepted.

When MDS1 MDS0 ADM = 001, it is in Auto Mode with 16-bit address field recognition, i.e., the first received address field is compared with register RAH1 (receive address high), RAH2 and the fixed values #FEH #FCH, the second address field is compared with register RAL1 and RAL2. Only the information with valid address will be accepted.

When transmitting I-frame, the address field transmission is implemented via register XAD1 (transmit address 1) and register XAD2 (transmit address 2).

When transmitting transparent-frame, the address field transmission is implemented via XFIFO.

The control field is generated automatically. I-frame is transmitted via XIF in command register (CMND), bit XTF of CMND can also initiate transmitting transparent frame in Auto Mode. Figure 5 shows frame format in Auto Mode.

Non-Auto Mode

When MDS1 MDS0 ADM = 010, it is in Non-Auto Mode with 8-bit address field recognition.

When MDS1 MDS0 ADM = 011, Non-Auto Mode with 16-bit address field recognition.

The address recognition ways are the same as in Auto Mode except that the transmit address is implemented via XFIFO (the first and second address fields).

In Non-Auto Mode, only transparent frame is transmitted. Figure 6 shows frame format in Non-Auto Mode.

Figure 5. Frame Format In Auto Mode

Flag	Address Field 1	Address Field 2	Control	Information	CRC	Flag

MDS1 MDS0 ADM = 000

Flag	RAL1 RAL2	Null	RFIFO RHCR	Information	CRC	Flag

MDS1 MDS0 ADM = 001

Flag	RAH1 RAH2	RAL1 RAL2	RFIFO RHCR	Information	CRC	Flag

Figure 6. Frame Format In Non-Auto Mode

Flag	Address Field 1	Address Field 2	Control	Information	CRC	Flag

MDS1 MDS0 ADM = 010

Flag	RAL1 RAL2	Null	RFIFO RHCR	Information	CRC	Flag

MDS1 MDS0 ADM = 011

Flag	RAH1 RAH2	RAL1 RAL2	RFIFO RHCR	Information	CRC	Flag

Transparent Mode

When MDS1 MDS0 ADM = 100, it is in Transparent Mode without address recognition.

When MDS1 MDS0 ADM = 101, it is in Transparent Mode with high address recognition, i.e., the first received address field is compared with RAH1 and RAH2 values. Only the frame with valid address will be accepted.

Figure 7 shows the frame format in Transparent Mode

Figure 8 shows the transparent frame format in Non-Auto Mode and Transparent Mode. XTF in command register initiates the transmission.

Clock Modes

PT7A6525/6526 has 8 clock modes: Clock Mode 0, Clock Mode 1, Clock Mode 2, Clock Mode 3, Clock Mode 4, Clock Mode 5, Clock Mode 6 and Clock Mode 7. They require different clock sources and control sources (strobe signal).

Clock Mode 0, Clock Mode 1 and Clock Mode 5 are mainly applied to the high data rate communication system. These clock modes need a complex circuit configuration.

Clock Modes 2, 3, 4, 6 and 7 are mainly applied to the low data rate communication systems. These clock modes need a simple circuit configuration .

This application note describes applications of Clock Mode 1, Clock Mode 3 and Clock Mode 5.

Figure 7. Frame Format In Transparent Mode

Flag	Address Field 1	Address Field 2	Control	Information	CRC	Flag

MDS1 MDS0 ADM = 100

Flag	RAL1 RFIFO	RFIFO RHCR	RFIFO	Information	RFIFO CRC RSTA CRC	Flag

MDS1 MDS0 ADM = 101

Flag	RAH1 RAH2	RAL1 RFIFO	RFIFO RHCR	Information	RFIFO CRC RSTA CRC	Flag

Figure 8. Transmitted Transparent Frame Format In Non-Auto Mode And Transparent Mode

. Flag	Address Field 1	Address Field 2	Control	Information	CRC	Flag
Flag	Address XFIFO	Address XFIFO	Control XFIFO	Information XFIFO		Flag

Figure 9. Transmitted I-Frame Format In Auto-Mode

Flag	Address Field 1	Address Field 2	Control	Information	CRC	Flag
Flag	Address XAD1	Address XAD2	Control Auto	Information XFIFO		Flag

• Clock Mode 1

When in Clock Mode 1, RxCLK must be connected to an external clock source, TxCLK to a transmission strobe signal and AxCLK to a receive strobe signal. This mode can be applied in time division multiplex applications or adjusting disparate transmit and receive data rate configuration. Maximum frequency of RxCLK is 8.192MHz. It is a synchronous communication. When TxCLK and AxCLK are not used, they must be tied to Vcc.

The CCR1 (Channel configuration register 1) determines which clock mode is chosen. Each bit of CCR1 is defined as Figure 10 (details sees data sheet of PT7A6525/6526).

Figure 10. Bit Definition of CCR1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PU	SC1	SC0	ODS	ITF/OIN	CM2	CM1	CM0

Note:

1. PU = 0, power down (standby); PU = 1, power up (active).
2. SC1 SC0 = 00, NRZ data encoding; SC1 SC0 = 10, NRZI data encoding; SC1 SC0 = 01, bus configuration, timing mode 1; SC1 SC0 = 11, bus configuration, timing mode 2.
3. ODS = 0, TxD pins are open drain outputs (when in bus configuration); ODS = 1, TxD pins are push-pull outputs.
4. ITF/OIN: interframe time fill/one insertion
5. CM2 CM1 CM0: Clock mode selection, 000 - clock mode 0; 001 - clock mode 1; ...; 111 - clock mode 7.

• Clock mode 3

PT7A6525/6526 offers the advantage of recovering receive clock from the received data stream by internal DPLL circuitry, thus no additional clock information needed via the serial link.

In Clock Mode 3, the receive and the transmit clock sources come from DPLL. DPLL's reference source comes from RxCLK. Thus baud rate factor is set as "1", RxCLK divided by 16 is data rate, and the receive station and the transmit station may have no phase relationship. This is an asynchronous communication. The maximum data rate is 1.2Mbits/s (RxCLK = 19.2MHz).

When the clock is generated internally, the device can operate in the other clock mode, such as clock mode 6 and clock mode 7. The internal clock is generated by connecting a crystal between pin AxCLKA and pin RxCLKA. Both channel A and channel B adopt AxCLKA and RxCLKA for crystal connection.

• Clock mode 5

In clock mode 5, main clock (RxCLK) and frame synchronizing signal (AxCLK) need be supplied. This mode is mainly used in synchronous communication system. The maximum data rate is 4.1Mb/s. The transmission time-slot and receive time-slot are programmable. So it can be applied in time-slot oriented PCM system.

Hardware Principle

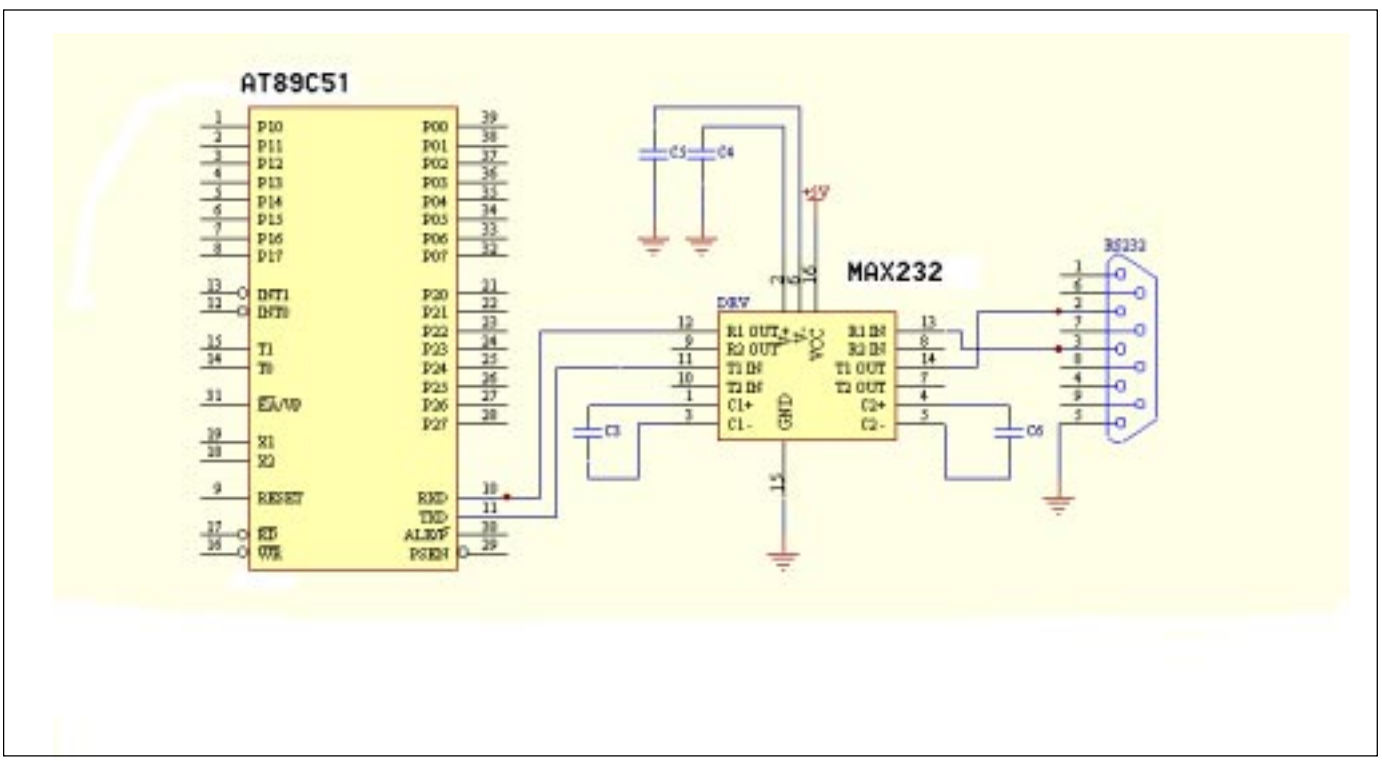
Communication between PC and AT89C51

The computer and AT89C51 communicate with each other via RS232. Figure 11 shows the schematic diagram.

MAX232 is a level transfer and drive circuit for RS232 interface. It includes DC/DC internally.

To use MAX232CPE, C3, C4, C5 and C6 are 1uF respectively; To used MAX232A or MAX202, C3, C4, C5 and C6 are 0.1uF respectively.

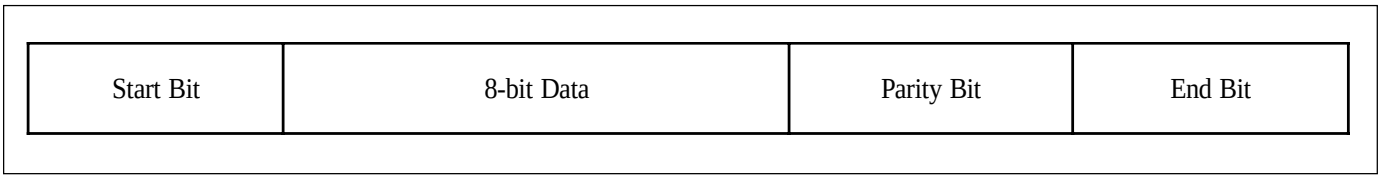
Figure 11. Schematic Diagram of Microprocessor and AT89C51



• RS232 Serial Communication Interface mode setting:

Computer (PC) sets COM1 or COM2 11-bit format per frame as shown in Figure 12.

Figure 12. Serial Frame Format



Computer (PC) sets COM baud rate to 19200. Data are received in either interrupt way or inquiry way, i.e., acknowledging interrupt signal or inquiring status register. Computer reads/write the data from/to the receive/transmit buffer .

• AT89C51 serial communication interface mode setting:

The serial data format is the same as that of RS232 by setting the AT89C51's SCON register and making serial interface in operation mode 3. Baud rate is implemented by setting Timer 1. Set Timer 1 in its operation mode 2 (auto-load time constant).

To generate 19200bps(baud rate), an 11.0592MHz crystal oscillator is adopted, and time constant value is FDH (FDH is written to TH1 and TL1).

AT89C51 adopts interrupt way or inquiry way to read the data from RS232 interface, i.e., it accepts Buffer Full Interrupt or inquires RI (if receive buffer is filled) to start data reading.

AT89C51 serial interface SCON and Timer 1 are set by the following program:

```
MOV  TMOD, #20H          ; SET TIMER AS TIME MODE 2
MOV PCON,#80H            ;
MOV  TL1, #0FDH          ; LOAD TIME CONSTANT
MOV TH1, #0FDH
SETB TR1                 ;START TIMER
MOV  SCON,  #0D0H        ;SET SERIAL INTERFACE MODE 3
```

Interface between AT89C51 and HDLC(PT7A6525)

Figure 13 shows connection between AT89C51 and PT7A6525.

/CS pin of the PT7A6525 is connected to P20 pin of the $\overline{AT}$89C51, so that the register and FIFO address of the PT7A6525/6526 is from 100H to 1FFH, namely the original register address of the PT7A6525/6526 plus 100H. For example, original address 6FH turns out 16FH (6FH+100H). On the demo board, the /$\overline{CS}$ of the PT7A6525/6526 is connected to ground, so its address is the same as the original address in the data sheet.

Connecting IM1 to ground, the CPU interface of PT7A6525/6526 will operate in INTEL bus mode.

If data transfer is performed in interrupt mode, an interrupt signal will be sent to AT89C51 by PT7A6525. AT89C51 reads the interrupt status register and finds out the cause of the interrupt, then the interrupt service program in AT89C51 will accomplish the data transfer requested by PT7A6525.

Figure 13. Connection between PT7A6525/6526 and CPU

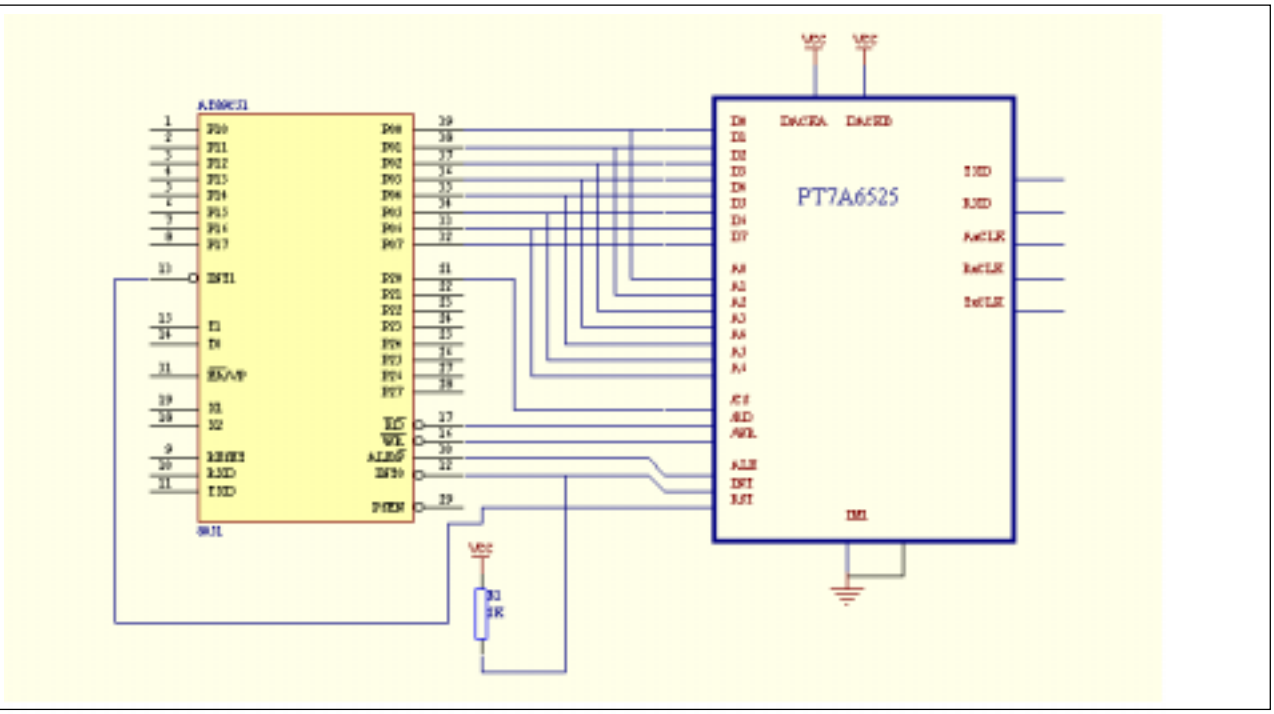
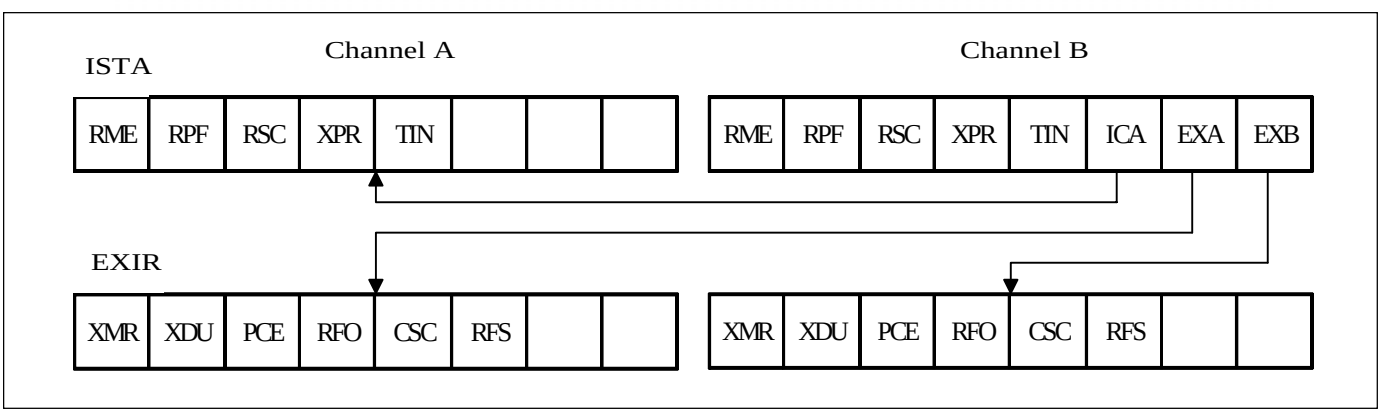


Figure 14. Interrupt Status Register Assignment



The data transmission and receive are executed by inquiring STAR and RSTA registers.

The details of bit functions of the STAR in application are explained as follows.

XDOV	XFW	XRNR	RRNR	RLI	CEC	CTS	WFA

XDOV: when XDOV = 1, transmit data overflow, i.e., more than 32 bytes have been written into XFIFO and cause data loss.

XFW: when XFW = 1, XFIFO is empty and data can be written into XFIFO.

XRNR: it indicates the status of HDLC: 0 - receiver ready; 1 - receiver not ready (valid in Auto Mode only).

RRNR: it indicates the status of the remote station: 0 - receiver ready; 1 - receiver not ready (valid in Auto Mode only).

RLI: when 1, it indicates neither FLAGs as interframe time fill nor frames are received via the receiver.

CEC: when 0, no command is currently executed and the CMND register can be written; when 1, a command is currently executed, no more command can be written at present via CMND register. This bit is mainly used to query if the current command is executed.

CTS: when the CIE bit in CCR2 is set, this bit indicates the state of CTS pin: 0 - high level at CTS pin, inactive; 1 - low level at the CTS pin, active.

WFA: when 1, indicates waiting for acknowledgment status.

More details of RSTA register can be found in datasheet of PT7A6525/6526.

The functions of RSTA register are explained as follows:

This register is mainly used to judge validity of current received frame, overflow of receive data, CRC check/ comparison, abortion of received message. If abortion is identified, this frame will be discarded by the CPU.

In address recognition mode, it can indicates if the valid address is detected.

When a frame has been received, the RSTA should be read to determine this frame is valid or invalid.

Demo Board

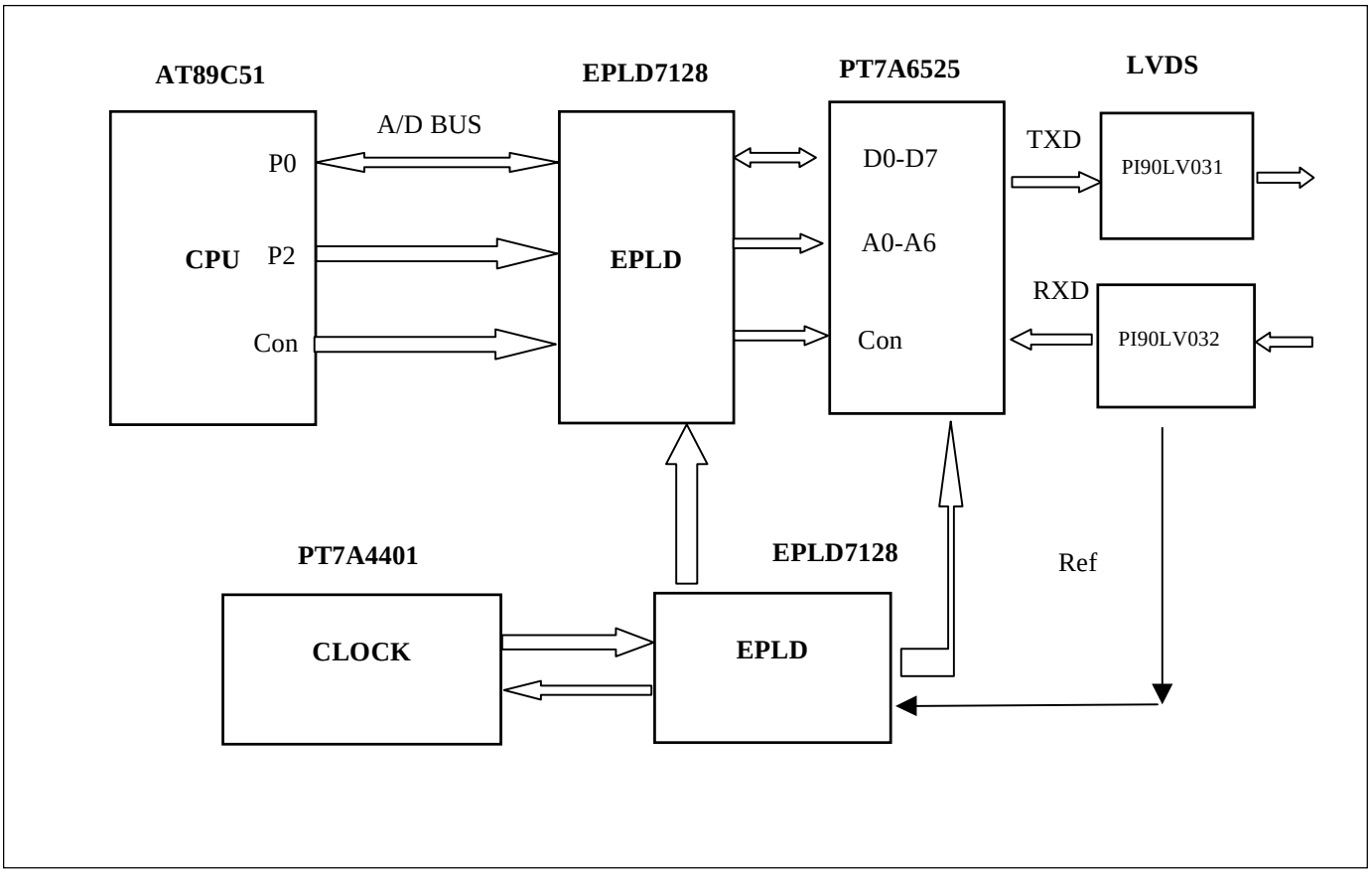
Figure 15 is the block diagram of the demo board.

It is possible to adapt the demo system to a selected operation mode by setting up proper hardware connection and revising the EPLD, including such opetation modes as clock modes, strobe signals and CPU interfaces.

By appending delay gates to EPLD, it can offer various signals for PT7A6525 to realize various setup and hold time, thus the tolerance of setup time and hold time can be measured.

The logic diagram of AT89C51 and PT7A6525 interfacing to the EPLD is illustrated in Appendix D.

Figure 15. Block Diagram of Demo Board



Software Functions

In order to debug PT7A6525 easily, PC can be arranged to control AT89C51 in the demo system. As PC can read/ write all the registers of PT7A6525/6526 indirectly via RS-232 interface, the contents of registers can be directly displayed on screen of PC. It is possible to set various operation modes by writing the registers of PT7A6525, simultaneously, EPLD can be modified.

Appendix C is a PC program flow diagram . Its operation is depicted in chapter “Operational Guide of Demo System” in the following pages.

Appendix B is an AT89C51 supervisory Program . Its main function is to receive control information from PC and transmit information from PT7A6525/6526 to PC. Thus it can make control over PT7A6525/6526 according to PC’s instructions.

The functions of the PC programs are as follows:

1. Select operation modes by rewriting the register contents.
2. Write transmitted information to transmit FIFO.
3. Write command to CMND register for resetting transceiver and starting information transmission.
4. Read register contents for arranging PT7A6525 /6526.
5. Read RFIFO.
6. Transmit/receive information to/from HDLC (PT7A6525/ 6526).

Operational Guide of Demo System

Hardware Configuration

Two boards can communicate with each other in the demo system, they are completely identical. To operate it, jumper(JMP) must be set on the demo board, it decides which board supplies reference clock as system synchronous clock, thus only one board is set as master station, the other one is set as slave station.

How To Connect The Demo Boards

Figure 16 shows how to connect the demo system.
The computer can exchange information with the other computer via COM1,COM2 and demo board.

Note: Plugging or unplugging the connector to PC with power-on may cause damage to system.

Each demo board has a RS232 9-pin connector. The pin definition is as follows:

pin 2: TxD
pin 3: RxD
pin 5: GND

The pin definition of the connector on demo board is the same as a DCE.

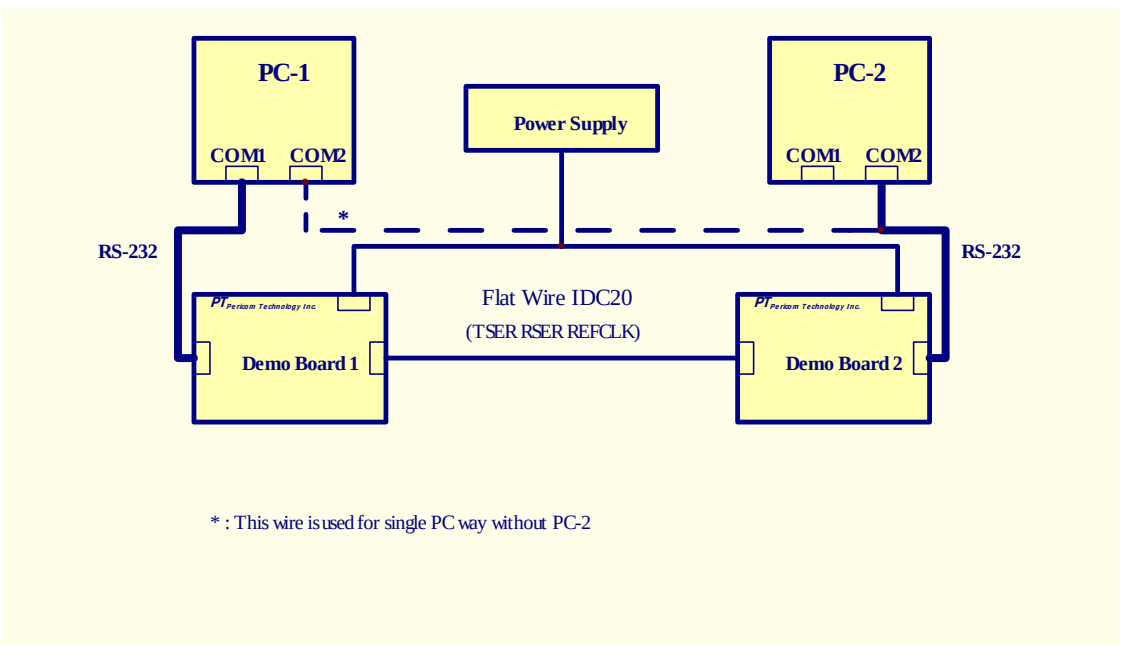
If the demo board is connected to a 9-pin connector of the COM1 or COM2 port of PC, the pin connection between the PC and the demo board is as follows:

PC Port	Demo Board Connector
pin 2	pin 2
pin 3	pin 3
pin 5	pin 5

If the port of PC is a 25-pin connector, the pin connection is as follows:

PC Port	Demo Board Connector
pin 2	pin 3
pin 3	pin 2
pin 7	pin 5

Figure 16. Demo System Connection Block Diagram for Single PC or Dual PCs



IDC20 Connector between Two Demo Boards

Two demo boards are connected with each other by an IDC20 flat wire. The IDC20 connector transfers Reference clock and TxD/RxD data between the two demo boards in LVDS level.

When a pair of connectors are connected by flat wire, the pin 1 of one connector must be connected to the pin 20 of the other connector, and pin 2 to pin 19, etc.
IDC20 Pins configuration:

Pin 1 and Pin 2	RXDB difference input
Pin3 and Pin 4	Ref CLK difference input
Pin 5 Pin 6 Pin 7 Pin 8 Pin 13 Pin 14 Pin 15 Pin 16	reserved
Pin 9 Pin 10 Pin11 Pin12	Ground
Pin 17 And Pin 18	Ref Clk difference output
Pin 19 and Pin 20	TXDB difference output

Power Connector

The power connector is to connect ground and +5V power supply. The pins' mark can be found on the board near to the connector.

Reset Button

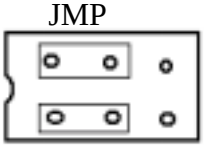
Reset button is used to reset the demo board. When press Reset Button, AT89C51 and PT7A6525/6526 will be reset, and AT89C51 will initialize PT7A6525/6526 registers. This process can be found in the program of AT89C51. PT7A6525 is operated in clock mode 1 and transparent mode 0, PT7A6525/6526 is at power-up, NRZ encoding state. TxD pins are push-pull outputs. All mode can be verified via reading CCR1 CCR2 MODE register etc.

To test more modes of PT7A6525/6526, the registers should be setup manually and EPLD need be setup again. The user can change the contents of registers by demo program.

Jumper

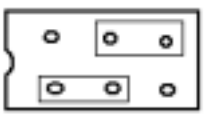
Jumper Function It is set as J-A or J-B for adapting Master Station or Slave Station. Master station supplies system reference clock, Slave station recover synchronous clock via reference clock.

JMP



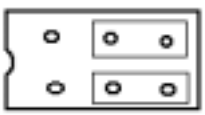
J-A Single Board Loop Mode

JMP



J-B Two Boards Master Station

JMP



J-C Two Boards Slave Station

Note: When single board operates in loop mode, JMP must be set as J-A;

When two boards communicate with each other, JMP must be set as J-B and J-C.

Software

In general, operation flow is as follows:

1) Select Hardware setup to adapt to desired clock mode.
2) Initialize registers of the PT7A6525/6526 (select desired operation mode).
3) Read the interrupt status register (decide what to do next after current status).
4) Write data to XFIFO.
5) Write command to CMND register (optional).
6) Read interrupt status register (judge if receive and transmit completed) (optional).
7) Read RFIFO (optional).

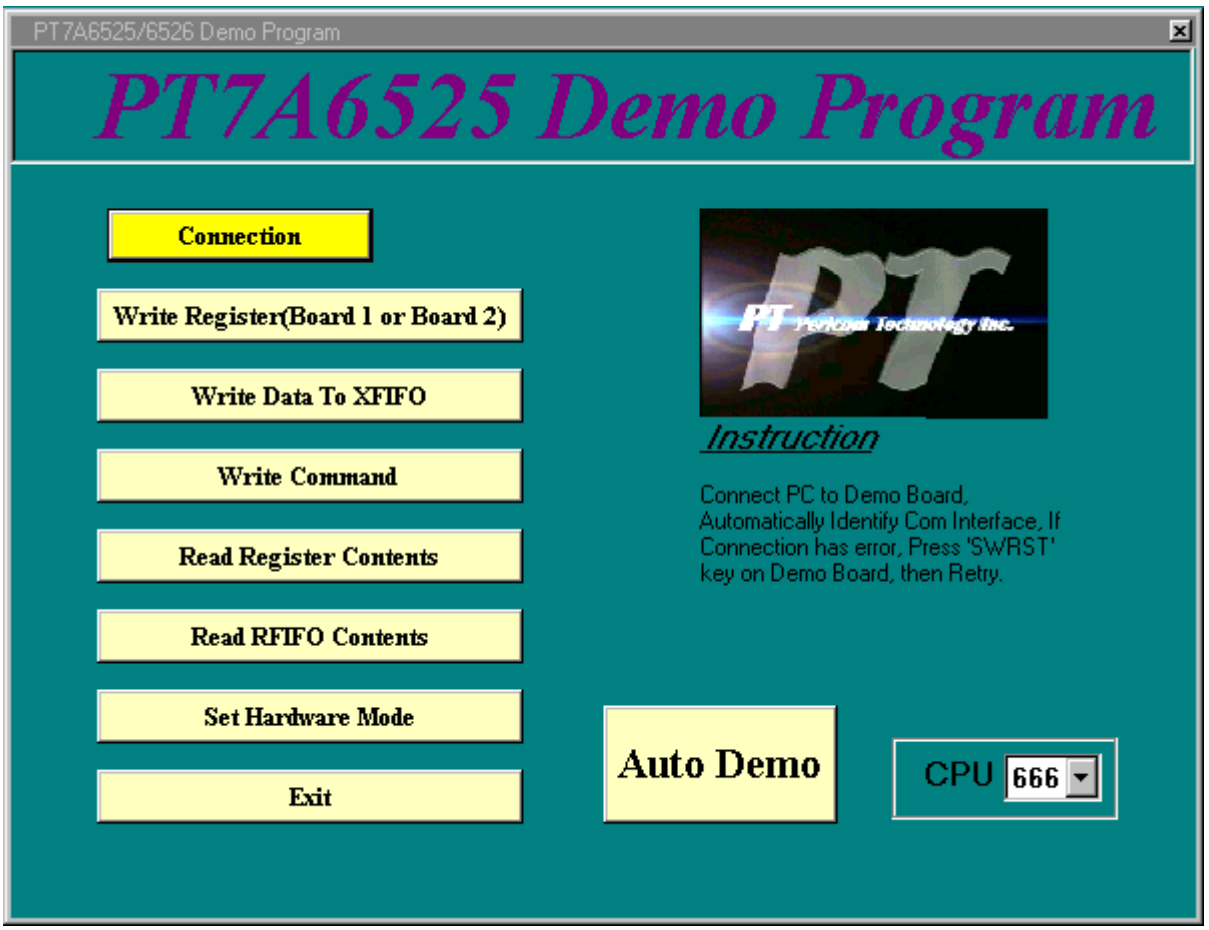
Main Menu

After connecting the demo system according to Figure 16, run file “Demo6525.exe ”, it is for windows 98.
Figure 17 shows Main Menu.

In order to make connection between PC and Demo Board. At first, click “Connection” button, Connection Result will be shown on screen.
Figure 18 shows Connection Information.
If connection has error, Press SWRST key on demo board, and then retry connection.

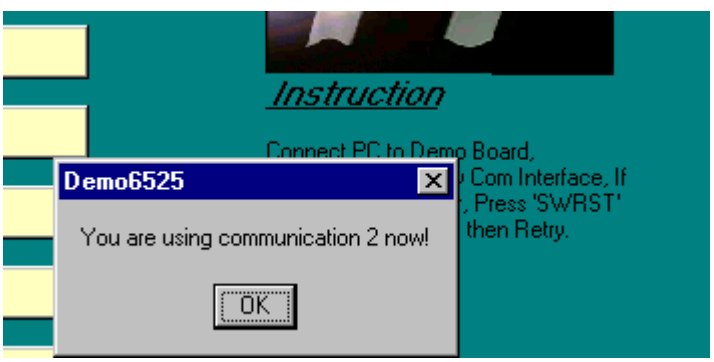
Now you can control PT7A6525/6526 via clicking the different button on the main menu.
Click Button “Write Register”, All the writable register will be shown on screen, and initial contents will be shown simultaneously. Figure 19 shows Write register window.

Figure 17 Main Select Item Menu



Note: Re-write CPU speed according to your PC's CPU type.

Figure 18 Connection Between PC and Demo Board



Now you can control PT7A6525/6526 via click different buttons on the main menu.

Write Register

Click Button "Write Register" will display all the writable registers . Figure 19 shows Write register window.

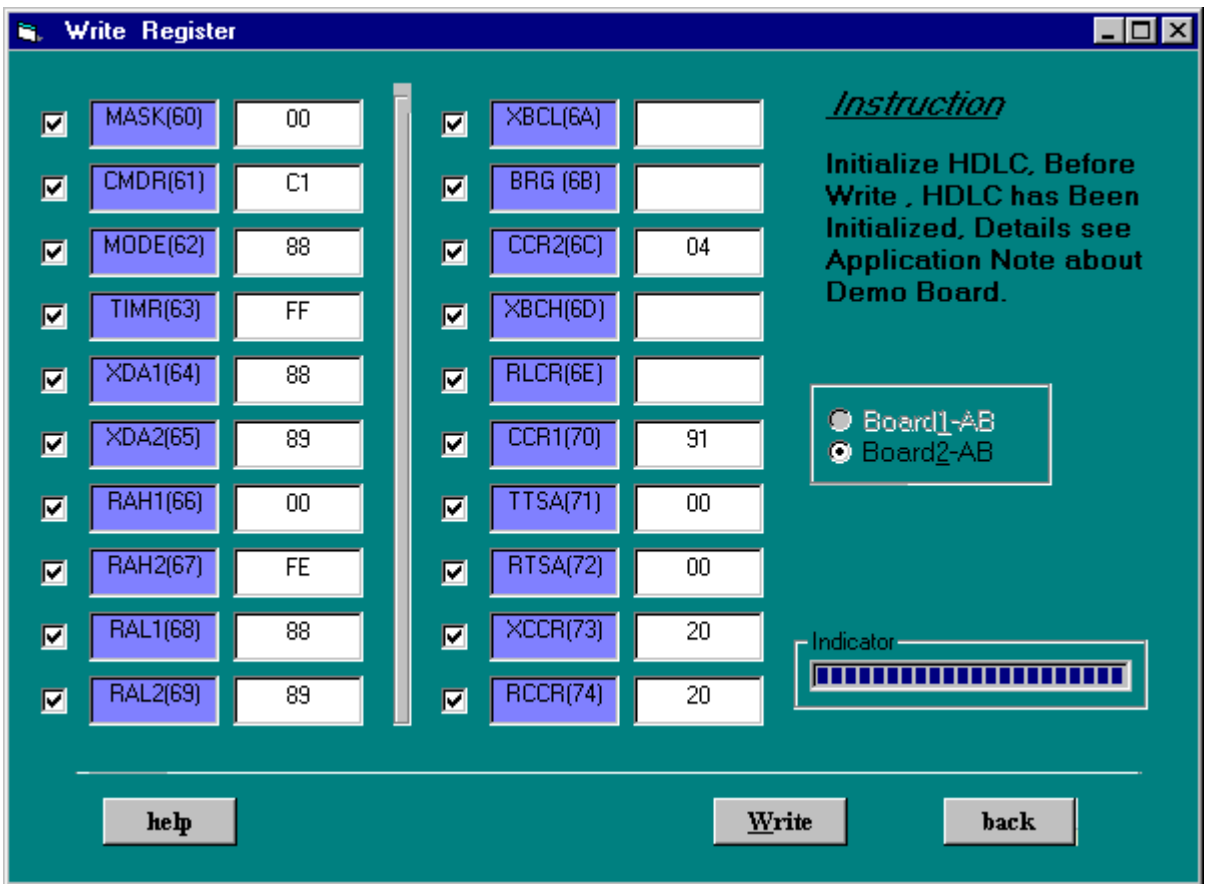
The register contents displayed is the same as initialization contents when Reset Demo board.

Write Register operating Flow:

1. Click option button on the left of register to be written.
2. Modify the content of the register.
3. Select board No.(Board 1 or Board2)
4. Click Write button, finish the writting process.

Note: Data to be written is HEX format

Figure 19. Write Register Window



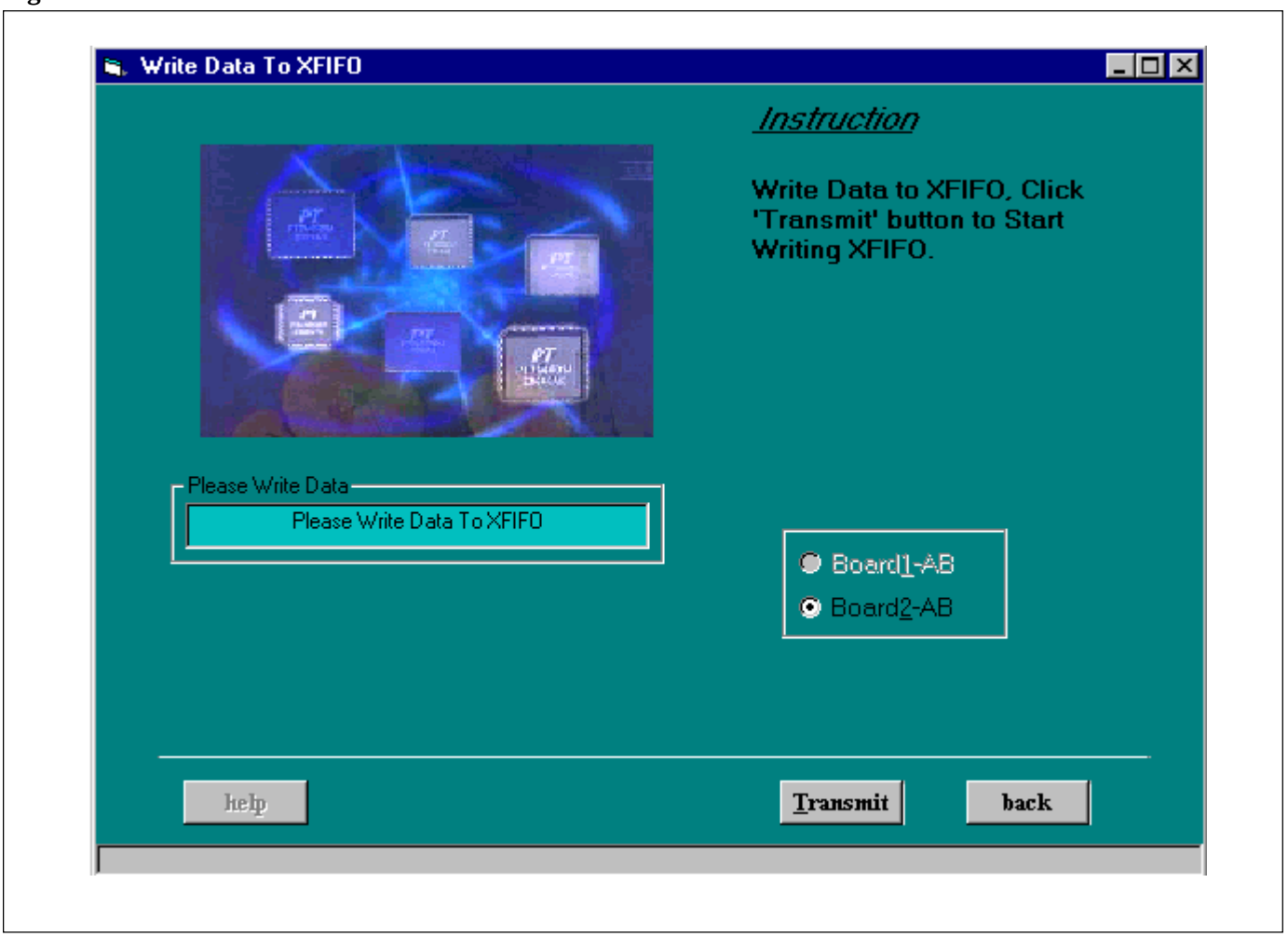
Write XFIFO

Click “WR Data” button will switch to Write XFIFO window, Figure 20 shows the writting XFIFO windows. In the window, it can write information to XFIFO. Up to 31-Bytes can be written to XFIFO.

Its writting flow is as the following:

1. Write information to textbox
2. Click Option button to select Board No.
3. Click transmit button, finish writting XFIFO process.

Figure 20. Write XFIFO Window



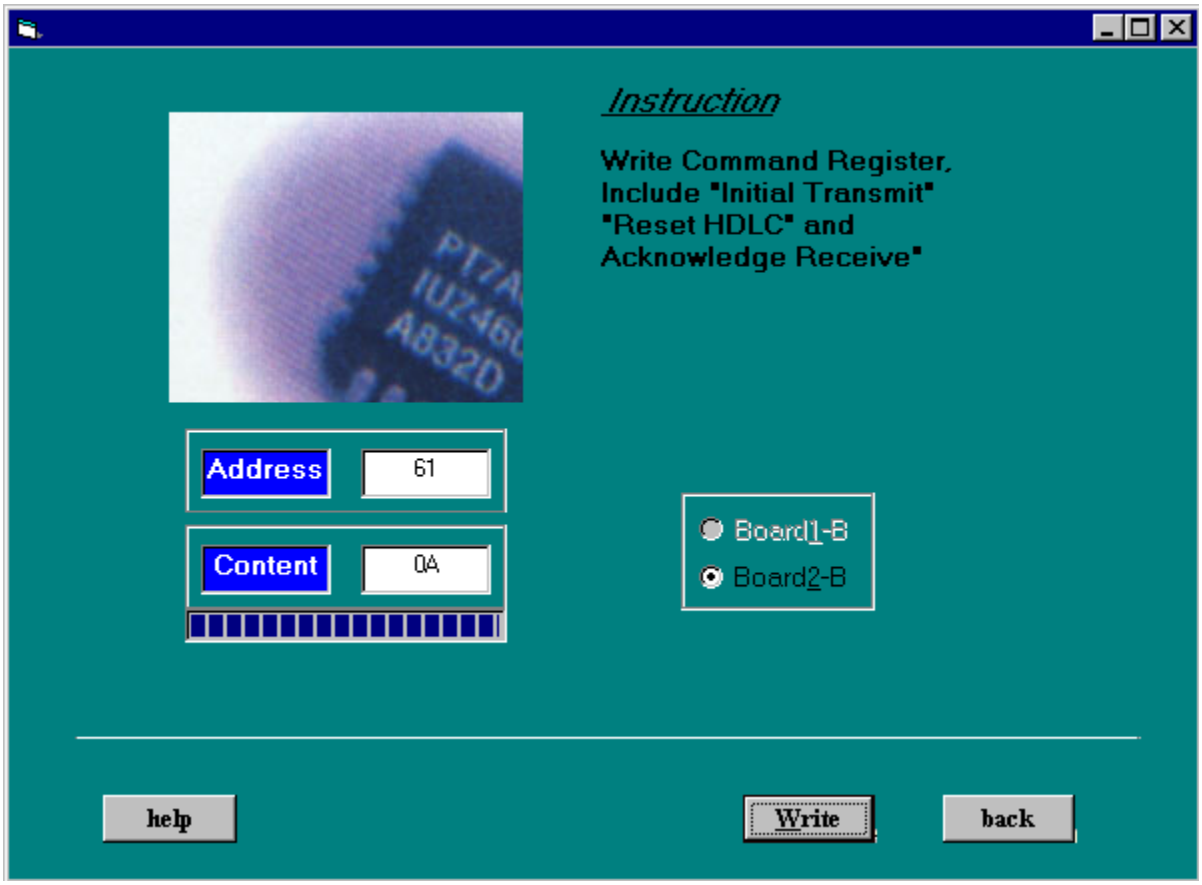
Write Command Register

Any writable register can be written in this window.

The default is B-channel's CMDR, transmit the last information.

Figure 21 shows Write Register Window

Figure 21 Write Command Register



Read Register Content

All readable registers can be shown in this window. STAR RSTA and ISTA are usually read in operation, their contents can decide the next step.

Figure 22 shows Read Register Window

Read Register Flow is shown as the following

1. Click Option Button for selecting Board No (1,2) and Channel No(A,B. A for only PT7A6525)
2. Click Read Button to finish Read Register Process.

Figure 22. Read Register Content

Read RFIFO

Click RD FIFO button, figure 24 will be shown .

To read RFIFO

when ISTA and RSTA indicate RFIFO has been filled, the contents of RFIFO can be read.

Note 1: ISTA is the channel's interrupt status register, its content includes the information about receiving interrupt, such as reaceive message end, receive pool full and so on. its format is hex, Hex(91)=Binary(10010001).

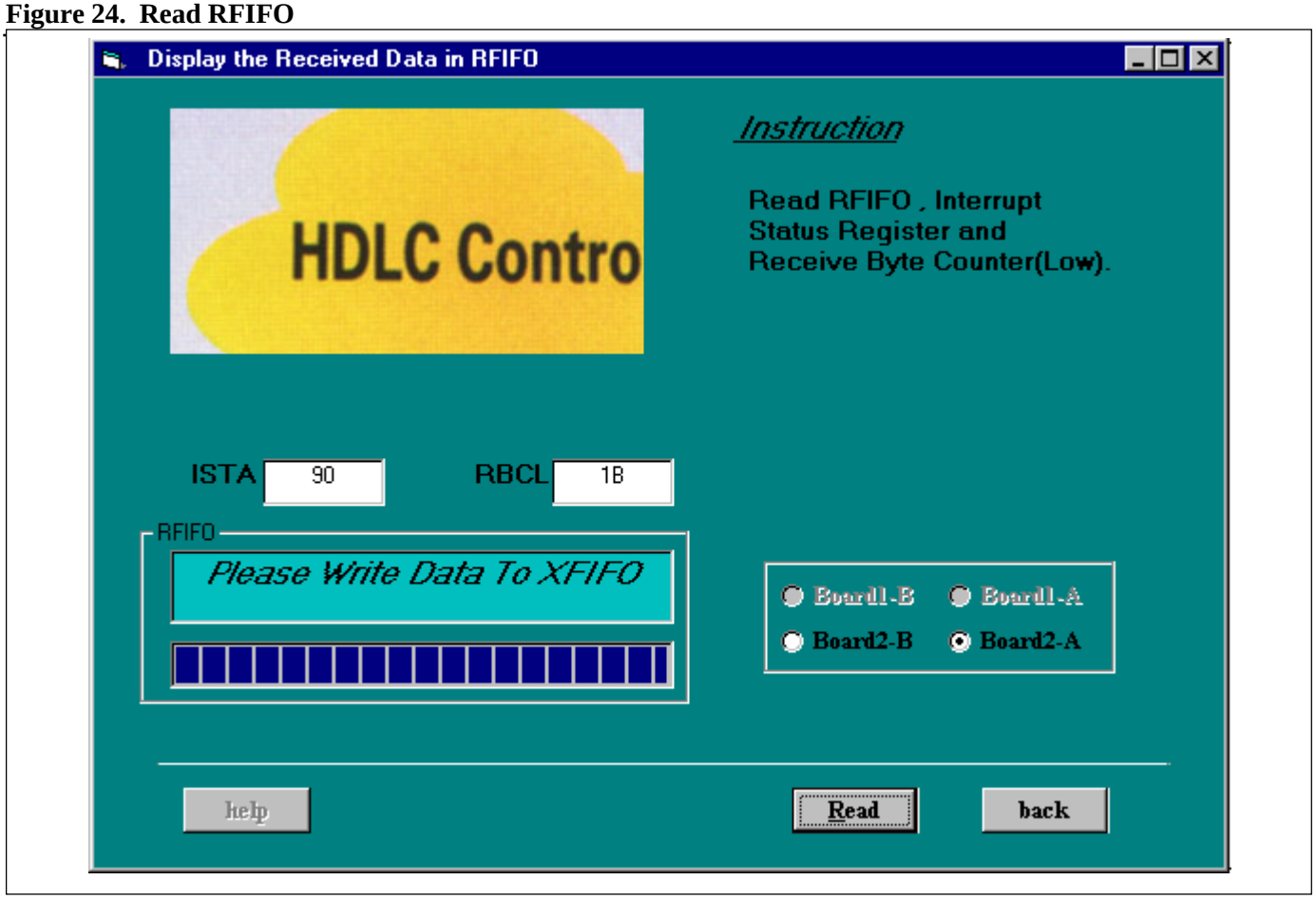
Note 2: Reading ISTA resets ISTA.

Note 3: RBCL is receive byte counter low 8-bit. it indicates message length in RFIFO, Its format is hex too, Hex(17)=Decimal(23), thus there are 23 characters received in RFIFO.

Read RFIFO flow is shown as follows:

1. Click option button to select receiving board No(1,2) and channel no(A,B). When two boards communicate each other, the receiving channel is B_channel. When single board loops, the receiving channel is A-Ch.
2. CLick read button to start reading RFIFO.

Figure 24. Read RFIFO



Setup Hardware Configuration of a Clock Mode

Function Description

Figure 25 shows Set Hardware window

Click button “Set M-1”, set hardware configuration as clock mode 1, and simultaneously modify CCR1’s Content for meeting with Clock mode 1. This result can be verified via Read Register.

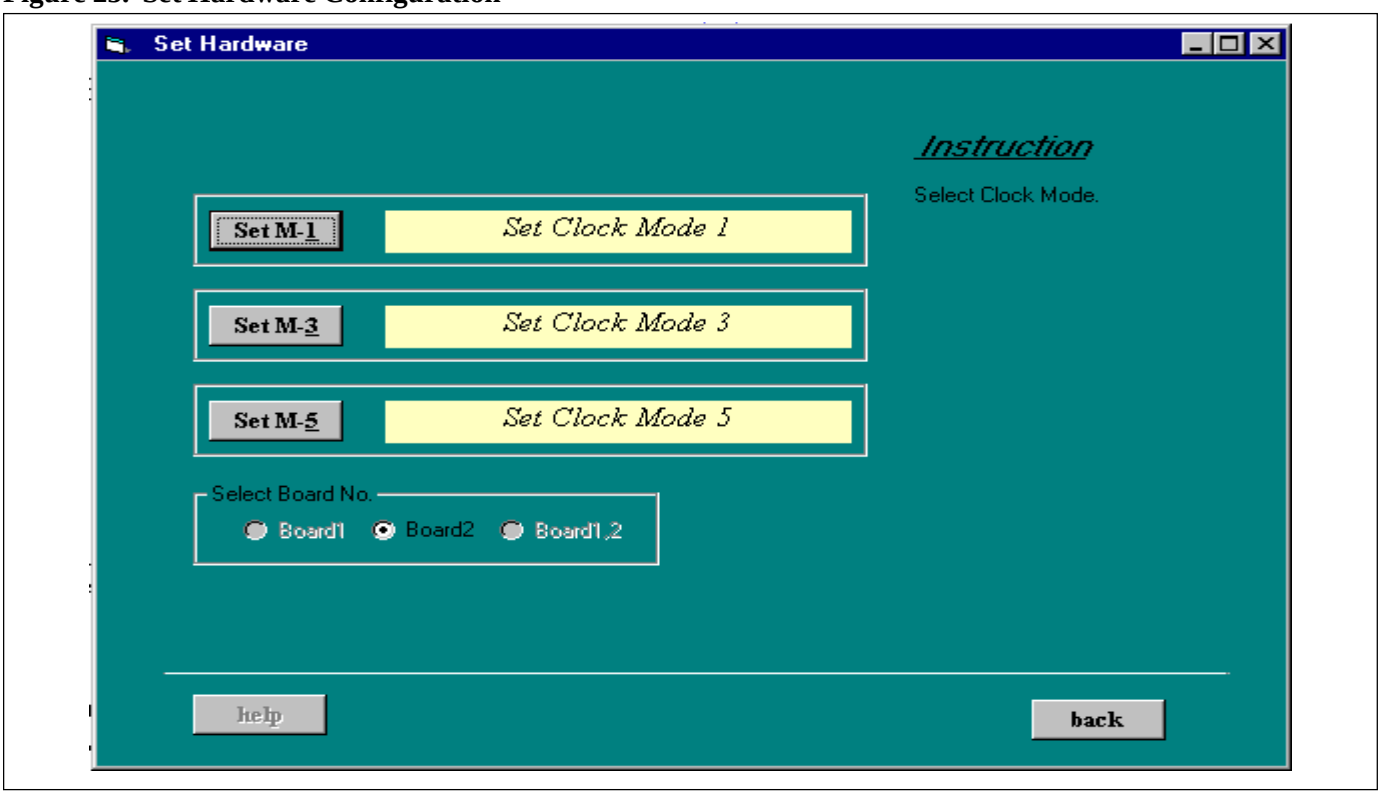
Click Button “Set M-3”, set hardware configuration as clock mode 3, and simultaneously modify CCR1’s content for meeting with clock mode 3. This result can be verified via Read Register. Clock Mode 3 can illustrate clock abstract function via DPLL of PT7A6525.

Click Button “Set M-5”, set hardware configuration as clock mode 5, and simultaneously modify CCR1’s content for meeting with clock mode 5. This result can be verified via Read Register.

Clock Mode 5 is mainly aplied in Oriented-PCM TDM System.It can transmit any bits up to 256 in any one of 64 time slot.

It is possible to re-write several registers-RCCR/TCCR/ RTSA/TTSA for meeting with time slot and Channel Capacity.

Figure 25. Set Hardware Configuration



Note:1. When only one serial communication, one board can perform simple demo, here B-Ch transmits information, A-Ch receives information. So this configuration is very suitable for verifying control register function.

Note 2. The Board connected to COM1 is defined as Board 1.
The Board connected to COM2 is defined as Board 2.

Examples

Example 1 Connecting PC to Demo Board

1. Press “SWRST” Key on the Demo Board;
2. Click Button “Connection” on Main Menu;
3. Demo Program can automatically identify COM1 or COM2 interface, and the connection information will be shown on the screen.

Example 2 Auto Demo**(Note 1)**

This process is that PT7A6525 B_channel transmits the data, PT7A6525 A_channel receives data from B_channel, JMP is set at single board loop mode. Operation flow is as follows:

1. Click Button “Auto_Demo” to begin Auto_Demo Process;
2. Click Button “Set M-1” “Set M-3” or “Set M-5” for selecting Clock Mode, this process will automatically set hardware and register with repect to Clock Mode, click Button “next” to next step;
3. Write the data(You are welcome) to XFIFO in textbox, then click Button “transmit” to start writing XFIFO, Click Button “next” to next step;
4. Read register to know the status of PT7A6525, select channel A or channel B, click Button “read”, analyze the contents of CCR1, Mode, ISTA etc. Click Button “next” to next step;
5. Write Command Register to initiate transmitting, Default “0A” is to transmit complete transparent frame, Click Button “write” to begin transmitting, Click Button “next” to next step.
6. Read the data from RFIFO, Click Button “Read” to show the contents of RFIFO on screen, the contents of RFIFO should be the string “You are welcome”. Click Button “finish” to return.

Example 3 Two PCs communication with each other

Each Board is separately connected to Com1 or Com2 on the difference PC. **(Note 2)**

Software operating flow is similar to Example 2.

1. Click Button “Set Hardware Mode” to select Clock Mode;
2. PC1 Writes data(You are welcome) to XFIFO of Channel_B.
3. PC1 Writes COMMAND to CMDR, start transmit ting.
4. PC2 reads RFIFO of Channel_B, The string “You are welcome” will be shown on screen.

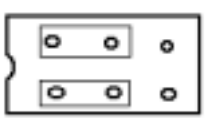
Example 4 Two Boards communication on one PC

Board 1 and Board 2 are separately connected to COM1 and COM2, and Jumper meets **Note 2.**

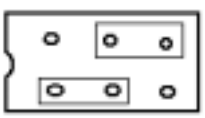
Software operating flow is similar to Example 3.

1. Click Button “Set Hardware Mode” to select Clock Mode, Board 1 and Board 2 have identical Clock Mode;
2. Board 1 Writes data(You are welcome) to XFIFO of Channel_B.
3. Board 1 Writes COMMAND(0A) to CMDR of Channel_B, start transmitting a complete transparent frame.
4. Board 2 reads RFIFO of Channel_B, the string “You are welcome” will be shown on screen.

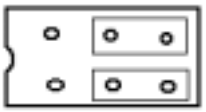
Note: 1 When the demo system is operated in single board loop mode, Jumper(JMP) should be set as follows:



Note 2 when two demo boards communicate with each other, Jumpers(JMP) is set as follows:



Master



Slave

Appendix A

Clock Modes and CPU Interface Connection

Figure 26 shows EPLD connection between PT7A6525 and AT89C51. Figure 27 shows clock source connection for Clock Mode 1, where TxD strobe signal (high active) and RxD strobe signal (high active) are both tied to high.

Figure 26. CPU Interfacing with EPLD Logic

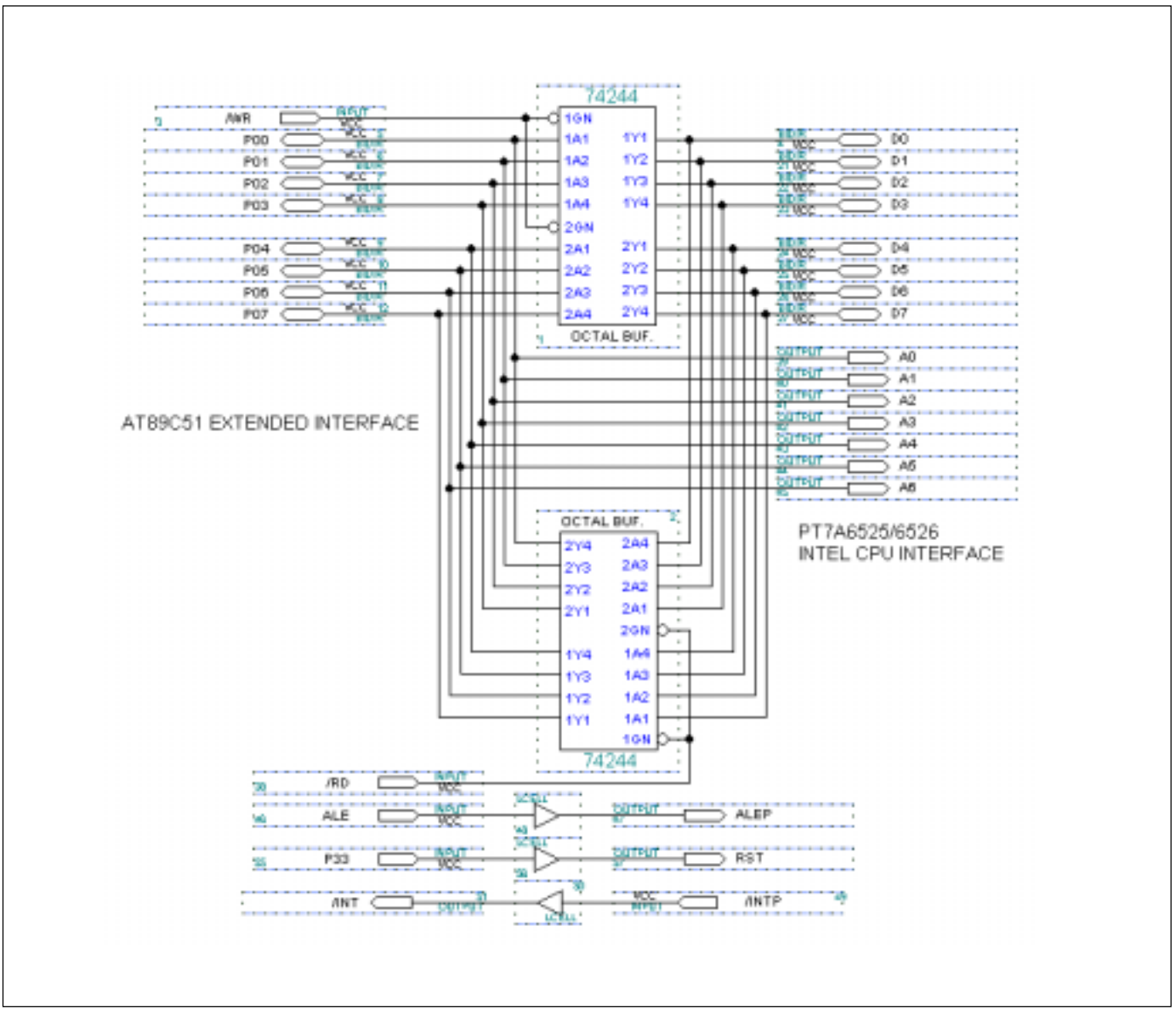


Figure 27. Clock Source Connection for Clock Mode 1

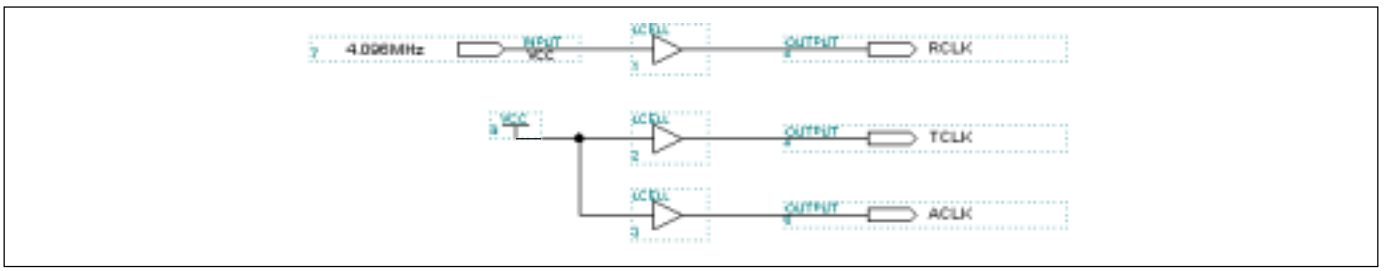


Figure 28 shows clock source connection for Clock Mode 3.

In clock mode 3, transmission clock and receive clock come from DPLL in PT7A6525/6526. The baud rate generator in PT7A6525/6526 supplies reference clock to DPLL. Refer to Figure 28a and Figure 28b. When baud rate factor is set to 1, transmission and receive data rate will be 1/16 RxCLK. For example, if RxCLK is 8.192MHz, data rate is 512kbit/s.

Figure 28a. Block Diagram of Clock Signal Direction

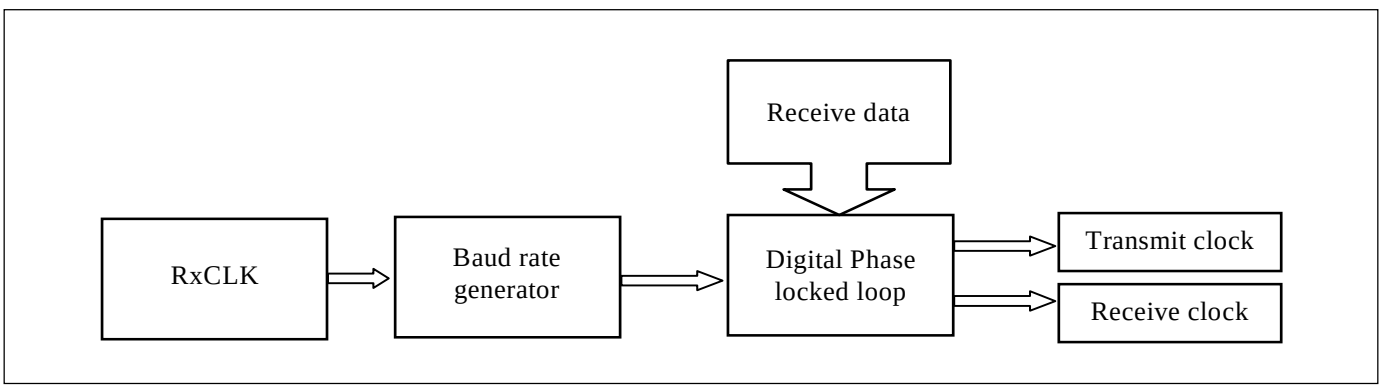
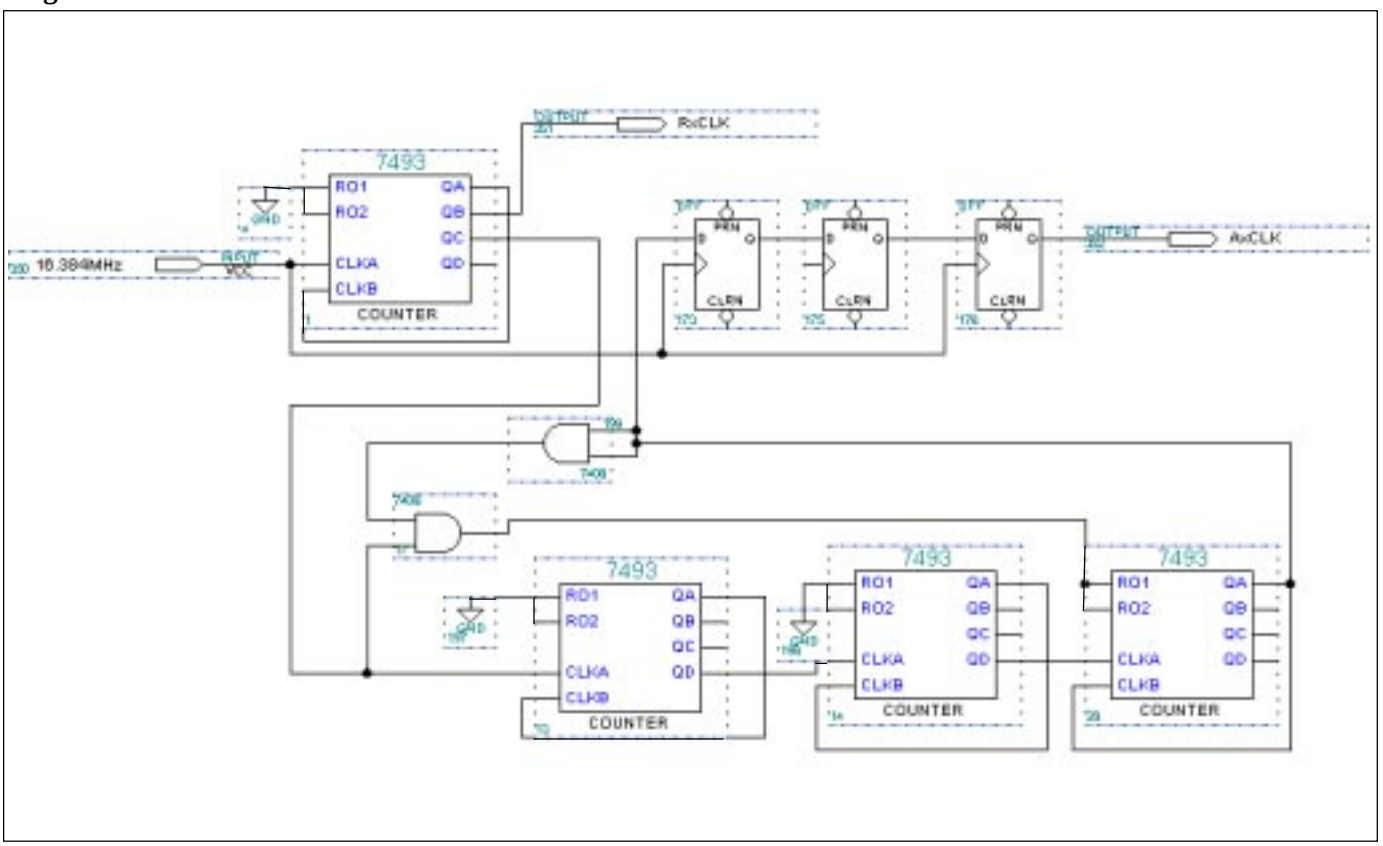


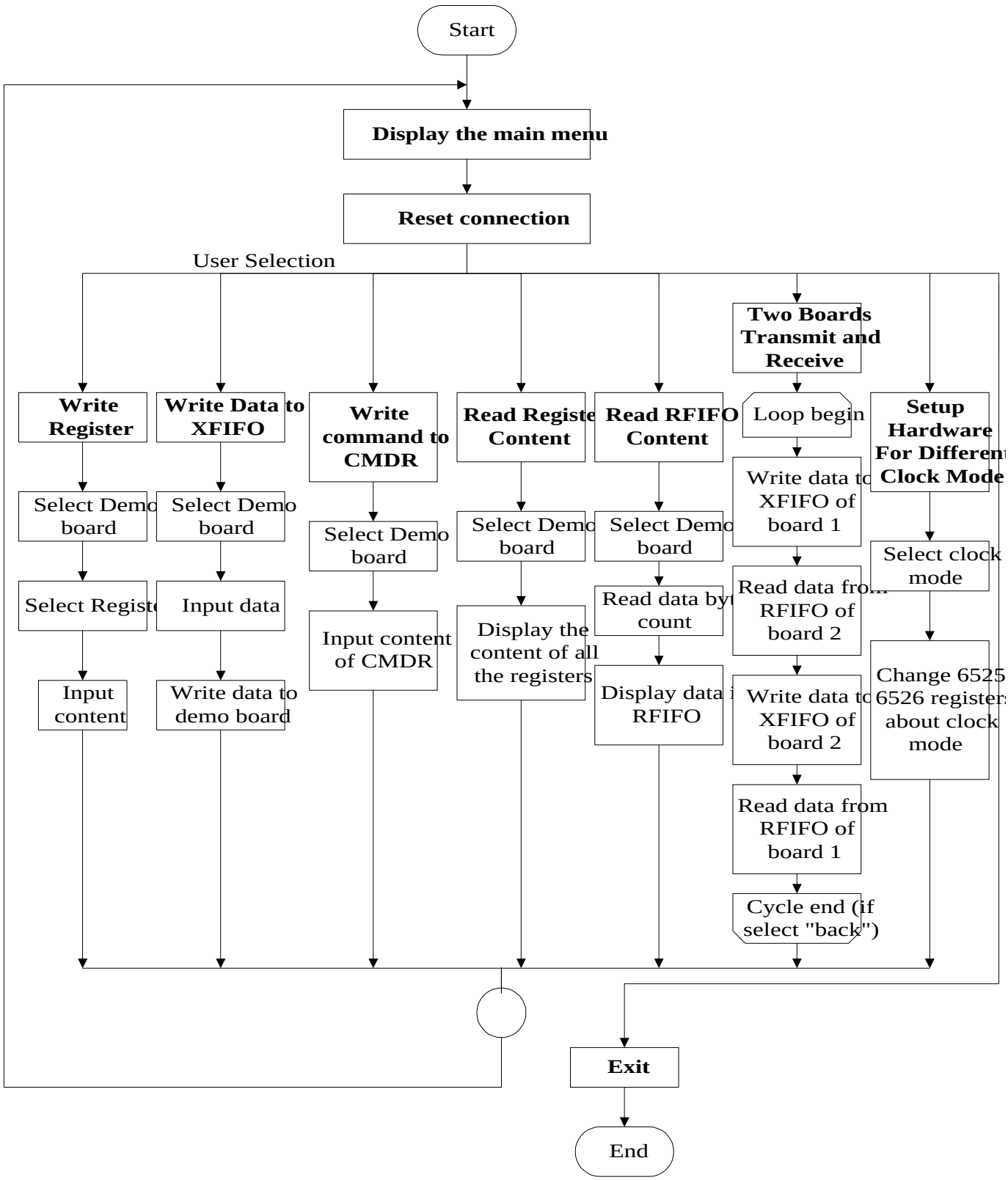
Figure 28b. Clock Source Connection for Clock Mode 3

Figure 29 shows clock source connection for Clock Mode 5.

Figure 29. Clock Source Connection for Clock Mode 5.



Appendix B: Demo Program Flow Diagram on PC



Notes

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