R2A20112ASP

Critical Conduction Mode Interleaved PFC Control IC

R03DS0047EJ0100
Rev.1.00
Jul 21, 2011

Description

The R2A20112A controls a boost converter to provide an active power factor correction.

The R2A20112A adopts critical conduction mode for power factor correction and realizes high efficiency and a low switching noise by zero current switching.

Interleaving function improves ripple current on input or output capacitor by 180 degrees phase shift.

Soft-star, the feedback loop short detection, two mode over-voltage-protection, over-current-protection, Over current ON/OFF timer protection for boost Diode short and slave ZCD open detection are built in the R2A20112A, and can constitute a power supply system of high reliability with few external parts.

Features

- Absolute Maximum Ratings
  — Supply voltage Vcc: 24 V
  — Operating junction temperature Tjopr: –40 to +150°C

- Electrical Characteristics
  — VREF output voltage Vref: 5.0 V ± 1.5%
  — UVLO operation start voltage Vuvlh: 10.5 V ± 0.7 V
  — UVLO operation shutdown voltage Vuvll: 9.3 V ± 0.5 V
  — UVLO hysteresis voltage Hysuvl: 1.2 V ± 0.5 V

- Functions
  — Boost converter control with critical conduction mode
  — Interleaving control
  — Soft start function for the reference voltage of Error Amp
  — Two mode PFC output Over-voltage-protection
    Mode1: Dynamic OVP corresponding to a voltage rise by dynamic load change.
    Mode2: Static OVP corresponding to over-voltage in stable.
  — PFC output Dynamic-under-voltage-protection (DUVP)
  — Feedback loop open/short detection
  — Master and Slave independence over-current-protection
  — 280 μs restart timer
  — Slave ZCD signal open detection
  — Over current ON/OFF timer protection for boost Diode short

- Package
  — Pb-free SOP-16

Ordering Information

Part No.	Package Name	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
R2A20112ASPW0	FP-16DAV	PRSP0016DH-B	SP	W (2,000 pcs/reel)

Pin Arrangement

(Top view)
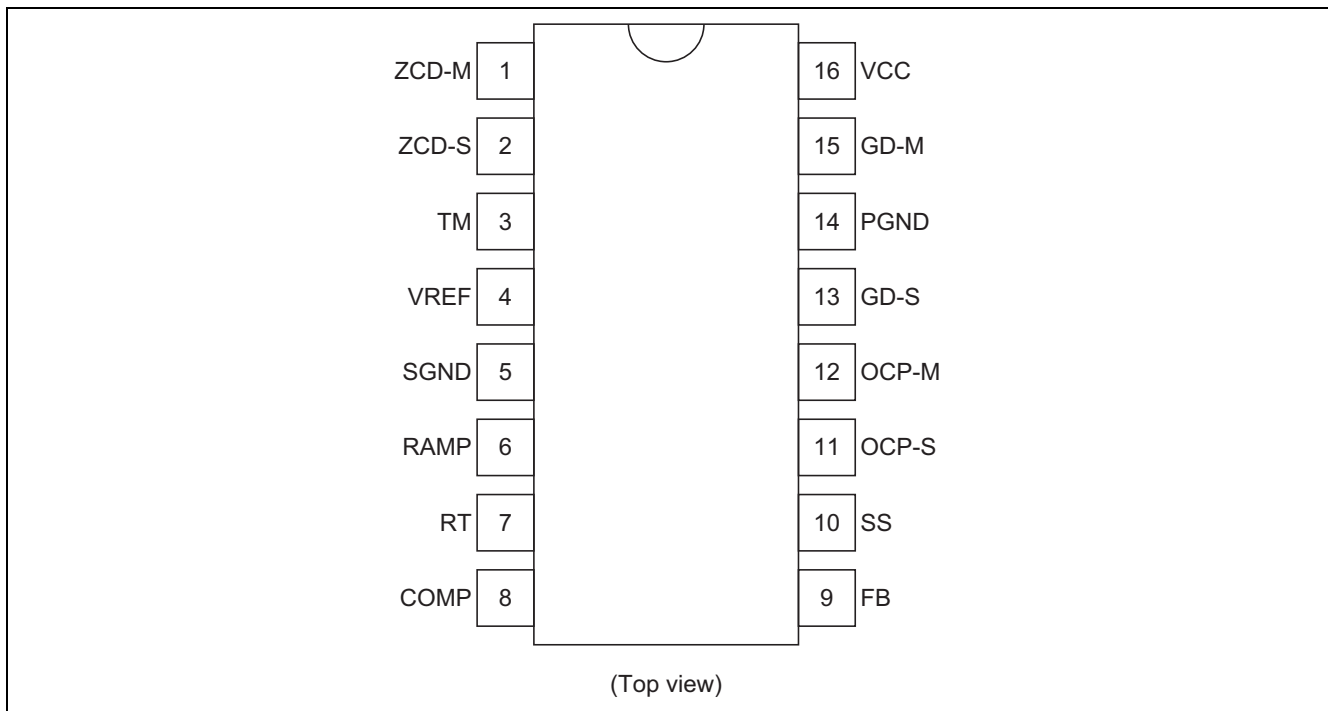
Pin Functions

Pin No.	Pin Name	Function
1	ZCD-M	Master converter zero current detection input terminal
2	ZCD-S	Slave converter zero current detection input terminal
3	TM	Over current ON/OFF timer protection terminal
4	VREF	Reference voltage output terminal
5	SGND	Signal Ground
6	RAMP	Ramp waveform setting terminal
7	RT	Oscillator frequency setting terminal
8	COMP	Error amplifier output terminal
9	FB	Error amplifier input terminal
10	SS	Soft start time setting terminal
11	OCP-S	Slave converter overcurrent detection terminal
12	OCP-M	Master converter overcurrent detection terminal
13	GD-S	Slave converter Power MOSFET drive terminal
14	PGND	Power Ground
15	GD-M	Master converter Power MOSFET drive terminal
16	VCC	Supply voltage terminal

Block Diagram

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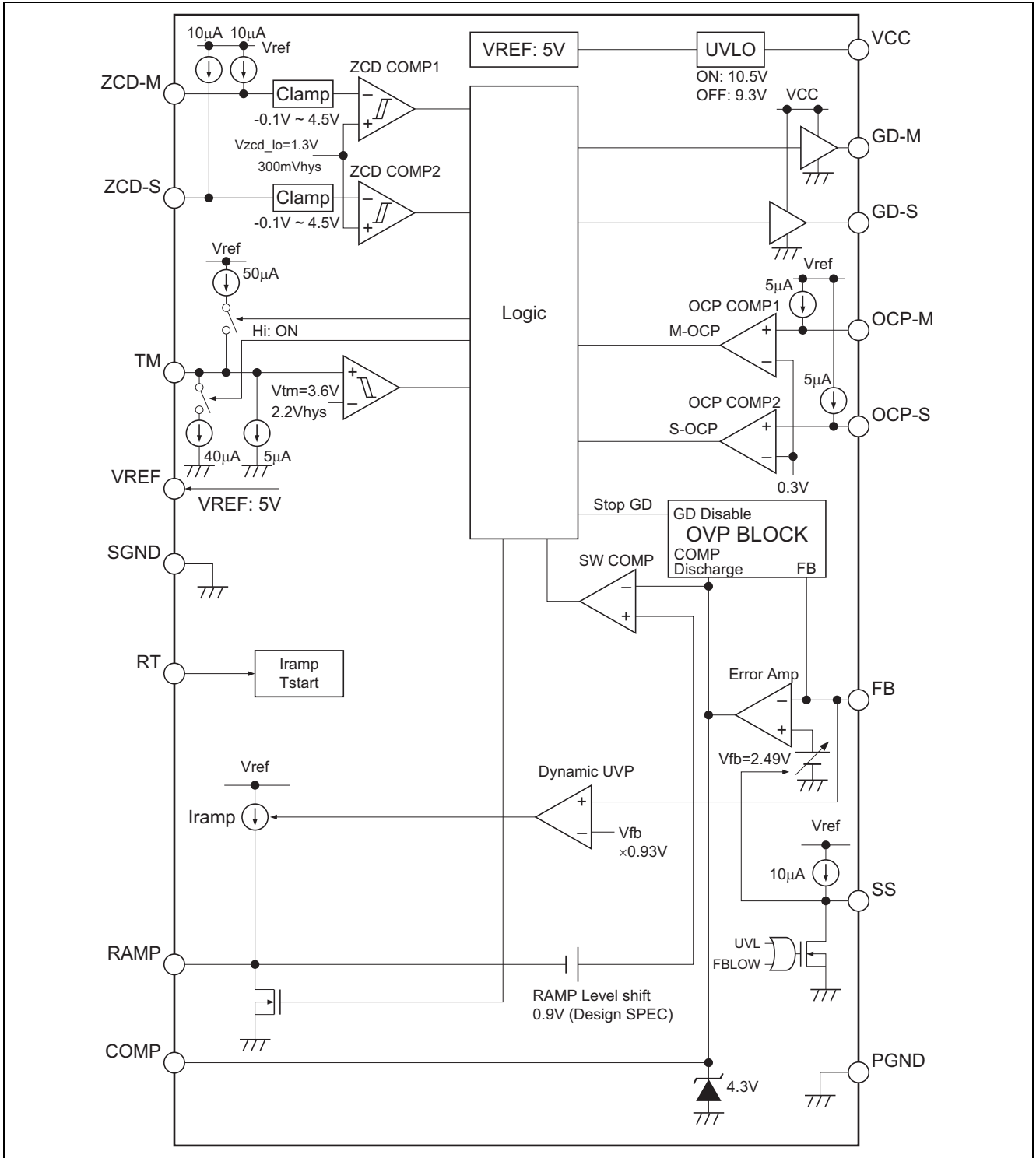
Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit	Notes
Supply voltage	VCC	−0.3 to +24	V	
GD terminal peak current	Ipk-gd	−300 +1200	mA	3
GD terminal DC current	Idc-gd	−15 +60	mA	
ZCD terminal current	Izcd	+3 −3	mA	
RT terminal current	Irt	−200	µA	4
Vref terminal current	Iref	−5	mA	
Vref terminal load capacitor	Cref min	1000	pF	
	Cref max	1	µF	
COMP terminal current	Icomp	±1	mA	
Terminal voltage	Vt-group1	−0.3 to Vcc	V	5
	Vt-group2	−0.3 to Vref	V	6
Vref terminal voltage	Vt-ref	−0.3 to Vref + 0.3	V	
OCP terminal voltage	Vt-ocp	*−1 to Vref	V	7
Power dissipation	Pt	1	W	8
Operating junction temperature	Tj-opr	−40 to +150	°C	
Storage temperature	Tstg	−55 to +150	°C	

Notes: 1. Rated voltages are with reference to the PGND terminal.

2. For rated currents, inflow to the IC is indicated by (+), and outflow by (−).

3. Shows the transient current when driving a capacitive load.

4. RT terminal's resistor is fixed 33 kΩ to GND.

5. This is the rated voltage for the following pins:
Nothing

6. This is the rated voltage for the following pins:
FB, SS, RAMP, TM

7. Minus value is peak voltage. Do not impress the DC voltage of the minus.

8. θja = 120°C/W
This value is a thing mounting on 40×40 (thickness: 1.6 mm) [mm^2],
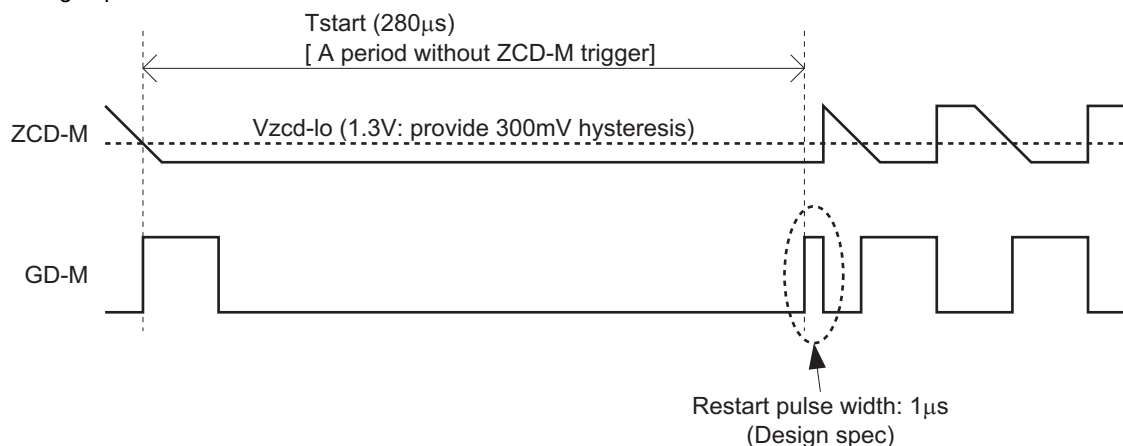a glass epoxy board of wiring density 10%.

Electrical Characteristics

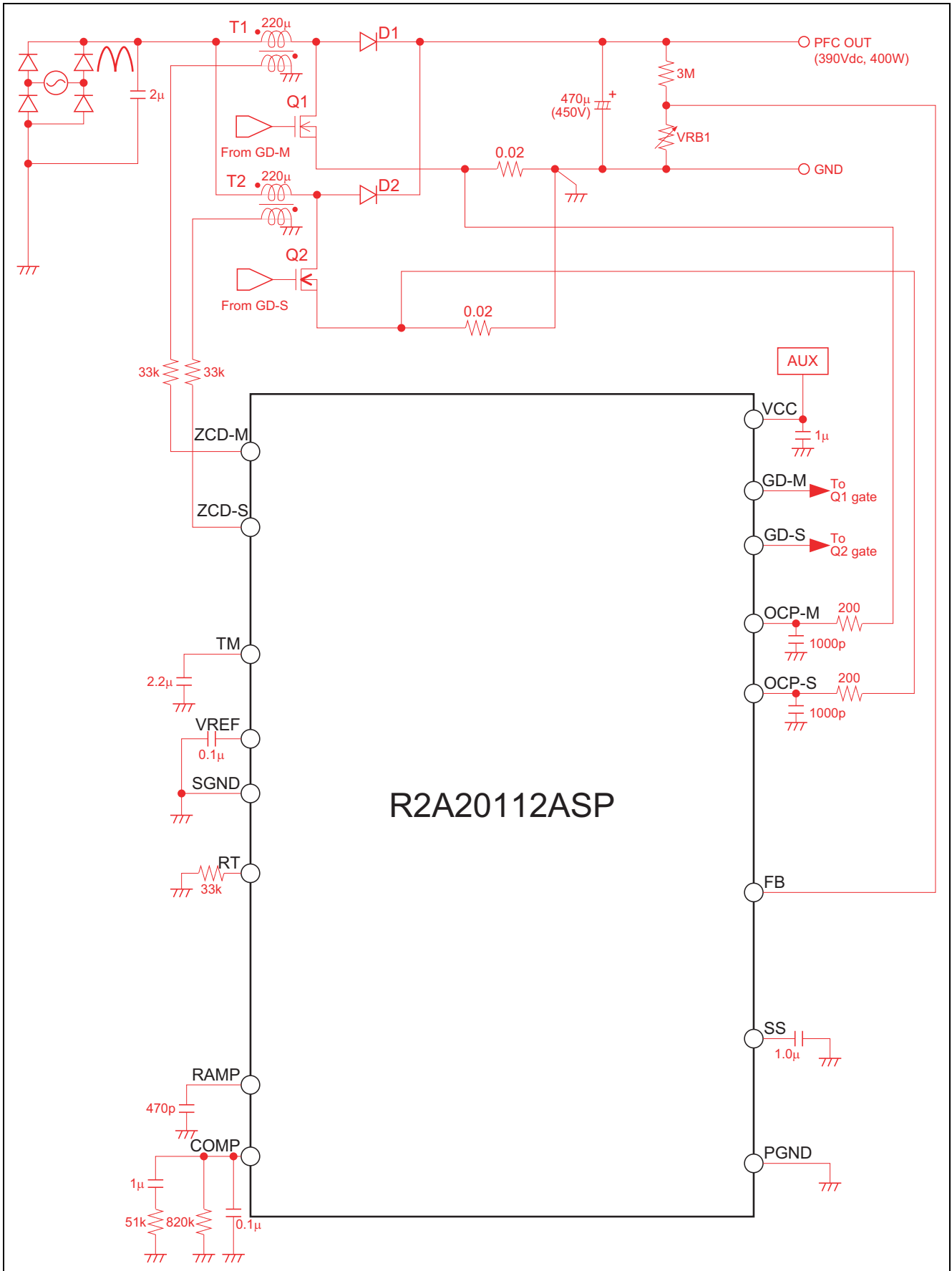(Ta = 25°C, VCC = 12 V, RT = 33 kΩ, RAMP = 820 pF, TM = 2.2 μF, SS = 1.0 μF, OCP = GND)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Supply	UVLO turn-on threshold	Vuvlh	9.8	10.5	11.2	V	
	UVLO turn-off threshold	Vuvll	8.8	9.3	9.8	V	
	UVLO hysteresis	Hysuvl	0.7	1.2	1.7	V	
	Standby current	Istby	—	85	170	μA	VCC = 8.9 V
	Operating current	Icc	—	4.2	6.3	mA	
VREF	Output voltage	Vref	4.925	5.00	5.075	V	Isource = −1 mA
	Line regulation	Vref-line	—	5	20	mV	Isource = −1 mA Vcc = 10 V to 24 V
	Load regulation	Vref-load	—	5	20	mV	Isource = −1 mA to −5 mA
	Temperature stability	dVref	—	±80	—	ppm/°C	Ta = −40 to +125°C [1]
Error amplifier	Feedback voltage	Vfb	2.452	2.490	2.528	V	FB-COMP short
	Input bias current	Ifb	−0.5	−0.3	−0.1	μA	Measured pin: FB FB = 3 V [1]
	Open loop gain	Av	—	60	—	dB	[1]
	Upper clamp voltage	Vclamp-comp	4.2	4.3	4.4	V	FB = 2.0 V
	Low voltage	Vl-comp	—	0.1	0.3	V	FB = 3.0 V
	Source current	Isrc-comp	—	−120	—	μA	FB = 1.5 V COMP = 2.5 V [1]
	Sink current	Isnk-comp	—	330	—	μA	FB = 3.5 V COMP = 2.5 V
	Transconductance	gm	120	200	290	μs	FB = 2.45V ↔ 2.55 V COMP = 2.5 V
Ramp	RAMP charge current at DUVP disable condition	Ic-ramp1	−60	−50	−40	μA	FB = 2.4 V
	RAMP charge current at DUVP enable condition	Ic-ramp2	−32	−25	−18	μA	FB = 2 V
	RAMP discharge current	Id-ramp	7	15	29	mA	RAMP = 1 V
	Low voltage	Vl-ramp	—	17	200	mV	Isink = 100 μA
Slave control	Phase delay	Phase	160	180	200	deg	FB = 2.5 V, COMP = 2 V [1, 2]
	On time ratio	Ton-ratio	0	—	5	%	

Notes: *1 Design spec
*2
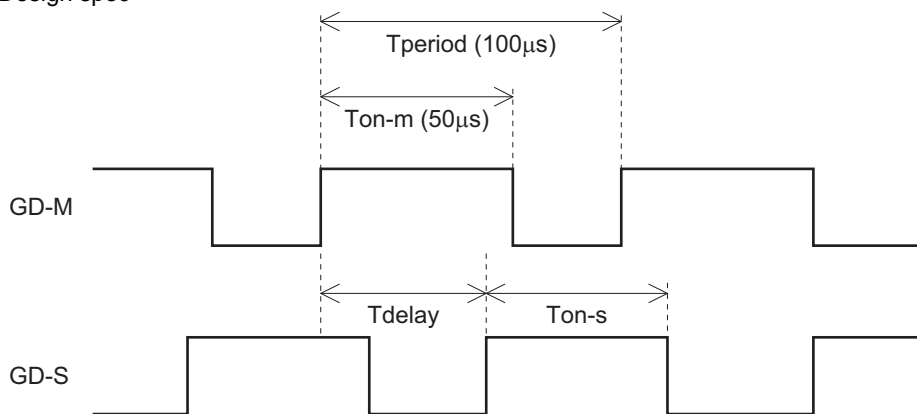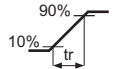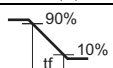
$$\text{Phase} = \frac{\text{Tdelay}}{\text{Tperiod}} \times 360 \ [\text{deg}]$$

$$\text{Ton-ratio} = \left(1 - \frac{\text{Ton-s}}{\text{Ton-m}}\right) \times 100 \ [\%]$$

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Electrical Characteristics (cont.)

(Ta = 25°C, VCC = 12 V, RT = 33 kΩ, RAMP = 820 pF, TM = 2.2 μF, SS = 1.0 μF, OCP = GND)

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Gate drive (GD-M & GD-S)	Gate drive rise time	tr-gd	—	20	100	ns	FB-COMP short CL = 100 pF
	Gate drive fall time	tf-gd	—	5	30	ns	FB-COMP short CL = 100 pF
	Gate drive low voltage	Vol1-gd	—	0.02	0.1	V	Isink = 2 mA
		Vol2-gd	—	0.01	0.2	V	Isink = 1 mA, VCC = 5 V
	Gate drive high voltage	Voh-gd	11.5	11.9	—	V	Isource = −2 mA *1
Over current protection (OCP-M & OCP-S)	OCP threshold voltage	Vocp	0.27	0.30	0.33	V	
	OCP source current	Iocp	−10	−5	−2.5	μA	OCP = 0 V
ON/OFF timer protection for Boost diode short	ON/OFF timer threshold voltage	Vtm	3.52	3.6	3.68	V	
	ON/OFF timer hysteresis	Hys-tm	2.1	2.2	2.3	V	
	Charge current	Isrc-tm	−54	−45	−36	μA	TM = 2 V, OCP-M = 1 V
	Discharge current at TM disable condition	Isnk-tm1	36	45	54	μA	TM = 2 V
	Discharge current at TM enable condition	Isnk-tm2	4.2	5	5.8	μA	TM = 5 V to 2 V
PFC output abnormality protection	Dynamic OVP threshold voltage	Vdovp	Vfb× 1.035	Vfb× 1.050	Vfb× 1.065	V	COMP = 2.5 V
	Static OVP threshold voltage	Vsovp	Vfb× 1.075	Vfb× 1.090	Vfb× 1.105	V	COMP = 2.5 V
	Static OVP hysteresis	Hys-sovp	50	100	150	mV	COMP = 2.5 V
	Dynamic UVP threshold voltage	Vduvp	—	Vfb× 0.930	Vfb× 0.950	V	COMP = 2.5 V *1
	FB low detect threshold voltage	Vfblow	0.45	0.50	0.55	V	COMP = 2.5 V
	FB low detect hysteresis	Hysfblow	0.16	0.20	0.24	V	COMP = 2.5 V
Zero current detector (ZCD-M & ZCD-S)	Upper clamp voltage	Vzcdh	4.0	4.5	5.0	V	Isource = −3 mA
	Lower clamp voltage	Vzcdl	−0.5	−0.1	0.4	V	Isink = 3 mA
	ZCD low threshold voltage	Vzcd-lo	0.9	1.3	1.6	V	*1
	ZCD hysteresis	Hyszcd	130	300	410	mV	*1
	Input bias current	Izcd	−14	−10	−6	μA	1.2 V < Vzcd < 2.5 V
ZCD-S open detector	Slave ZCD open detect delay time	tzcds	—	100	—	ms	ZCD-S: OPEN Gate drive 10 kHz *1
Soft start	Charge current	Ic-ss	−14	−10	−6	μA	SS = 3 V, FB = 1 V
Restart	Restart time delay	Tstart	210	280	350	μs	ZCD-M = 10 kΩ to GND ZCD-S = 10 kΩ to GND *2

Notes: *1 Design spec
       *2

Tstart (280μs)
[A period without ZCD-M trigger]

ZCD-M   Vzcd-lo (1.3V: provide 300mV hysteresis)

GD-M

Restart pulse width: 1μs
(Design spec)

System Diagram

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g

NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.
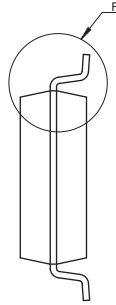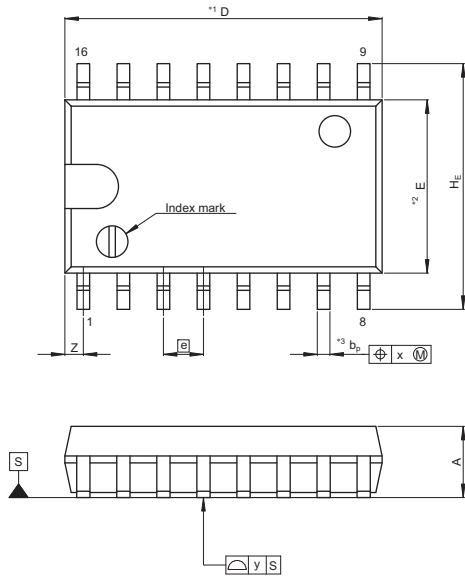
Terminal cross section
(Ni/Pd/Au plating)

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L_1	——	1.15	——

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Notice

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Renesas Electronics Corporation

http://www.renesas.com

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141