

Product Overview

Address Spaces

Addressing Modes

Control Registers

Interrupt Structure

Instruction Set

1 PRODUCT OVERVIEW

SAM8 PRODUCT FAMILY

Samsung's SAM8 family of 8-bit single-chip CMOS microcontrollers offers a fast and efficient CPU with a wide range of integrated peripherals, in various mask-programmable ROM sizes. Analog its major CPU features are:

- Efficient register-oriented architecture
- Selectable CPU clock sources
- Idle and Stop power-down mode release by interrupt
- Built-in basic timer with watchdog function

The sophisticated interrupt structure recognizes up to eight interrupt levels. Each level can have one or more interrupt sources and vectors. Fast interrupt processing (within a minimum of six CPU clocks) can be assigned to specific interrupt levels.

S3C8625/C8627/C8629/P8629 MICROCONTROLLERS

S3C8625/C8627/C8629/P8629 single-chip 8-bit microcontrollers are based on the powerful SAM8 CPU architecture. The internal register file is logically expanded to increase the on-chip register space. S3C8625/C8627/C8629/P8629 contain 16/32 K bytes of on-chip program ROM.

In line with Samsung's modular design approach, the following peripherals are integrated with the SAM8 core:

- Four programmable I/O ports (total 27 pins)
- One 8-bit basic timer for oscillation stabilization and watchdog functions
- One 8-bit general-purpose timer/counter with selectable clock sources
- One 12-bit counter with selectable clock sources, including Hsync or Csync input
- One interval timer
- PWM block with seven 8-bit PWM circuits
- Sync processor block (for Vsync and Hsync I/O, Csync input, and Clamp signal output)
- DDC and normal Multi-master IIC-bus
- 4-channel A/D converter (8-bit resolution)

S3C8625/C8627/C8629/P8629 are a versatile microcontrollers which are ideal for use in multi-sync monitors or in general-purpose applications that require sophisticated timer/counter, PWM, sync signal processing, A/D converter, and multi-master IIC-bus support with DDC. They are available in a 42-pin SDIP or a 44-pin QFP package.

OTP

S3C8625/C8627/C8629 microcontrollers are also available in OTP (One Time Programmable) version named, S3P8629. S3P8629 microcontroller has an on-chip 32-Kbyte one-time-programmable EPROM instead of masked ROM. S3P8629 is comparable to S3C8625/C8627/C8629, both in function and pin configuration except its ROM size.

FEATURES

CPU

- SAM8 CPU core

Memory

- 16/24/32-Kbyte internal program memory (ROM)
- 464-byte general-purpose register area

Instruction Set

- 78 instructions
- IDLE and STOP instructions added for power-down modes

Instruction Execution Time

- Minimum 500 ns (with 12 MHz CPU clock)

Interrupts

- Ten interrupt sources
- Ten interrupt vectors
- Seven interrupt level
- Fast interrupt feature

General I/O

Four I/O Ports (total 27pins)

8-Bit Basic Timer

Programmable timer for oscillation stabilization interval control or watchdog timer function

Three selective internal clock frequencies

Timer/Counters

One 8-bit Timer/Counter with several clock sources (Capture mode)

One 12-bit Counter with H-sync and several clock sources

One Interval Timer

Pulse Width Modulator (PWM)

8-bit PWM: 7-CH

Sync-Processor Block

Vsync-I, Hsync-I, Csync-I input and Vsync-O, Hsync-O, Clamp-O output pins

Pseudo sync signal output

Auto SOG detection

Auto Hsync polarity detection

DDC Multi-Master IIC-Bus 1-Ch

Serial Peripheral Interface

Support for Display Data Channel (DDC1/DDC2B/DDC2Bi/DDC2B+)

Normal Multi-Master IIC-Bus 1-Ch

Serial Peripheral Interface

A/D Converter

4-channel; 8-bit resolution

Oscillator Frequency

8 MHz to 12 MHz crystal operation

Internal Max. 12 MHz CPU clock

Operating Temperature Range

– 40 °C to + 85 °C

Operating Voltage Range

4.0 V to 5.5 V

Package Types

42-pin SDIP, 44-pin QFP

BLOCK DIAGRAM

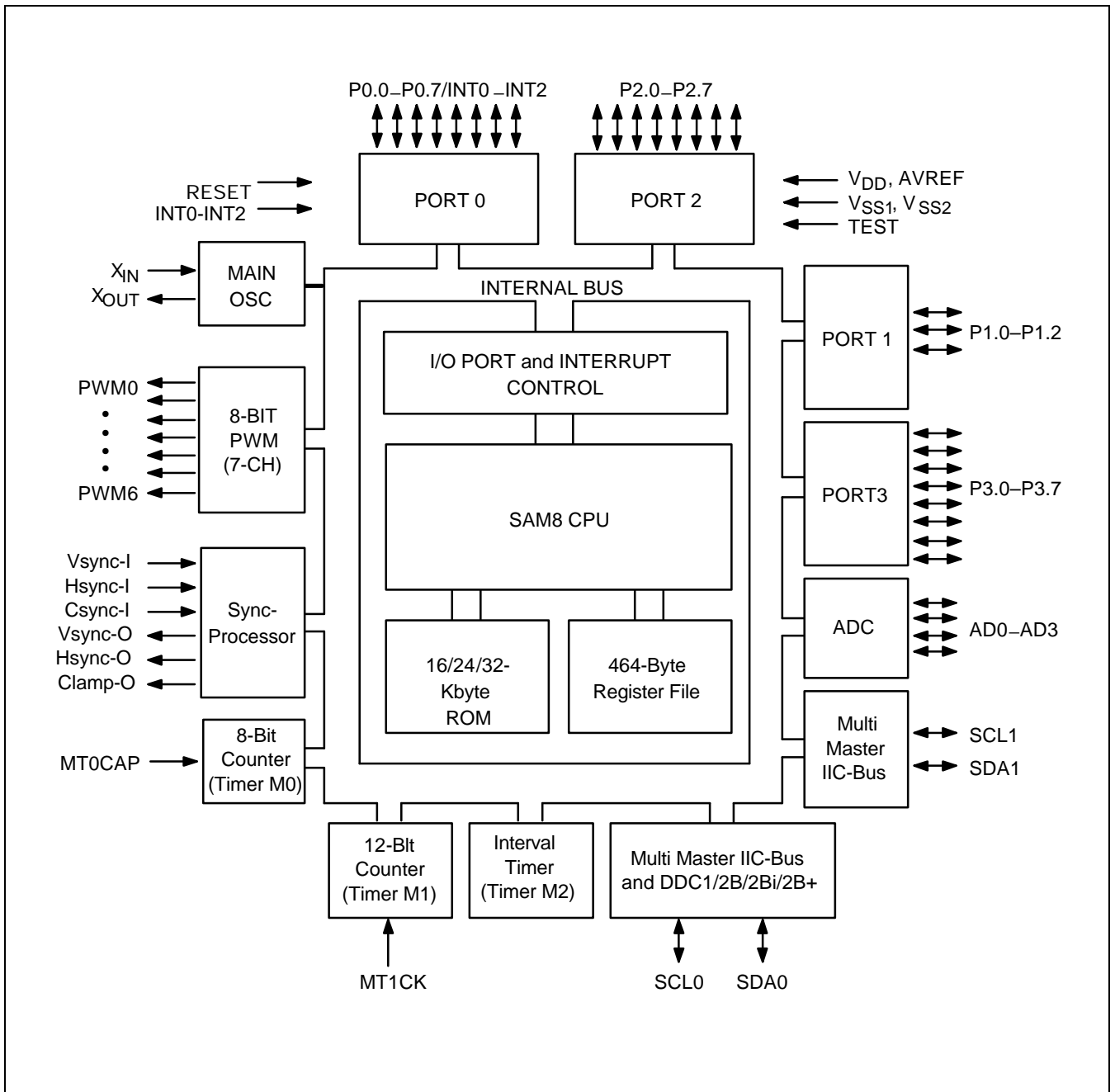


Figure 1-1. Block Diagram

PIN ASSIGNMENTS

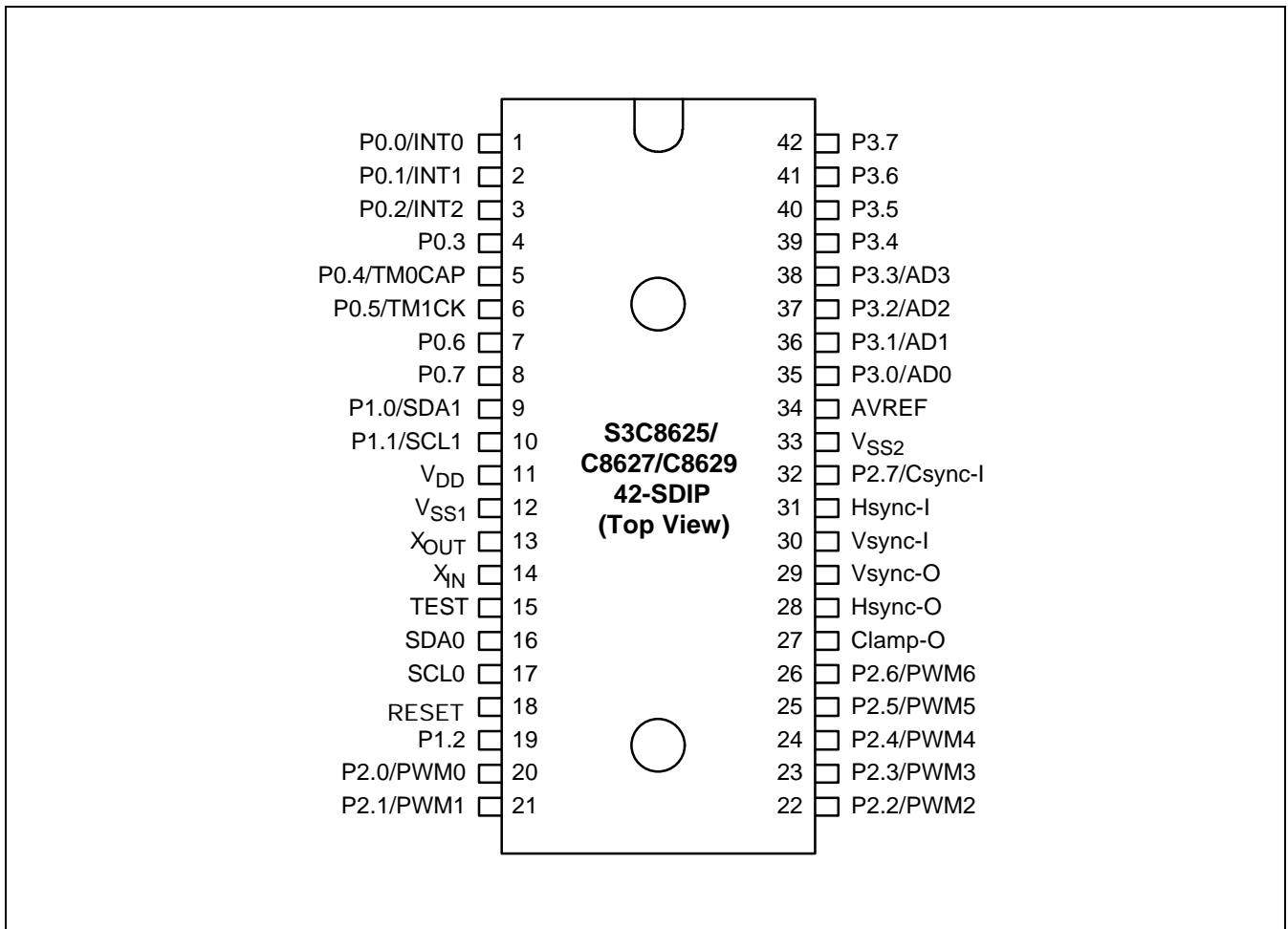


Figure 1-2. S3C8625/C8627/C8629 42-SDIP Pin Assignment

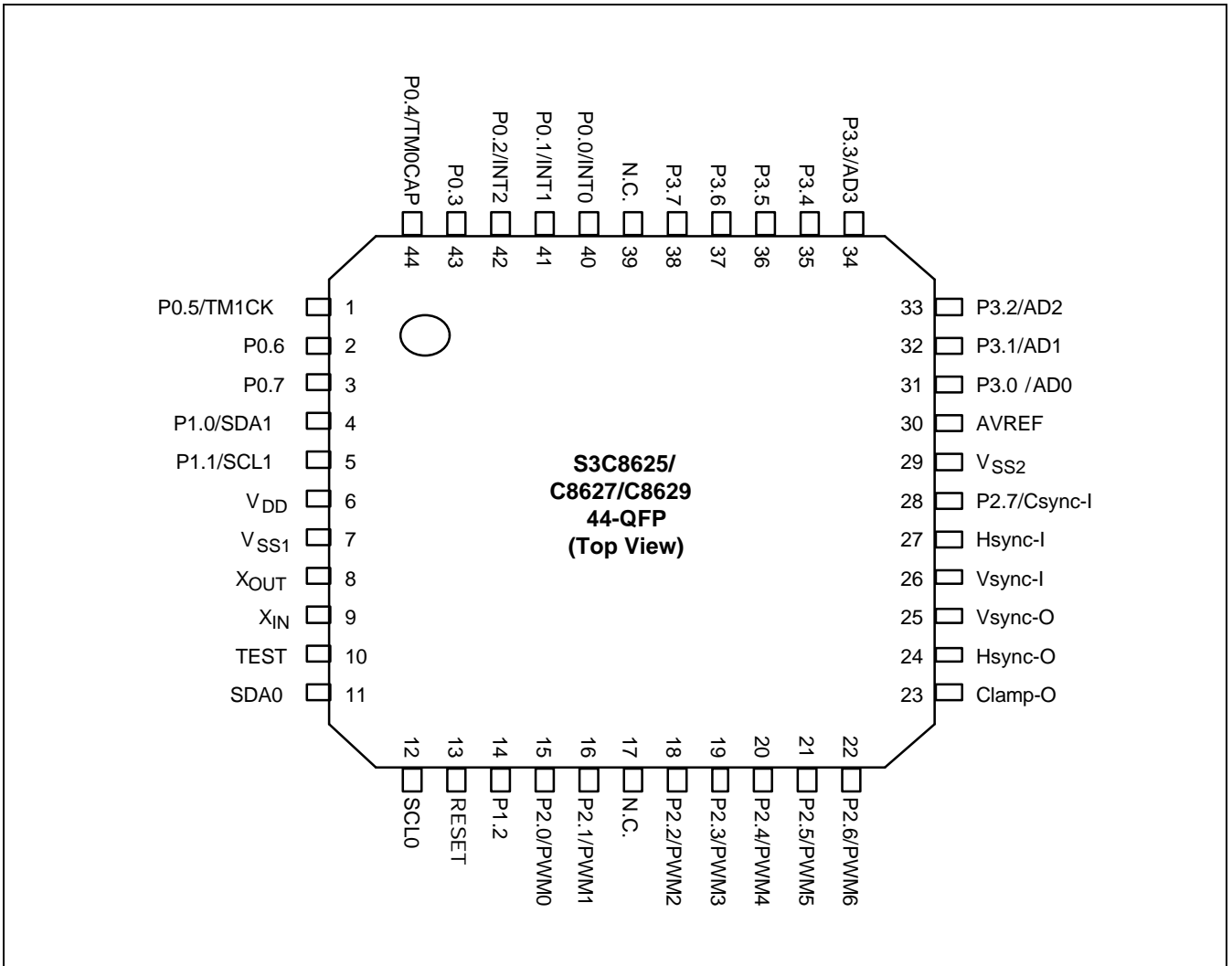


Figure 1-3. S3C8627/C8629 44-QFP Pin Assignment

PIN DESCRIPTIONS

Table 1-1. S3C8625/C8627/C8629/P8629 Pin Descriptions

Pin Names	Pin Type	Pin Description	Circuit Type	SDIP Pin Numbers	Shared Functions
P0.0 P0.1 P0.2 P0.3 P0.4 P0.5 P0.6 P0.7	I/O	General-purpose, 8-bit I/O port. Shared functions include three external interrupt inputs and I/O for timer M0 and M1. Selective configuration of port 0 pins to input or output mode is supported.	D-1 D-1 D-1 D-1 D-1 D-1 D-1 D-1	1 2 3 4 5 6 7 8	INT0 INT1 INT2 TM0CAP TM1CK
P1.0 P1.1 P1.2	I/O	General-purpose, 3-bit I/O port. Selective configuration is available for port 1 pins to input, push-pull output, n-channel open-drain mode, or IIC-bus clock and data I/O.	E-1 E-1 E-1	9 10 19	SDA1 SCL1
P2.0 P2.1 P2.2 P2.3 P2.4 P2.5 P2.6 P2.7	I/O	General-purpose, 8-bit I/O port Selective configuration of port 2 pins to input or output mode is supported. The port 2 pin circuits are designed to push-pull PWM output and Csync signal input.	D-1 D-1 D-1 D-1 E-1 E-1 E-1 D-1	20 21 22 23 24 25 26 32	PWM0 PWM1 PWM2 PWM3 PWM4 PWM5 PWM6 Csync-I
P3.0–P3.3 P3.4–P3.7	I/O	General-purpose, 8-bit I/O port Selective configuration port 3 pins to input or output mode is supported. Multiplexed for alternative use as A/D converter inputs AD0–AD3.	D-1 E	35–38, 39–42	AD0–AD3
Hsync-I Vsync-I Clamp-O Hsync-O Vsync-O SDA0 SCL0	I I O O O I/O I/O	The pins are sync processor signal I/O, IIC-bus clock, and data I/O.	A A A A A G-3 G-3	31 30 27 28 29 16 17	–
V _{DD} , V _{SS1} , AVREF, V _{SS2}	–	Power pins ADC power pins	– –	11, 12 34, 33	–
X _{IN} , X _{OUT}	–	System clock I/O pins	–	14, 13	–
RESET	I	System reset pin	B	18	–
TEST	I	Factory test pin input 0V:Normal operation,5V:Factory test mode	–	15	–

PIN CIRCUITS

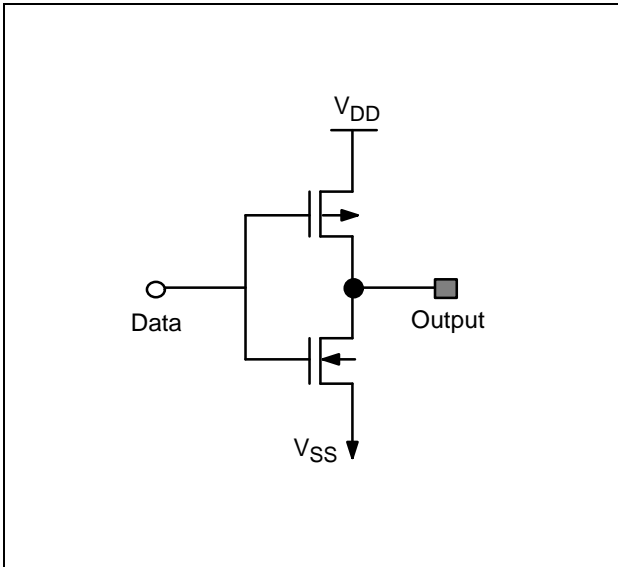


Figure 1-4. Pin Circuit Type A

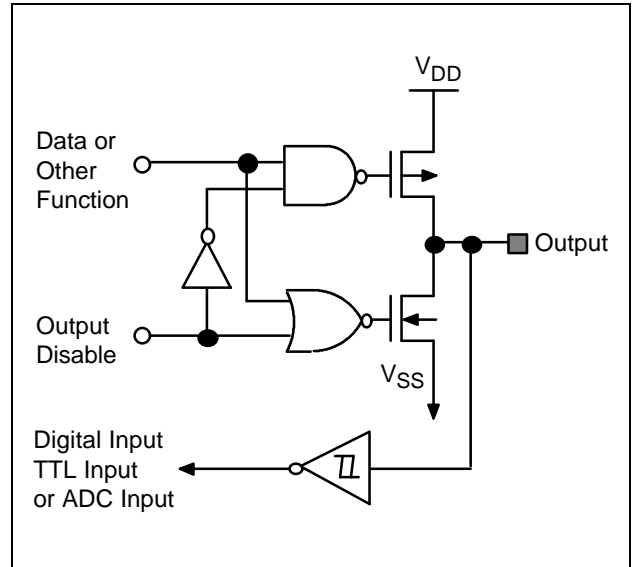


Figure 1-6. Pin Circuit Type D-1

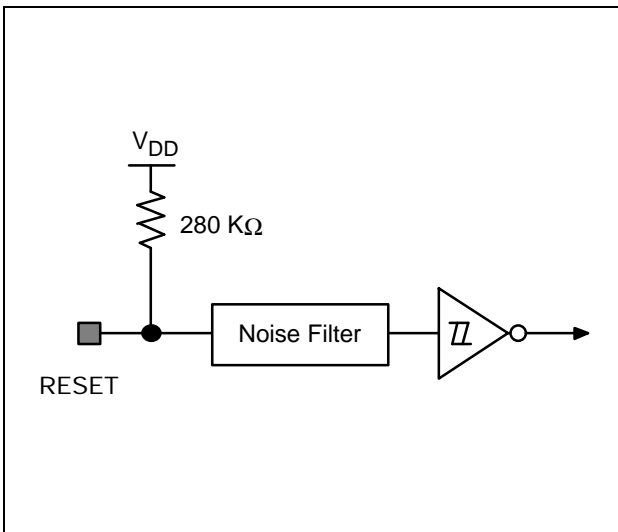


Figure 1-5. Pin Circuit Type B (RESET)

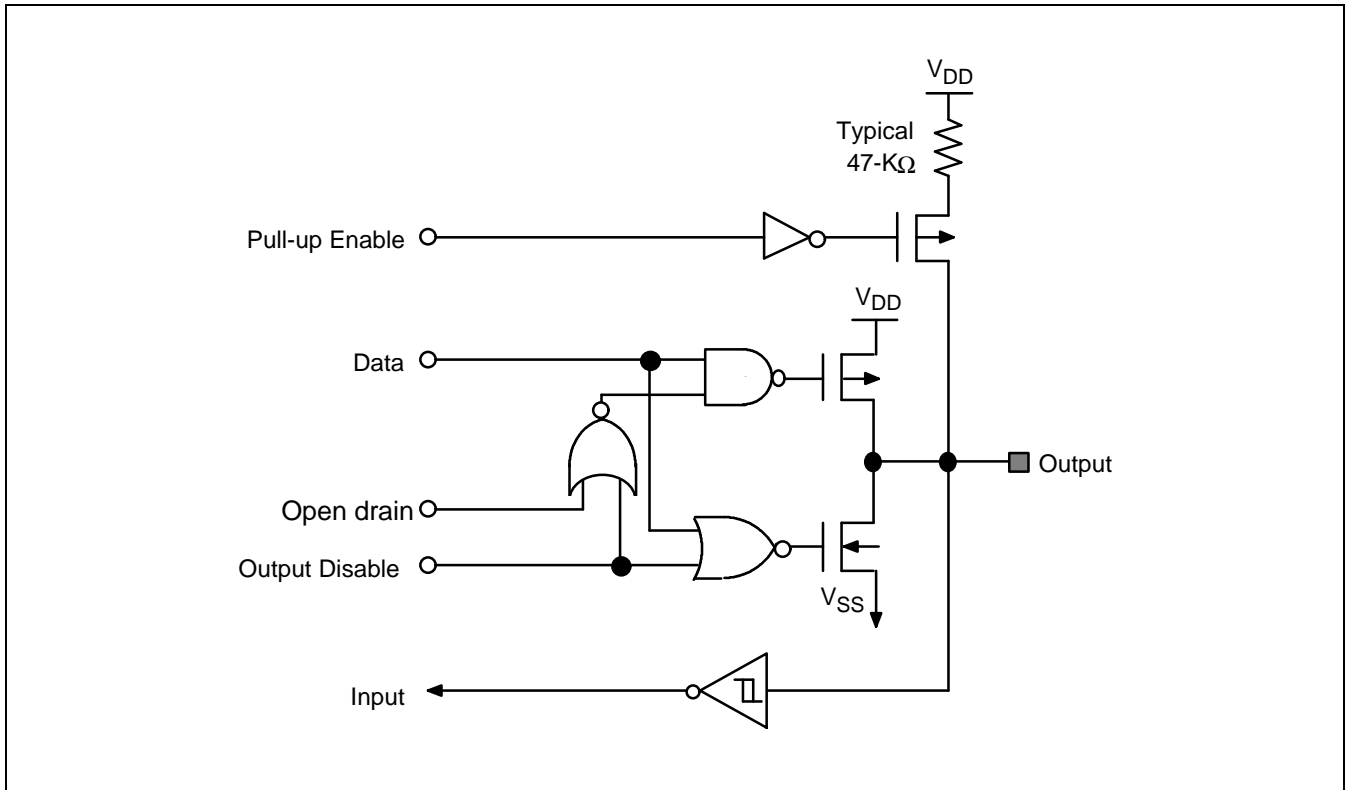


Figure 1-7. Pin Circuit Type E

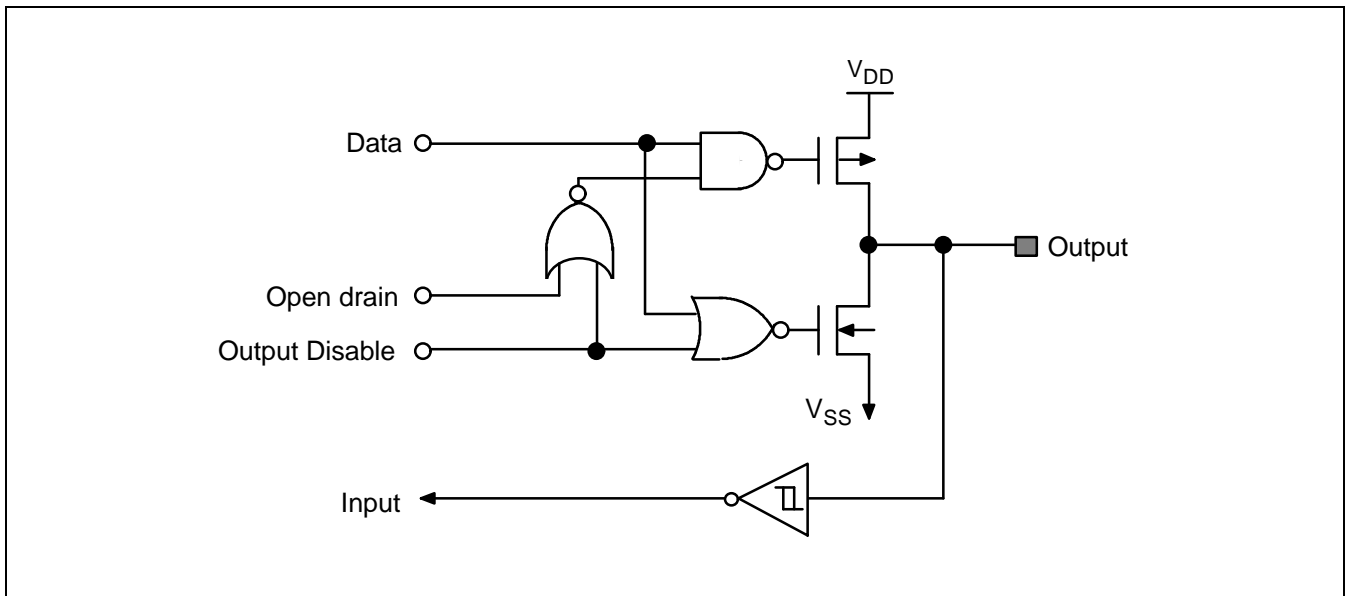


Figure 1-8. Pin Circuit Type E-1

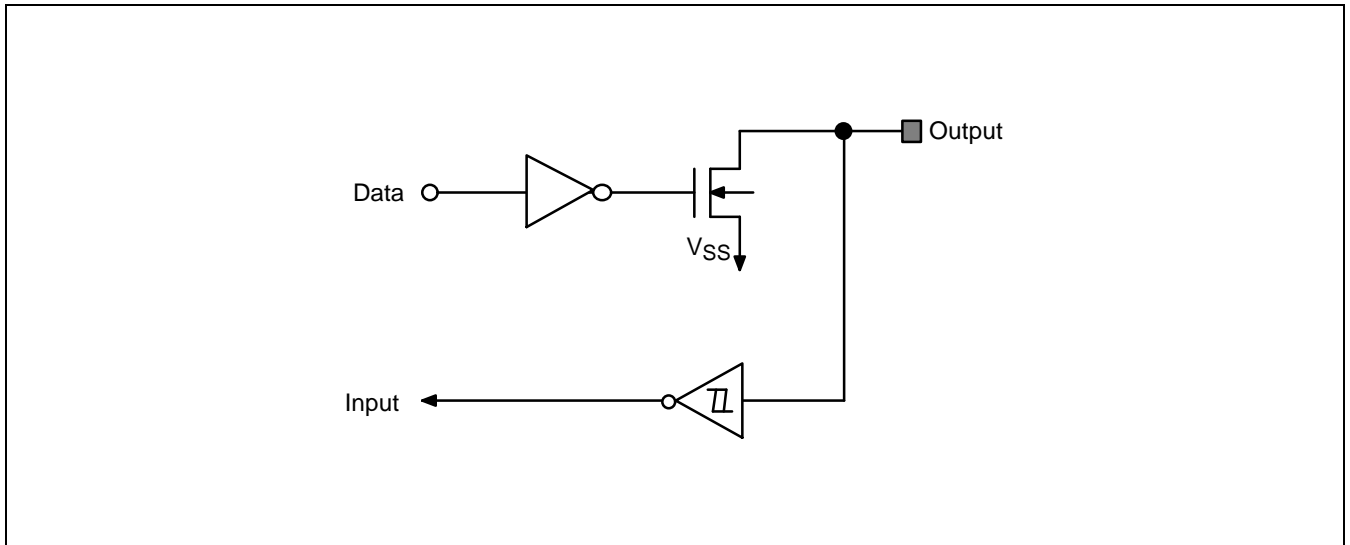


Figure 1-9. Pin Circuit Type G-3

19 ELECTRICAL DATA

OVERVIEW

In this section, S3C8625/C8627/C8629 electrical characteristics are presented in tables and graphs. The information is arranged in the following order:

- Absolute maximum ratings
- D.C. electrical characteristics
- Data retention supply voltage in stop mode
- Stop mode release timing when initiated by a reset
- I/O capacitance
- A/D Converter electrical characteristics
- A.C. electrical characteristics
- Input timing measurement points for P0.0–P0.2, TM0CAP, and TM1CK
- Oscillation characteristics
- Oscillation stabilization time
- Clock timing measurement points for X_{IN}
- Schmitt trigger characteristics

Table 19-1. Absolute Maximum Ratings

 $(T_A = 25^\circ\text{C})$

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input voltage	V_{I1}	Type C (n-channel, open-drain)	– 0.3 to + 7.0	V
	V_{I2}	All port pins except V_{I1}	– 0.3 to $V_{DD} + 0.3$	
Output voltage	V_O	All output pins	– 0.3 to $V_{DD} + 0.3$	V
Output current High	I_{OH}	One I/O pin active	– 10	mA
		All I/O pins active	– 60	
Output current Low	I_{OL}	One I/O pin active	+ 30	mA
		Total pin current except port 3	+ 100	
		Sync-processor I/O pins and IIC-bus clock and data pins	+ 150	
Operating temperature	T_A	–	– 40 to + 85	$^\circ\text{C}$
Storage temperature	T_{STG}	–	– 65 to + 150	$^\circ\text{C}$

Table 19-2. D.C. Electrical Characteristics

 $(T_A = -40^\circ\text{C to } +85^\circ\text{C}, V_{DD} = 4.0\text{ V to } 5.5\text{ V})$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High voltage	V_{IH1}	All input pins except V_{IH2} and V_{IH3}	$0.8 V_{DD}$	–	V_{DD}	V
	V_{IH2}	X_{IN}	2.7		V_{DD}	
	V_{IH3}	TTL input (Hsyncl, Vsyncl, and Csyncl)	2.0		V_{DD}	
Input Low voltage	V_{IL1}	All input pins except V_{IL2} and V_{IL3}	–	–	$0.2 V_{DD}$	V
	V_{IL2}	X_{IN}			1.0	
	V_{IL3}	TTL input (Hsyncl, Vsyncl, and Csyncl)			0.8	
Output High voltage	V_{OH1}	$I_{OH} = -8\text{ mA}$; Port 3 only	$V_{DD} - 1.0$	–	–	V
	V_{OH2}	$I_{OH} = -2\text{ mA}$ Ports 0, 2, ClampO, H, and VsyncO				
	V_{OH3}	$I_{OH} = -6\text{ mA}$; Port 1				

Table 19-2. D.C. Electrical Characteristics (Continued)

(T_A = -40 °C to +85 °C, V_{DD} = 4.0 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Low voltage	V _{OL1}	I _{OL} = 8 mA; port 3 only	–	–	0.4	V
	V _{OL2}	I _{OL} = 2 mA Port 0, 2, ClampO, H, and VsyncO			0.4	
	V _{OL3}	I _{OL} = 6 mA Port 1; SCL and SDA			0.6	
Input High leakage current	I _{LIH1}	V _{IN} = V _{DD} All input pins except X _{IN} , X _{OUT}	–	–	3	μA
	I _{LIH2}	V _{IN} = V _{DD} ; X _{OUT} only	–	–	20	
	I _{LIH3}	V _{IN} = V _{DD} ; X _{IN} only	2.5	6	20	
Input Low leakage current	I _{LIL1}	V _{IN} = 0 V; All input pins except X _{IN} , X _{OUT} , and RESET	–	–	–3	μA
	I _{LIL2}	V _{IN} = 0 V; X _{OUT} only	–	–	–20	
	I _{LIL3}	V _{IN} = 0 V; X _{IN} only	–2.5	–6	–20	
Output High leakage current	I _{LOH1}	V _{OUT} = V _{DD}	–	–	3	μA
Output Low leakage current	I _{LOL1}	V _{OUT} = 0 V	–	–	–3	μA
Pull-up resistor	R _{L1}	V _{IN} = 0 V Ports 3.7–3.4	20	47	80	kΩ
	R _{L2}	V _{IN} = 0 V RESET only	150	280	480	
Supply current (note)	I _{DD1}	Operation mode; 12 MHz crystal C1 = C2 = 22pF	–	15	30	mA
	I _{DD2}	Idle mode; 12 MHz crystal C1 = C2 = 22pF		5	10	
	I _{DD3}	Stop mode		1	10	μA

NOTE: Supply current does not include drawn internal pull-up resistors and external loads of output.

Table 19-3. Data Retention Supply Voltage in Stop Mode

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Stop mode	2	–	5.5	V
Data retention supply current	I_{DDDR}	Stop mode, $V_{DDDR} = 2.0\text{ V}$	–	–	5	μA

NOTES:

1. During the oscillator stabilization wait time (t_{WAIT}), all CPU operations must be stopped.
2. Supply current does not include drawn through internal pull-up resistors and external output current loads.

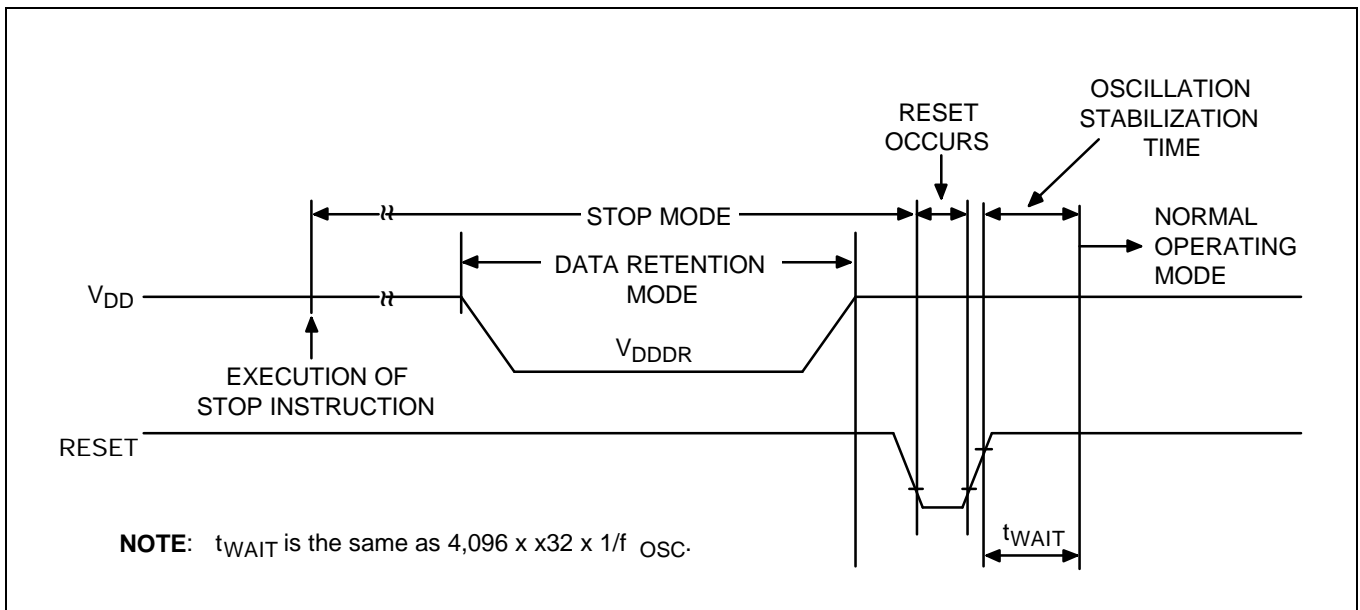


Figure 19-1. Stop Mode Release Timing When Initiated by a Reset

Table 19-4. Input/Output Capacitance

($T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, $V_{DD} = 0\text{ V}$)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input capacitance	C_{IN}	$f = 1\text{ MHz}$; unmeasured pins are connected to V_{SS}	–	–	10	pF
Output capacitance	C_{OUT}					
I/O capacitance	C_{IO}					

Table 19-5. A/D Converter Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 4.0 V to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resolution			–	8	–	bit
Total accuracy		V _{DD} = 5 V Conversion time = 5 μs	–	–	± 2	LSB
Integral linearity error	ILE	AV _{REF} = 5 V		–	± 1	
Differential linearity error	DLE	AV _{SS} = 0 V		–	± 1	
Offset error of top	EOT			± 1	± 2	
Offset error of bottom	EOB			± 0.5	± 2	
Conversion time ⁽¹⁾	t _{CON}	8 bit conversion 34 x n/f _{OSC} ⁽³⁾ , n=1,4,8,16	17	–	170	μs
Analog input voltage	V _{IAN}	–	AV _{SS}	–	AV _{REF}	V
Analog input impedance	R _{AN}	–	2	1000	–	mΩ
Analog reference voltage	AV _{REF}	–	2.5	–	V _{DD}	V
Analog ground	AV _{SS} ⁽⁴⁾	–	V _{SS}	–	V _{SS}	V
Analog input current	I _{ADIN}	AV _{REF} = V _{DD} = 5V	–	–	10	μA
Analog block Current ⁽²⁾	I _{ADC}	AV _{REF} = V _{DD} = 5V	–	1	3	mA
		AV _{REF} = V _{DD} = 3V		0.5	1.5	mA
		AV _{REF} = V _{DD} = 5V When power down mode		100	500	nA

NOTES:

- "Conversion time" is the time required from the moment a conversion operation starts until it ends.
- I_{ADC} is an operating current during the A/D conversion.
- f_{OSC} is the main oscillator clock.
- V_{SS} port shaves with the AV_{SS} for S3C8625/C8627/C8629.

Table 19-6. A.C. Electrical Characteristics

(T_A = -40 °C to +85 °C, V_{DD} = 4.0 V to 5.5V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Noise Filter	t _{NF1H} t _{NF1L}	INT0-2, TM0CAP and TM1CK (RC delay)	300	-	-	ns
	t _{NF2}	RESET only (RC delay)	800	-	-	

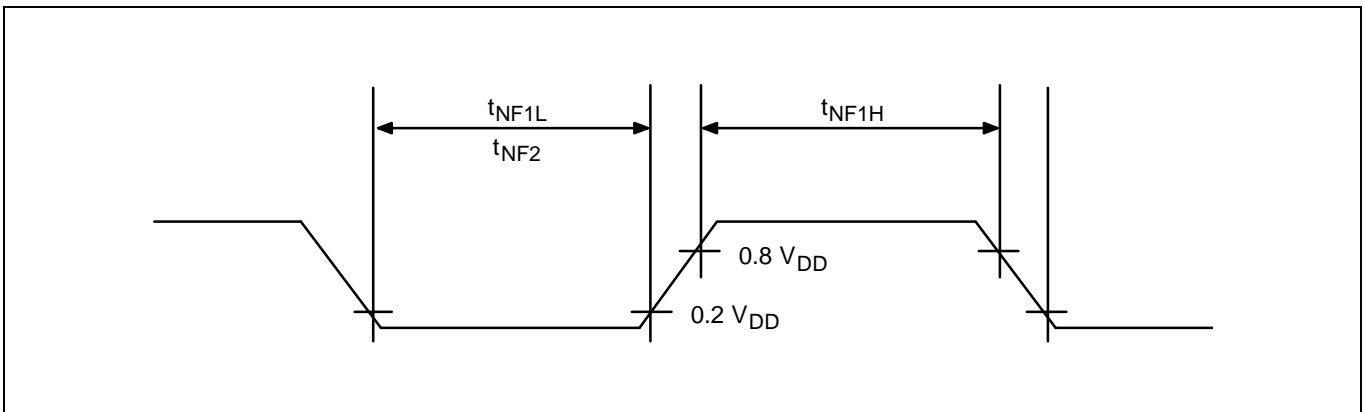
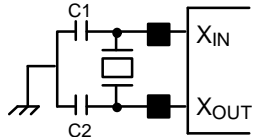
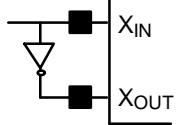


Figure 19-2. Input Timing Measurement Points for P0.0-P0.2, TM0CAP, and TM1CK

Table 19-7. Oscillation Characteristics

($T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$)

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Main crystal or ceramic		$V_{DD} = 4.0\text{ V to } 5.5\text{ V}$	8	–	12	MHz
External clock (main)		$V_{DD} = 4.0\text{ V to } 5.5\text{ V}$	8	–	12	MHz

NOTE: The maximum oscillator frequency is 12 MHz. If you use an oscillator frequency higher than 12 MHz, you cannot select a non-divided CPU clock using CLKCON settings. That is, you must select one of the divide-by values.

Table 19-8. Oscillation Stabilization Time

($T_A = -40\text{ }^\circ\text{C} + 85\text{ }^\circ\text{C}$, $V_{DD} = 4.0\text{ V to } 5.5\text{ V}$)

Oscillator	Test Condition	Min	Typ	Max	Unit
Crystal	$V_{DD} = 4.0\text{ V to } 5.5\text{ V}$	–	–	20	ms
Ceramic	$V_{DD} = 4.0\text{ V to } 5.5\text{ V}$	–	–	10	
External clock	X_{IN} input high and low level width (t_{XH} , t_{XL})	25	–	500	ns

NOTE: Oscillation stabilization time is the time required for the CPU clock to return to its normal oscillation frequency after a power-on occurs, or when Stop mode is released.

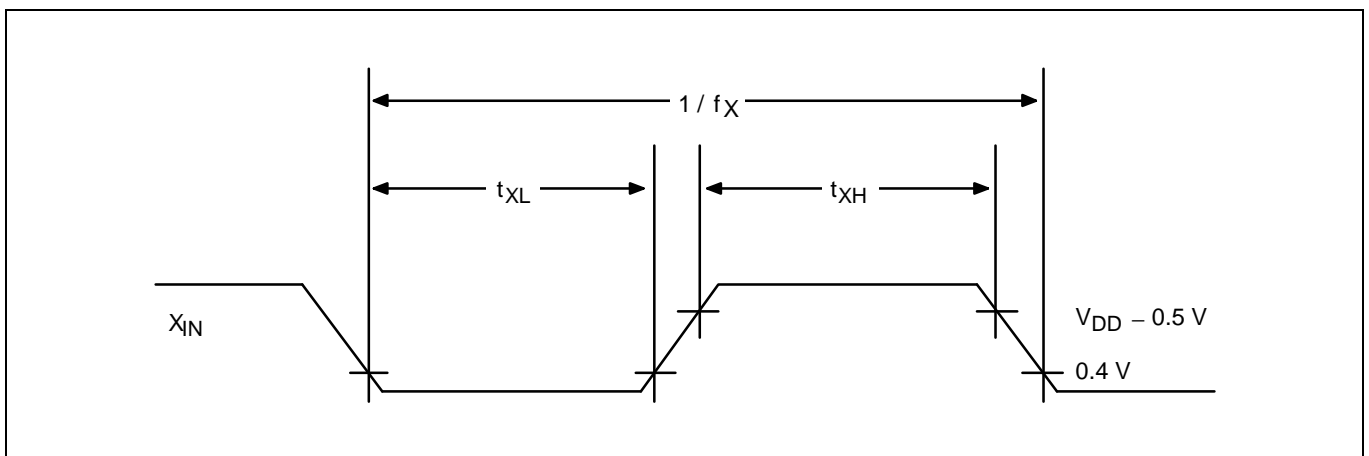


Figure 19-3. Clock Timing Measurement Points for X_{IN}

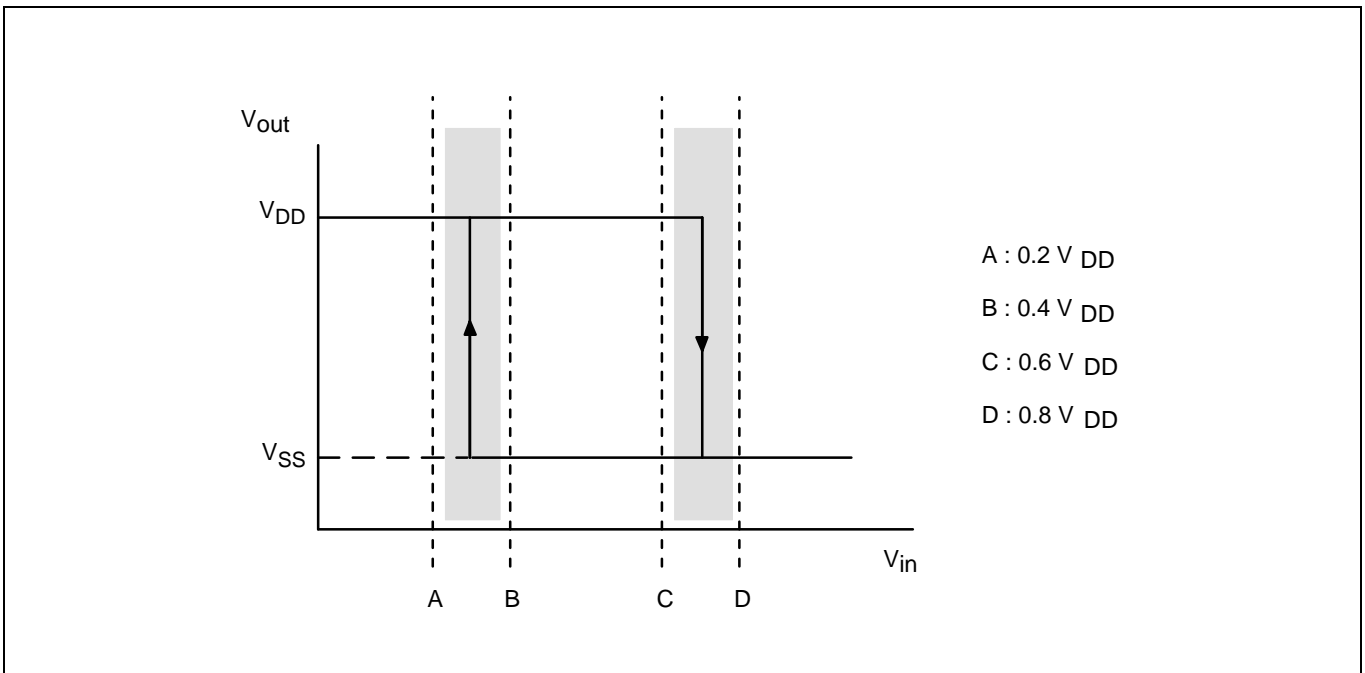


Figure 19-4. Schmitt Trigger Characteristics (Normal Port; except TTL Input)

20 MECHANICAL DATA

OVERVIEW

The S3C8625/C8627/C8629 microcontroller is available in a 42-pin SDIP package (Samsung part number 42-SDIP-600) and a 44-QFP package (Samsung part number 44-QFP-1010B).

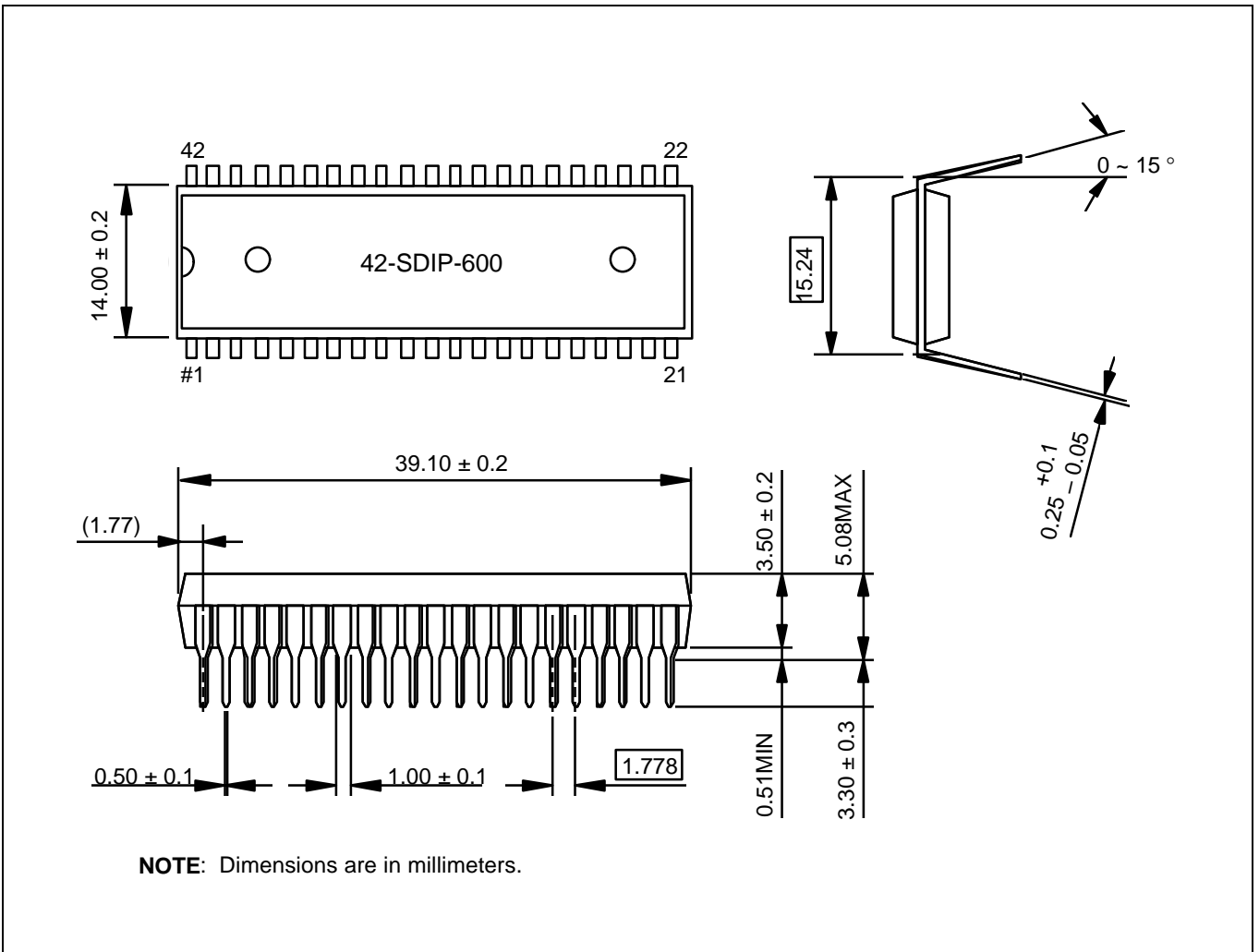


Figure 20-1. 42-Pin SDIP Package Mechanical Data (42-SDIP-600)

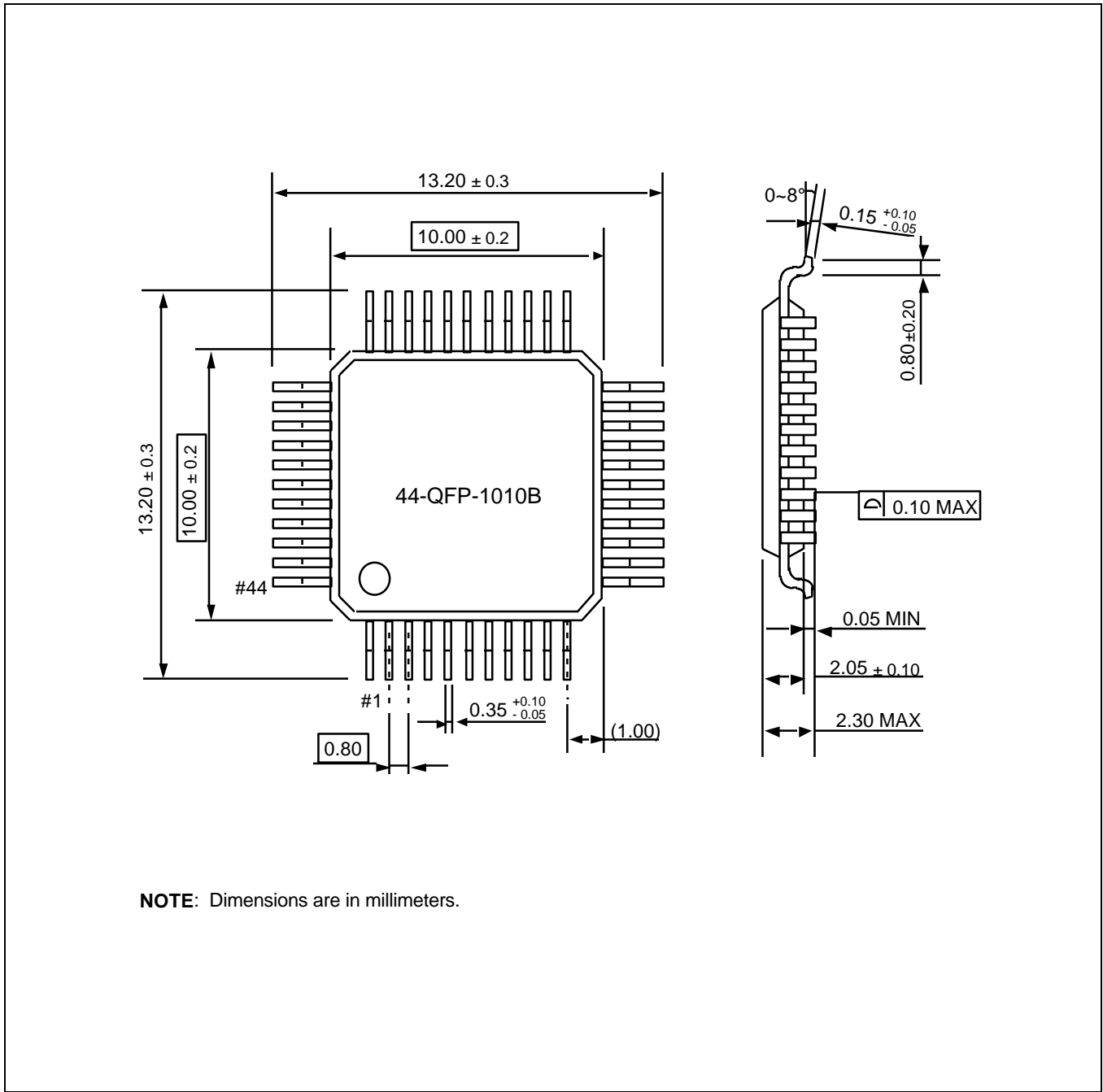


Figure 20-2. 44-Pin QFP Package Mechanical Data (44-QFP-1010B)

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S3P8629 OTP

OVERVIEW

The S3P8629 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C8625/C8627/C8629 microcontrollers. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by serial data format.

The S3P8629 is fully compatible with the S3C8625/C8627/C8629, both in function and in pin configuration. Because of its simple programming requirements, the S3P8629 is ideal for use as an evaluation chip for the S3C8625/C8627/C8629.

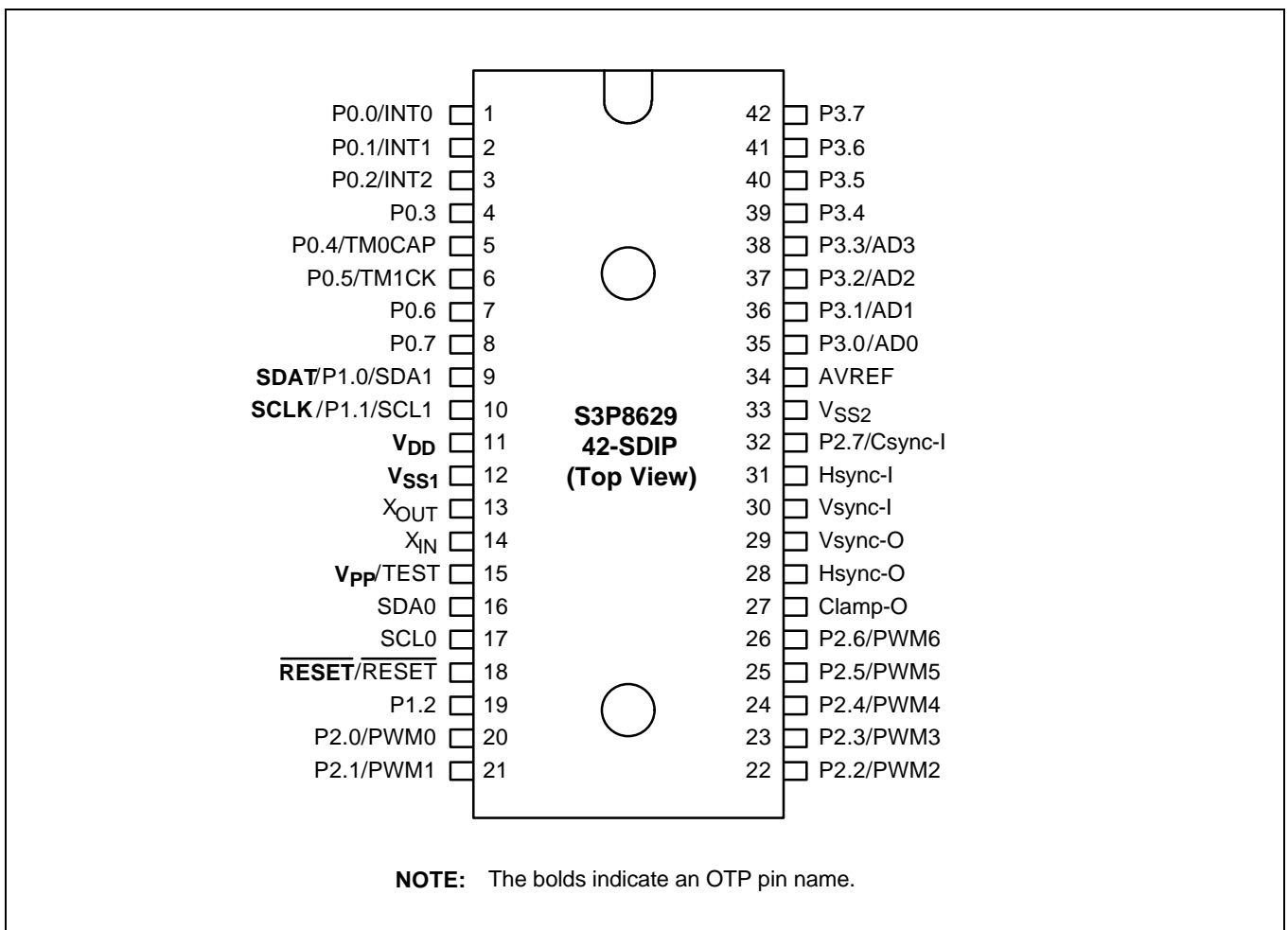


Figure 21-1. S3P8629 Pin Assignments (42-SDIP Package)

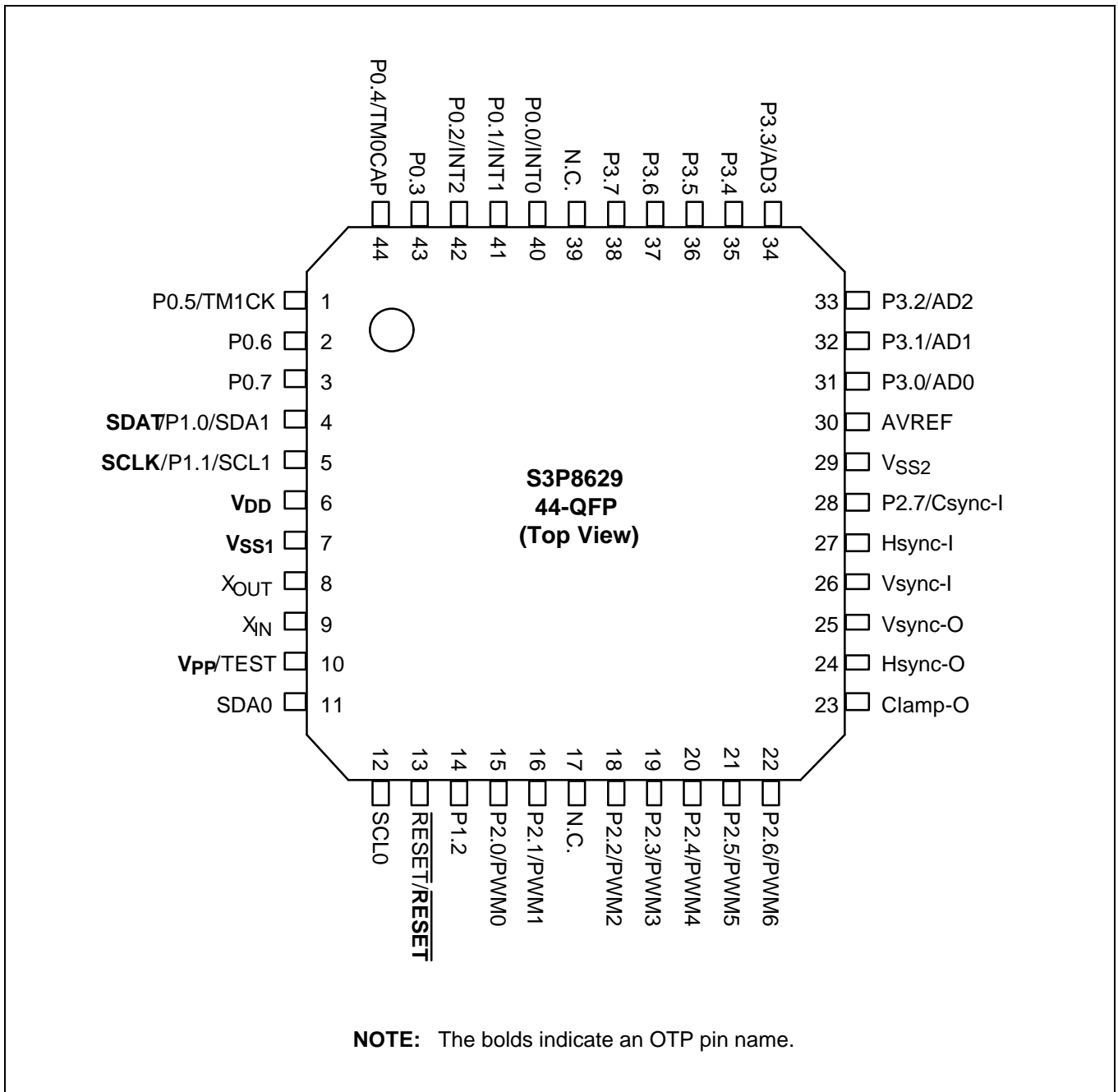


Figure 21-2. S3P8629 Pin Assignments (44-QFP Package)

Table 21-1. Descriptions of Pins Used to Read/Write the EPROM

Main Chip Pin Name	During Programming			
	Pin Name	Pin No.	I/O	Function
P1.0	SDAT	9 (4)	I/O	Serial data pin. Output port when reading and input port when writing. Can be assigned as a Input/push-pull output port.
P1.1	SCLK	10 (5)	I	Serial clock pin. Input only pin.
TEST	V _{PP} (TEST)	15 (10)	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	18 (13)	I	Chip Initialization
V _{DD} /V _{SS1}	V _{DD} /V _{SS1}	11/12 (6/7)	I	Logic power supply pin. V _{DD} should be tied to +5 V during programming.

NOTE: Parentheses indicate 44-QFP OTP pin number.

Table 21-2. Comparison of S3P8629 and S3C8625/C8627/C8629 Features

Characteristic	S3P8629	S3C8625/C8627/C8629
Program Memory	32-Kbyte EPROM	16/24/32-Kbyte mask ROM
Operating Voltage (V _{DD})	4.0 V to 5.5 V	4.0 V to 5.5V
OTP Programming Mode	V _{DD} = 5 V, V _{PP} (TEST)=12.5V	
Pin Configuration	42SDIP, 44QFP	42SDIP, 44QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP}(TEST) pin of the S3P8629, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 21-3. Operating Mode Selection Criteria

V _{DD}	V _{PP} (TEST)	REG/ MEM	ADDRESS (A15–A0)	R/W	MODE
5 V	5 V	0	0000H	1	EPROM read
	12.5 V	0	0000H	0	EPROM program
	12.5 V	0	0000H	1	EPROM verify
	12.5 V	1	0E3FH	0	EPROM read protection

NOTE: "0" means Low level; "1" means High level.

D.C. ELECTRICAL CHARACTERISTICS

Table 21-4. D.C. Electrical Characteristics

($T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{DD} = 4.0\text{ V}$ to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input High leakage current	I_{LIH1}	$V_{IN} = V_{DD}$ All input pins except X_{IN} , X_{OUT}	–	–	3	μA
	I_{LIH2}	$V_{IN} = V_{DD}$; X_{OUT} only	–	–	20	
	I_{LIH3}	$V_{IN} = V_{DD}$; X_{IN} only	2.5	6	20	
Input Low leakage current	I_{LIL1}	$V_{IN} = 0\text{ V}$; All input pins except X_{IN} , X_{OUT} , and RESET	–	–	–3	μA
	I_{LIL2}	$V_{IN} = 0\text{ V}$; X_{OUT} only	–	–	–20	
	I_{LIL3}	$V_{IN} = 0\text{ V}$; X_{IN} only	–2.5	–6	–20	
Output High leakage current	I_{LOH1}	$V_{OUT} = V_{DD}$	–	–	3	μA
Output Low leakage current	I_{LOL1}	$V_{OUT} = 0\text{ V}$	–	–	–3	μA
Pull-up resistor	R_{L1}	$V_{IN} = 0\text{ V}$ Ports 3.7–3.4	20	47	80	$\text{k}\Omega$
	R_{L2}	$V_{IN} = 0\text{ V}$ RESET only	150	280	480	
Supply current (note)	I_{DD1}	Operation mode; 12 MHz crystal $C1 = C2 = 22\text{pF}$	–	15	30	mA
	I_{DD2}	Idle mode; 12 MHz crystal $C1 = C2 = 22\text{pF}$		5	10	
	I_{DD3}	Stop mode		1	10	μA

NOTE: Supply current does not include drawn internal pull-up resistors and external loads of output.