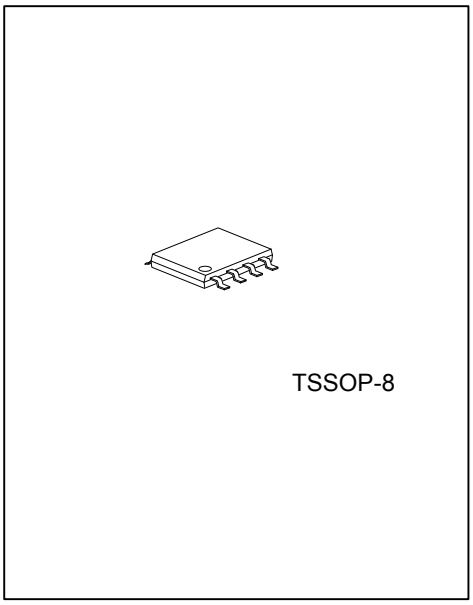
U74LVC2G240

CMOS IC

DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



■ DESCRIPTION

The **U74LVC2G240** is a dual buffer or driver with 3-state outputs. It is designed for 1.65V to 5.5V operation.
The **U74LVC2G240** is composed of two 1-bit buffers/drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, data passes from A (input) to Y (output). When $\overline{OE}$ is high, the outputs are in the high-impedance state.
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor, and the minimum value of the resistor is determined by the current-sinking capability of the driver.
The **U74LVC2G240** is fully specified for partial-power-down applications using I_{OFF}. The I_{OFF} circuitry disables the outputs and prevents damaging current backflow through the device when it is powered down.

■ FEATURES

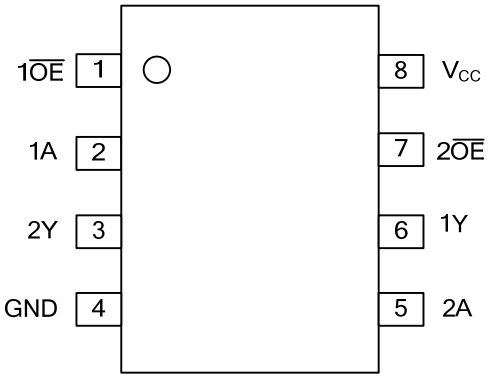
* Wide Supply Voltage Range from 1.65V to 5.5V
* Max t_{PD} of 4.6 ns at 3.3V
* Up to 5.5V Inputs Accept Voltages
* Low Power Consumption, I_{CC} = 10 μA (Max.)
* ±24 mA Output Driver at 3.3V
* Typical V_{OLP} (Output Ground Bounce) < 0.8V, V_{CC} = 3.3 V, T_A = 25 ℃
* Typical V_{OHV} (Output V_{OH} Undershoot) > 2V, V_{CC} = 3.3 V, T_A = 25 ℃

■ ORDERING INFORMATION

Ordering Number	Package	Packing
U74LVC2G240G-P08-R	TSSOP-8	Tape Reel

U74LVC2G240G-P08-R (1) Packing Type (2) Package Type (3) Halogen Free	(1) R: Tape Reel (2) P08:TSSOP-8 (3) G: Halogen Free

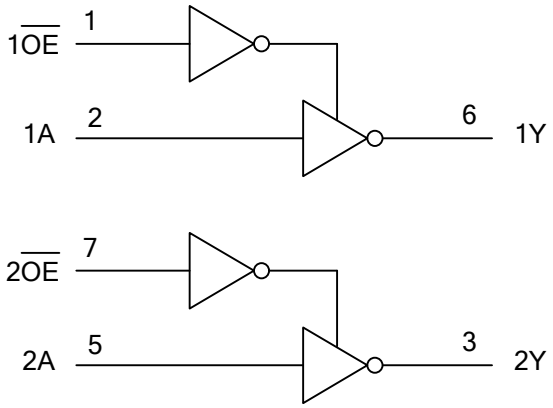
■ PIN CONFIGURATION



■ FUNCTION TABLE (Each Buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

■ LOGIC DIAGRAM (Positive Logic)



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~6.5	V
Input Voltage	V_{IN}	-0.5~6.5	V
Output Voltage (any output in the high-impedance or power-off state)	V_{OUT}	-0.5~6.5	V
Output Voltage (any output in the high or low state)	V_{OUT}	-0.5~V_{CC}+0.5	V
Input Clamp Current	I_{IK}	-50	mA
Output Clamp Current	I_{OK}	-50	mA
Output Current	I_{OUT}	±50	mA
V_{CC} or GND Current	I_{CC}	±100	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	RATINGS	UNIT
Junction to Ambient	θ_{JA}	190	°C /W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
High-Level Input Voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65* V_{CC}			V
		V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 3V to 3.6V	2			
		V_{CC} = 4.5V to 5.5V	0.7* V_{CC}			
Low-Level Input Voltage	V_{IL}	V_{CC} = 1.65V to 1.95V			0.35* V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.8	
		V_{CC} = 4.5V to 5.5V			0.3* V_{CC}	
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}	High or low state	0		V_{CC}	V
		3-state	0		5.5	
High-Level Output Current	I_{OH}	V_{CC}=1.65V			-4	mA
		V_{CC}=2.3V			-8	
		V_{CC}=3V			-16	
					-24	
		V_{CC}=4.5V			-32	
Low-Level Output Current	I_{OL}	V_{CC}=1.65V			4	mA
		V_{CC}=2.3V			8	
		V_{CC}=3V			16	
					24	
		V_{CC}=4.5V			32	
Input Transition Rise or Fall Rate	t_R / t_F	V_{CC}=1.8±0.15V, 2.5±0.2V			20	ns/V
		V_{CC}=3.3±0.3V			10	
		V_{CC}=5.0+0.5V			5	
Operating Temperature	T_{OPR}		-40		85	°C

■ ELECTRICAL CHARACTERISTICS (T_A =25°C , V_{CC} = 3.3 V, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
High-Level Output Voltage	V_{OH}	I_{OH} = -100 μA	V_{CC} = 1.65V to 5.5V	V_{CC} -0.1			V
		I_{OH} = -4 mA	V_{CC} = 1.65V	1.2			
		I_{OH} = -8 mA	V_{CC} = 2.3V	1.9			
		I_{OH} = -16 mA	V_{CC} = 3V	2.4			
		I_{OH} = -24 mA	V_{CC} = 3V	2.3			
		I_{OH} = -32 mA	V_{CC} = 4.5V	3.8			
Low-Level Output Voltage	V_{OL}	I_{OL} = 100 μA	V_{CC} = 1.65V to 5.5V			0.1	V
		I_{OL} = 4 mA	V_{CC} = 1.65V			0.45	
		I_{OL} = 8 mA	V_{CC} = 2.3V			0.3	
		I_{OL} = 16 mA	V_{CC} = 3V			0.4	
		I_{OL} = 24 mA	V_{CC} = 3V			0.55	
		I_{OL} = 32 mA	V_{CC} = 4.5V			0.55	
Input Leakage Current (A or $\overline{OE}$ inputs)	$I_{I(LEAK)}$	V_{IN} = 5.5V or GND, V_{CC} = 0 to 5.5V				±5	μA
OFF-State Current	I_{OFF}	V_{IN} or V_O = 5.5V, V_{CC} = 0V				±10	μA
High-Impedance State Current	I_{OZ}	V_O = 0 to 5.5V, V_{CC} = 3.6V				10	μA
Quiescent Supply Current	I_Q	V_{IN} = 5.5V or GND, I_{OUT} = 0, V_{CC} = 1.65V to 5.5V				10	μA
Additional quiescent Supply Current	ΔI_Q	One input at V_{CC} – 0.6V; other inputs at V_{CC} or GND; V_{CC}=3V to 5.5V				500	μA
Input Capacitance	C_{IN}	V_{IN} = V_{CC} or GND, V_{CC}=3.3V			4		pF
Output Capacitance	C_{OUT}	V_{OUT} = V_{CC} or GND, V_{CC}=3.3V			6		pF

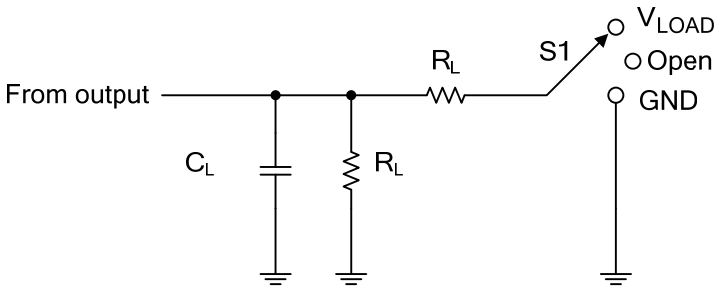
■ SWITCHING CHARACTERISTICS (T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Propagation Delay from Input A to Output Y	t_{PLH} / t_{PHL} (t_{PD})	V_{CC}=1.8±0.15V, R_L=1KΩ		C_L=30pF	2		11.3	ns
		V_{CC}=2.5±0.2V, R_L=500Ω			1.4		5.5	
		V_{CC}=3.3±0.3V, R_L=500Ω	R_L=500Ω	C_L=50pF	1.1		4.6	
		V_{CC}=5±0.5V, R_L=500Ω			1		4	
Propagation Delay from Input $\overline{OE}$ to Output Y	t_{PZL} / t_{PZH} (t_{EN})	V_{CC}=1.8±0.15V, R_L=1KΩ		C_L=30pF	2.7		11.7	ns
		V_{CC}=2.5±0.2V, R_L=500Ω			1.9		6.6	
		V_{CC}=3.3±0.3V	R_L=500Ω	C_L=50pF	1.4		5.4	
		V_{CC}=5±0.5V			1.1		5	
Propagation Delay from Input $\overline{OE}$ to Output Y	t_{PLZ} / t_{PHZ} (t_{DIS})	V_{CC}=1.8±0.15V, R_L=1KΩ		C_L=30pF	1.7		12.8	ns
		V_{CC}=2.5±0.2V, R_L=500Ω			0.8		5.7	
		V_{CC}=3.3±0.3V	R_L=500Ω	C_L=50pF	1.2		5.5	
		V_{CC}=5±0.5V			0.5		4.2	

■ OPERATING CHARACTERISTICS (T_A =25°C)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN	TYP	MAX	UNIT
Power Dissipation Capacitance per buffer/driver	C_{PD}	Outputs enabled	V_{CC} = 1.8V	f=10MHz				pF
			V_{CC} = 2.5V					
			V_{CC} = 3.3V			15		
			V_{CC} = 5V			17		
		Outputs disabled	V_{CC} = 1.8V	f=10MHz		1		pF
			V_{CC} = 2.5V			1		
			V_{CC} = 3.3V			2		
			V_{CC} = 5V			2		

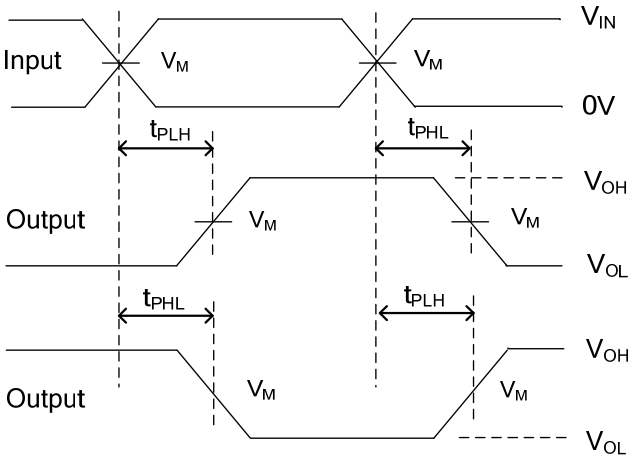
■ TEST CIRCUIT AND WAVEFORMS



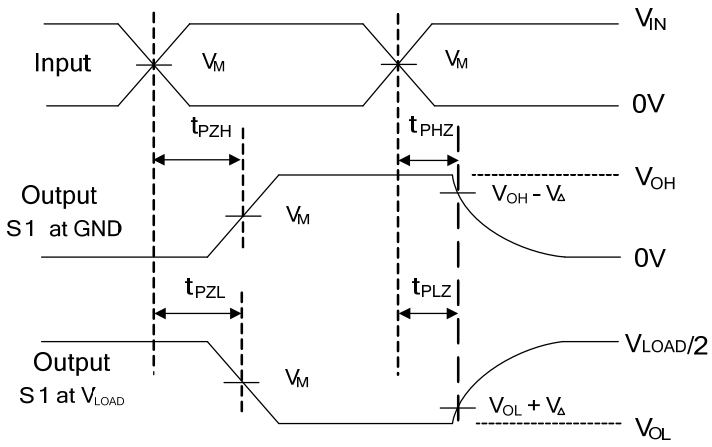
TEST CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_{IN}	t_R, t_F					
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	$2*V_{CC}$	30pF	1KΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	$2*V_{CC}$	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	$2*V_{CC}$	50pF	500Ω	0.3V



Propagation delay times
Inverting and noninverting outputs



Enable and disable times
Low and high level enabling

Notes: 1. C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤10MHz, Z_O = 50Ω.