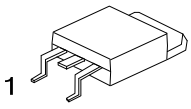
# 12 Amps, 100 Volts
# N-CHANNEL POWER MOSFET




TO-252

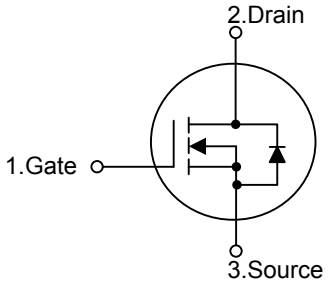
## ■ DESCRIPTION

The UTC **UT12N10** is an N-channel mode Power FET using UTC's advanced technology to provide custumers with minimum on-state resistance by extremely high dense cell design. Moreover, it' s good at handing high power and current.

## ■ FEATURES

* 100V, 12A, $R_{DS(ON)}$ = 180mΩ @$V_{GS}$ = 10V.
* Be good at handing high power and current.
* Very high dense cell design for super low $R_{DS(ON)}$.
* Lead free product is acquired.

## ■ SYMBOL




## ■ ORDERING INFORMATION

| Ordering Number | | Package | Pin Assignment | | | Packing |
|---|---|---|---|---|---|---|
| Lead Free | Halogen Free | | 1 | 2 | 3 | |
| UT12N10L-TN3-R | UT12N10G-TN3-R | TO-252 | G | D | S | Tape Reel |

Note: Pin Assignment: G: Gate D: Drain S: Source

UT12N10L-TN3-R

| | |
|---|---|
| (1)Packing Type | (1) R: Tape Reel |
| (2)Package Type | (2) TN3: TO-252 |
| (3)Lead Free | (3) G: Halogen Free, L: Lead Free |

## ■ ABSOLUTE MAXIMUM RATINGS ($T_C$=25°C, unless otherwise noted)

| PARAMETER | | SYMBOL | RATINGS | UNIT |
|---|---|---|---|---|
| Drain-Source Voltage | | $V_{DSS}$ | 100 | V |
| Gate-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Drain Current | Continuous | $I_D$ | 12 | A |
| | Pulsed (Note 1) | $I_{DM}$ | 44 | A |
| Power Dissipation | | $P_D$ | 43 | W/°C |
| Junction Temperature | | $T_J$ | +150 | °C |
| Storage Temperature | | $T_{STG}$ | -55~+150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

Note:1 Repetitive Rating: Pulse width limited by maximum junction temperature

## ■ THERMAL CHARACTERISTICS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Junction to Ambient (Note 2) | $\theta_{JA}$ | 50 | °C/W |
| Junction to Case | $\theta_{JC}$ | 3.5 | °C/W |

Note: $\theta_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.
$\theta_{JC}$ is guaranteed by design while $\theta_{JA}$ is determined by the user's board design.

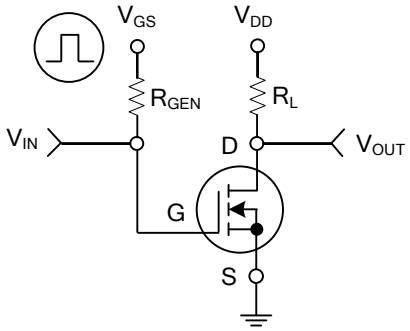
Note:2 When mounted on a 1 $in^2$ pad of 2 oz copper

## ■ ELECTRICAL CHARACTERISTICS ($T_C$=25°C, unless otherwise noted)

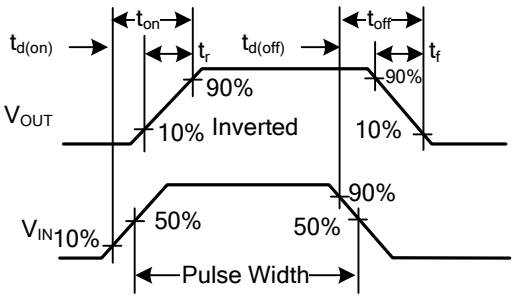
| PARAMETER | | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain-Source Breakdown Voltage | | $BV_{DSS}$ | $I_D$=250μA, $V_{GS}$=0V | 100 | | | V |
| Drain-Source Leakage Current | | $I_{DSS}$ | $V_{DS}$=100V, $V_{GS}$=0V | | | 1 | μA |
| Gate- Source Leakage Current | Forward | $I_{GSS}$ | $V_{GS}$=+20V, $V_{DS}$=0V | | | +100 | nA |
| | Reverse | | $V_{GS}$=-20V, $V_{DS}$=0V | | | -100 | nA |
| **ON CHARACTERISTICS** (Note 1) | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 2 | | 4 | V |
| Static Drain-Source On-State Resistance | | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=6A | | 150 | 180 | mΩ |
| Forward Transconductance | | $g_{FS}$ | $V_{DS}$=10V, $I_D$=6A | | 5 | | S |
| **DYNAMIC PARAMETERS** (Note 2) | | | | | | | |
| Input Capacitance | | $C_{ISS}$ | $V_{GS}$=0V, $V_{DS}$=25V, f=1.0MHz | | 430 | | pF |
| Output Capacitance | | $C_{OSS}$ | | | 90 | | pF |
| Reverse Transfer Capacitance | | $C_{RSS}$ | | | 20 | | pF |
| **SWITCHING PARAMETERS** (Note 2) | | | | | | | |
| Total Gate Charge | | $Q_G$ | $V_{GS}$=10V, $V_{DS}$=80V, $I_D$=12A | | 8 | 16 | nC |
| Gate to Source Charge | | $Q_{GS}$ | | | 1.5 | | nC |
| Gate to Drain Charge | | $Q_{GD}$ | | | 2 | | nC |
| Turn-ON Delay Time | | $t_{D(ON)}$ | $V_{DD}$=80V, $I_D$=12A, $V_{GS}$=10V, $R_G$=9.1Ω | | 12 | 24 | ns |
| Rise Time | | $t_R$ | | | 7 | 14 | ns |
| Turn-OFF Delay Time | | $t_{D(OFF)}$ | | | 18 | 35 | ns |
| Fall-Time | | $t_F$ | | | 3 | 6 | ns |
| **SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS** | | | | | | | |
| Maximum Body-Diode Continuous Current | | $I_S$ | | | | 12 | A |
| Drain-Source Diode Forward Voltage (Note 1) | | $V_{SD}$ | $I_S$=12A, $V_{GS}$=0V | | | 1.2 | V |

Note: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%
2. Guaranteed by design, not subject to production testing.

## ■ TEST CIRCUITS AND WAVEFORMS




Switching Test Circuit




Switching Waveforms