





EH35 25

Series -RoHS Compliant (Pb-free) 5.0V 4 Pad 3.2mm x 5mm Ceramic SMD HCMOS/TTL High Frequency Oscillator

Frequency Tolerance/Stability ±25ppm Maximum

Operating Temperature Range – 0°C to +70°C

TS -35.328M

Nominal Frequency 35.328MHz

- Pin 1 Connection Tri-State (Disabled Output: High Impedance)

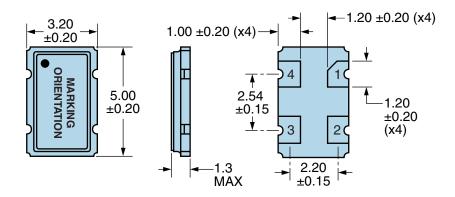
Duty Cycle 50 ±10(%)

#25ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration) Aging at 25°C #5ppm/year Maximum O°C to +70°C Supply Voltage 5.0Vdc ±10% Input Current 50mA Maximum (No Load) Output Voltage Logic High (Voh) Output Voltage Logic Low (Vol) Rise/Fall Time 6nSec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load) Duty Cycle 50±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Output Logic Type CMOS Pin 1 Connection Tri-State Input Voltage (Vih and Vil) 4250pSec Maximum, ±100pSec Typical Start Up Time 10mSec Maximum, ±30pSec Typical Start Up Time 10c C to +70°C ±5ppm/year Maximum #25°C, Shock, and Vibration Tolerance at 25°C, Frequency Stability over the Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration) #250ppm Maximum (Inclusive of all conditions: Calibration Tolerance at 25°C, Frequency Stability Over the Operating Auging at 25°C, Shock, and Vibration) #250ppm Maximum (Inclusive Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration) #250ppm Maximum (No Load) #250ppm Maximum (No Load) 0.4 Vdc Minimum with TTL Load, Vdd-0.4Vdc Minimum with HCMOS Load (IOL = -16mA) 0.4 Vdc Maximum (Measured at 0.8Vdc Maximum with HCMOS Load (IOL = -16mA) 0.4 Vdc Maximum (Measured at 0.8Vdc Maximum with HCMOS Load (IOL = -16mA) 1.5 Vdc Minimum to enable output: High Impedance)	ELECTRICAL SPECIFICATIONS		
Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C, Shock, and Vibration) ±5ppm/year Maximum O°C to +70°C Supply Voltage Input Current SomA Maximum (No Load) Output Voltage Logic High (Voh) Output Voltage Logic Low (Vol) Rise/Fall Time On Sec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load) Duty Cycle 50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Load Drive Capability Output Logic Type CMOS Pin 1 Connection Tri-State Input Voltage (Vih and Vil) Absolute Clock Jitter ±250pSec Maximum, ±30pSec Typical Start Up Time O°C to +70°C \$50 ±50 +00°C \$50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) ### Connection Tri-State Input Voltage (Vih and Vil) ±50pSec Maximum, ±100pSec Typical \$50 ±20pSec Maximum, ±30pSec Typical \$50 ±50pSec Maximum, ±30pSec Typical	Nominal Frequency	35.328MHz	
Operating Temperature Range O°C to +70°C Supply Voltage 5.0Vdc ±10% Input Current 50mA Maximum (No Load) Output Voltage Logic High (Voh) Output Voltage Logic Low (Vol) O.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOH = -16mA) Output Voltage Logic Low (Vol) O.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOL = +16mA) Fise/Fall Time Onesc Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load) Output Cycle 50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Output Logic Type CMOS Output Logic Type CMOS Tri-State (Disabled Output: High Impedance) Tri-State Input Voltage (Vih and Vil) Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical Start Up Time 10mSec Maximum	Frequency Tolerance/Stability	Operating Temperature Range, Supply Voltage Change, Output Load Change, 1st Year Aging at 25°C,	
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Input Current 50mA Maximum (No Load) Output Voltage Logic High (Voh) 2.4Vdc Minimum with TTL Load, Vdd-0.4Vdc Minimum with HCMOS Load (IOH = -16mA) Output Voltage Logic Low (Vol) Rise/Fall Time 6nSec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load) Duty Cycle 50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Load Drive Capability 10TTL Load or 50pF HCMOS Load Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (Disabled Output: High Impedance) +2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical Start Up Time 10mSec Maximum 1.4Vdc Minimum with HCMOS Load (IOL = +16mA) 0.4Vdc Maximum with HCMOS Load (IOL = +16mA) 0	Operating Temperature Range	0°C to +70°C	
Output Voltage Logic High (Voh) 2.4Vdc Minimum with TTL Load, Vdd-0.4Vdc Minimum with HCMOS Load (IOH = -16mA) 0.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOL = +16mA) 6.Sec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load) Duty Cycle 50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Load Drive Capability 10TTL Load or 50pF HCMOS Load Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (Disabled Output: High Impedance) +2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output. Absolute Clock Jitter 2.50pSec Maximum, ±100pSec Typical ±50pSec Maximum, ±30pSec Typical Start Up Time 10mSec Maximum	Supply Voltage	5.0Vdc ±10%	
Output Voltage Logic Low (Vol) 0.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOL = +16mA) 6nSec Maximum (Measured at 0.8Vdc to 2.0Vdc with TTL Load or at 20% to 80% of waveform with HCMOS Load) Duty Cycle 50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Load Drive Capability 10TTL Load or 50pF HCMOS Load Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (Disabled Output: High Impedance) Tri-State Input Voltage (Vih and Vil) +2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical 50pSec Maximum, ±30pSec Typical 10mSec Maximum 10mSec Maximum	Input Current	50mA Maximum (No Load)	
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HCMOS Load) Duty Cycle 50 ±10(%) (Measured at 1.4Vdc with TTL Load or at 50% of waveform with HCMOS Load) Load Drive Capability 10TTL Load or 50pF HCMOS Load Maximum Output Logic Type CMOS Pin 1 Connection Tri-State (Disabled Output: High Impedance) Tri-State Input Voltage (Vih and Vil) +2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±30pSec Typical Start Up Time 10mSec Maximum	Output Voltage Logic Low (Vol)	0.4Vdc Maximum with TTL Load, 0.5Vdc Maximum with HCMOS Load (IOL = +16mA)	
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enable output. Absolute Clock Jitter ±250pSec Maximum, ±100pSec Typical One Sigma Clock Period Jitter ±50pSec Maximum, ±30pSec Typical Start Up Time 10mSec Maximum	Pin 1 Connection	Tri-State (Disabled Output: High Impedance)	
One Sigma Clock Period Jitter ±50pSec Maximum, ±30pSec Typical Start Up Time 10mSec Maximum	Tri-State Input Voltage (Vih and Vil)	+2.2Vdc Minimum to enable output, +0.8Vdc Maximum to disable output (High Impedance), No Connect to enable output.	
Start Up Time 10mSec Maximum	Absolute Clock Jitter	±250pSec Maximum, ±100pSec Typical	
·	One Sigma Clock Period Jitter	±50pSec Maximum, ±30pSec Typical	
Storage Temperature Range -55°C to +125°C	Start Up Time	10mSec Maximum	
	Storage Temperature Range	-55°C to +125°C	

ENVIRONMENTAL & MECHANICAL SPECIFICATIONS		
Fine Leak Test	MIL-STD-883, Method 1014, Condition A	
Gross Leak Test	MIL-STD-883, Method 1014, Condition C	
Mechanical Shock	MIL-STD-202, Method 213, Condition C	
Resistance to Soldering Heat	MIL-STD-202, Method 210	
Resistance to Solvents	MIL-STD-202, Method 215	
Solderability	MIL-STD-883, Method 2003	
Temperature Cycling	MIL-STD-883, MEthod 1010	
Vibration	MIL-STD-883, Method 2007, Condition A	



MECHANICAL DIMENSIONS (all dimensions in millimeters)

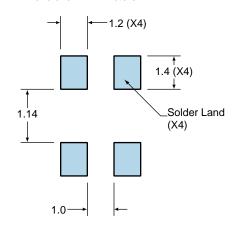


PIN CONNECTION	
1	Tri-State
2	Ground/Case Ground
3	Output
4	Supply Voltage

LINE	MARKING
1	E35.328 E=Ecliptek Designator

Suggested Solder Pad Layout

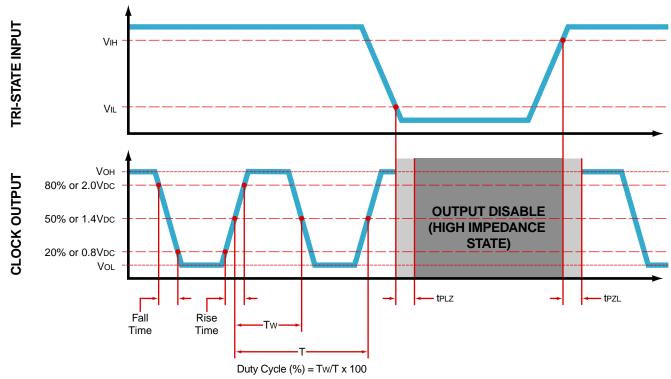
All Dimensions in Millimeters



All Tolerances are ±0.1



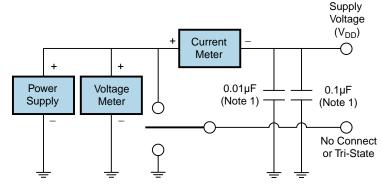
OUTPUT WAVEFORM & TIMING DIAGRAM

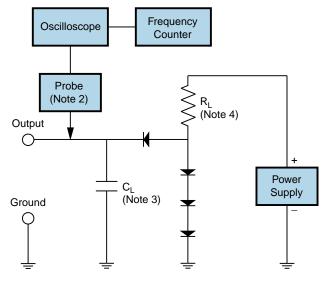


Test Circuit for TTL Output

Output Load Drive Capability	R _L Value (Ohms)	C _L Value (pF)
10TTL	390	15
5TTL	780	15
2TTL	1100	6
10LSTTL	2000	15
1TTL	2200	3

Table 1: R_L Resistance Value and C_L Capacitance Value Vs. Output Load Drive Capability





Note 1: An external $0.1\mu F$ low frequency tantalum bypass capacitor in parallel with a $0.01\mu F$ high frequency ceramic bypass capacitor close to the package ground and V_{DD} pin is required.

Note 2: A low capacitance (<12pF), 10X attenuation factor, high impedance (>10Mohms), and high bandwidth (>300MHz) passive probe is recommended.

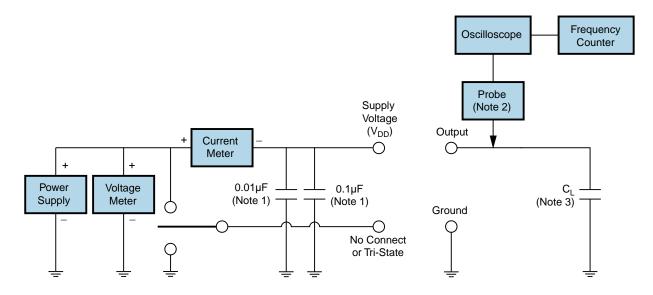
Note 3: Capacitance value C_{L} includes sum of all probe and fixture capacitance.

Note 4: Resistance value R_L is shown in Table 1. See applicable specification sheet for 'Load Drive Capability'.

Note 5: All diodes are MMBD7000, MMBD914, or equivalent.



Test Circuit for CMOS Output



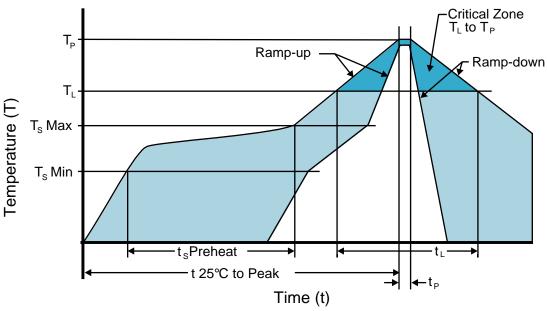
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Note 3: Capacitance value \dot{C}_L includes sum of all probe and fixture capacitance.



Recommended Solder Reflow Methods

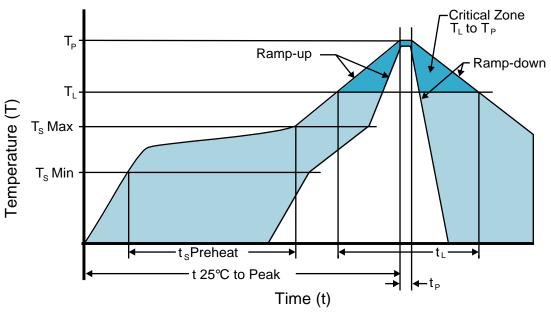


High Temperature Infrared/Convection

T _s MAX to T _∟ (Ramp-up Rate)	3°C/second Maximum
Preheat	
- Temperature Minimum (Ts MIN)	150°C
- Temperature Typical (T _s TYP)	175°C
- Temperature Maximum (T _s MAX)	200°C
- Time (t _s MIN)	60 - 180 Seconds
Ramp-up Rate (T _L to T _P)	3°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	217°C
- Time (t∟)	60 - 150 Seconds
Peak Temperature (T _P)	260°C Maximum for 10 Seconds Maximum
Target Peak Temperature (T _P Target)	250°C +0/-5°C
Time within 5°C of actual peak (tp)	20 - 40 seconds
Ramp-down Rate	6°C/second Maximum
Time 25°C to Peak Temperature (t)	8 minutes Maximum
Moisture Sensitivity Level	Level 1



Recommended Solder Reflow Methods



Low Temperature Infrared/Convection 240°C

T _S MAX to T _L (Ramp-up Rate)	5°C/second Maximum
Preheat	
- Temperature Minimum (T _s MIN)	N/A
- Temperature Typical (T _S TYP)	150°C
- Temperature Maximum (T _s MAX)	N/A
- Time (t _s MIN)	60 - 120 Seconds
Ramp-up Rate (T _L to T _P)	5°C/second Maximum
Time Maintained Above:	
- Temperature (T∟)	150°C
- Time (t∟)	200 Seconds Maximum
Peak Temperature (T _P)	240°C Maximum
Target Peak Temperature (T _P Target)	240°C Maximum 1 Time / 230°C Maximum 2 Times
Time within 5°C of actual peak (tp)	10 seconds Maximum 2 Times / 80 seconds Maximum 1 Time
Ramp-down Rate	5°C/second Maximum
Time 25°C to Peak Temperature (t)	N/A
Moisture Sensitivity Level	Level 1

Low Temperature Manual Soldering

185°C Maximum for 10 seconds Maximum, 2 times Maximum.

High Temperature Manual Soldering

260°C Maximum for 5 seconds Maximum, 2 times Maximum.