Positive Voltage Control of GaAs MMIC Control Devices

Rev. V3

Discussion

GaAs control devices have seen a tremendous growth in recent years with M/A-COM being the market leader in this area. The fact that these devices are negative voltage controlled devices has precluded the use of standard low cost CMOS drivers and has forced users to develop hybrid driver circuits to accomplish the driver function. This application note discusses a configuration which allows the user to drive GaAs control devices with standard CMOS logic gates. Although specific examples are presented, this application is generic and can be applied to any GaAs control device.

Design Approach

Since the GaAs FET requires a 0 V to -5 V relative voltage between the source and the gate, an alternative to using negative control voltage is to elevate or float the DC voltage at the source of the FET to +5 V and use a 0 V to +5 V control voltage. This would produce the required voltage differential between the source and gate to 0 V and -5 V. In many circuit applications, the source of the FET's are required to be RF ground. This grounding is very critical to circuit performance requiring the 5 V supply which is applied to the source be AC coupled to ground. Figure 1 shows a typical schematic of this topology for a single bit of a digital attenuator.

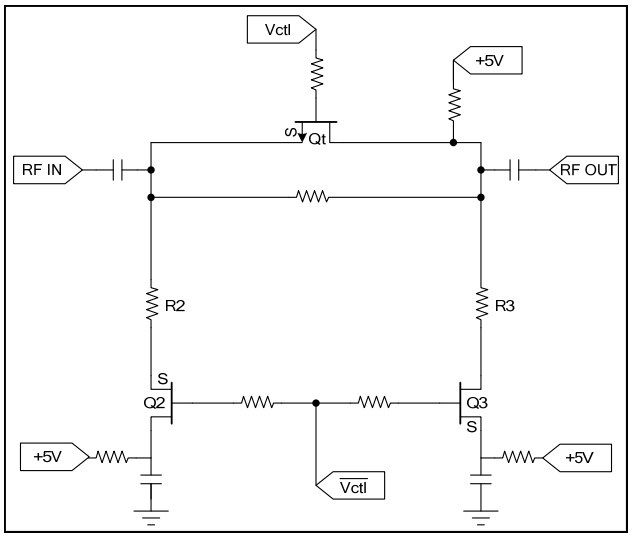

Figure 1.
Positive Voltage Control Configuration of a Single Attenuator Bit

Design Considerations

One area of concern in RF design is the adequate grounding of the devices. If good ground is not maintained, the performance of the device at the higher attenuation / isolation states will be degraded and will not meet the expected specification. When floating the source of a FET which is required to have a ground connection, the quality of the AC coupling capacitor and the PCB layout becomes extremely critical. The coupling capacitor must be a high-Q capacitor such as the ATC100A series supplied by American Technical Ceramics or equivalent. For operation at lower frequencies a higher value of capacitor must be chosen. Any increase in inductance or path length will degrade the performance of the device so the designer must exercise good judgment in the placement of components and the number of via holes used to pick up ground. The best solution would be to utilize a coplanar layout where the AC coupling capacitor can be soldered directly to ground. If a microstrip layout is used, the designer must use as many via holes as possible and place them in very close proximity to the capacitor.

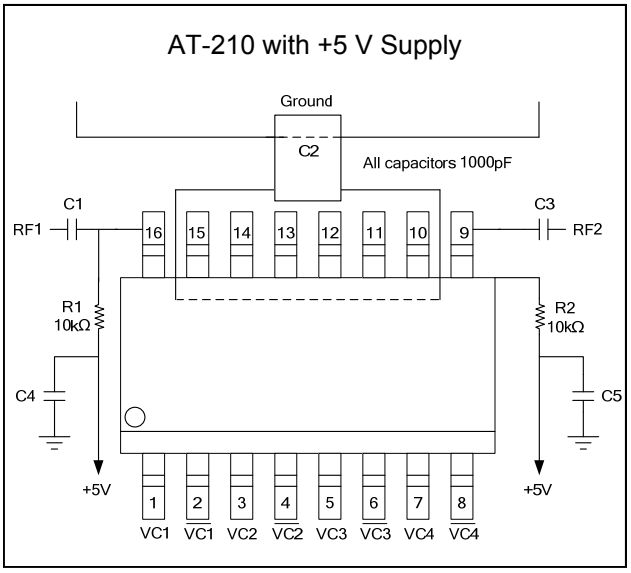

Figure 2a.
Positive Voltage Control Configuration of the AT-210

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Rev. V3

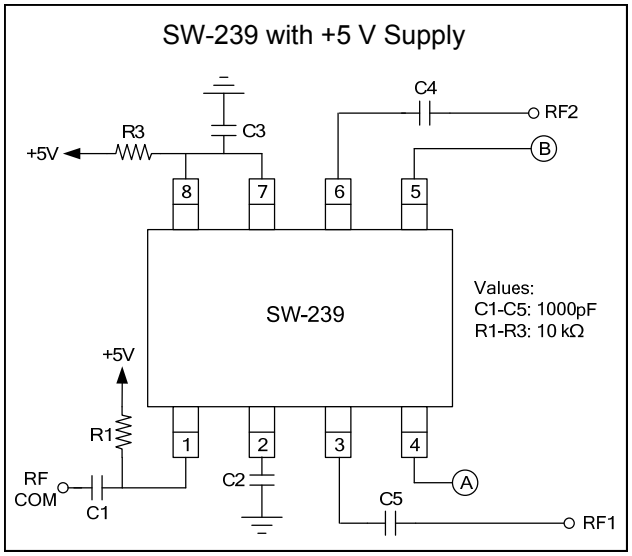

Figure 2b.
Positive Voltage Control Configuration of the SW-239

Applications

This type of voltage floating technique can be used in most control component applications. A typical switch and digital attenuator application are presented in Figure 2. Each application is similar in that the source of the FET's are biased at +5 V and the gates can be controlled by 0 and +5 V.

In all cases, the ground pins which have a source connection must be AC coupled with the shortest possible path to ground.

The AT-210 is shown as an example of a digital attenuator which is floated. Pins 10 through 15 are normally grounded, but in this case are floated to the +5 V supply and AC coupled to ground. One of the RF connections must also be tied to +5 V to ensure the source of the series FET's are floated. As mentioned above, all efforts to minimize inductance to ground must be taken to ensure the full attenuation range of the device. A truth table for the digital attenuator in the floated configuration is shown in Table 1.

Control Inputs								Attn (dB)
$\overline{VC4}$	VC4	$\overline{VC3}$	VC3	$\overline{VC2}$	VC2	$\overline{VC1}$	VC1	
0	1	0	1	0	1	0	1	Ref.
1	0	0	1	0	1	0	1	1
0	1	1	0	0	1	0	1	2
1	0	1	0	0	1	0	1	3
0	1	0	1	1	0	0	1	4
1	0	0	1	1	0	0	1	5
0	1	1	0	1	0	0	1	6
1	0	1	0	1	0	0	1	7
0	1	0	1	0	1	1	0	8
1	0	0	1	0	1	1	0	9
0	1	1	0	0	1	1	0	10
1	0	1	0	0	1	1	0	11
0	1	0	1	1	0	1	0	12
1	0	0	1	1	0	1	0	13
0	1	1	0	1	0	1	0	14
1	0	1	0	1	0	1	0	15

Table 1.
AT-210 Truth Table (+5 V Control)

The SW-239 is shown as an example of a SPDT switch which is floated using this technique. Pins 2, 7, and 8 are normally ground and must be floated with +5 V as well as being AC coupled to ground. A +5 V supply is also required at the RF common to ensure that the source of the series FET's are floated. The resistors R1 and R3 will result in slower switching speed, but will minimize coupling of RF signals along the +5 V line. A truth table for this device in the floated configuration is given in Table 2.

Control A	Control B	RF1	RF2
0 V	+5 V	ON	OFF
+5 V	0 V	OFF	ON

Table 2.
SW-239 Truth Table

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The AT-250 is a VVA that can, similarly, be floated for positive bias operation as shown in Figure 3.

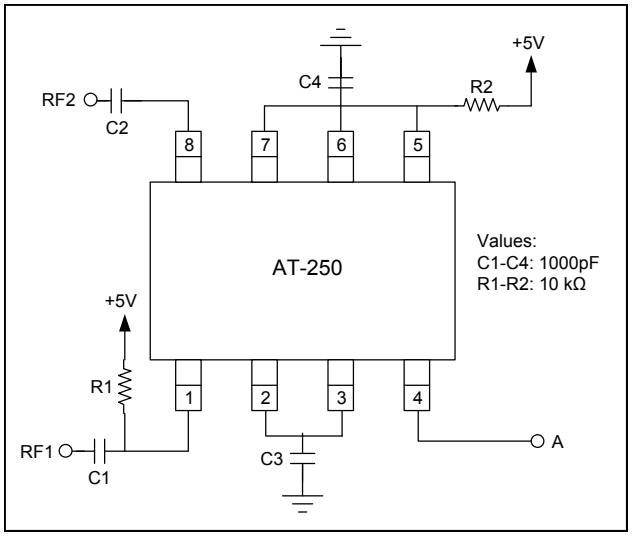

Figure 3.
Positive Voltage Control Configuration of the AT-250