DS05-11205-1E

MEMORY

CMOS 4M × 36 FAST PAGE MODE DRAM MODULE

MB85396A-60/-70

CMOS 4M × 36 Bit Fast Page Mode DRAM Module

■ DESCRIPTION

The Fujitsu MB85396A is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of eight MB8117400A devices and four MB814100C devices. The MB85396A is optimized for those applications requiring high speed, high performance and large memory storage. The operation and electrical characteristics of the MB85396A are the same as the MB8117400A which features fast page mode operation. For ease of memory expansion, the MB85396A is offered in a 72-pad Single In-line Memory Module package (SIMM).

■ ABSOLUTE MAXIMUM RATINGS (See NOTE.)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +7.0	V*1
Input Voltage	V_{IN}	–0.5 to +7.0	V*1
Output Voltage	V_{OUT}	–0.5 to +7.0	V*1
Short Circuit Output Current	I_{OUT}	±50	mA
Power Dissipation	P_D	12	W
Storage Temperature	T_{STG}	–55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

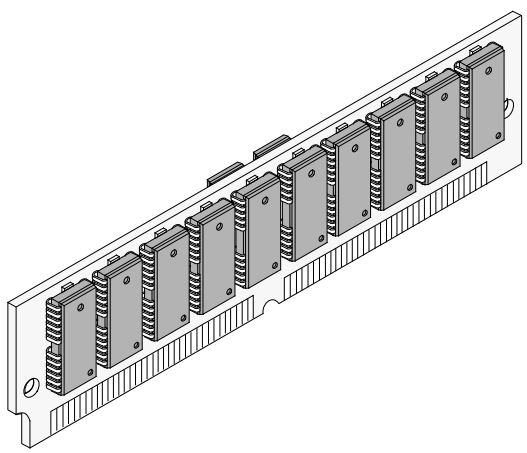
This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ PRODUCT LINE & FEATURES

Parameter		MB85396A-60	MB85396A-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		110 ns min.	130 ns min.
Address Access Time		30 ns max.	35 ns max.
$\overline{CAS}$ Access Time		15 ns max.	20 ns max.
Fast Page Mode Cycle Time		40 ns min.	45 ns min.
Power Dissipation	Operating Mode	5962 mW max.	5148 mW max.
	Standby Mode	66mW(CMOS) / 132mW(TTL)	

- Organization: 4,194,304 words x 36 bits (Parity)
- Memory : MB8117400A, 8 pcs
  MB814100C, 4 pcs
- Decoupling Capacitor, 12 pcs
- 5.0 V ± 10% Supply Voltage
- Fast Page operation
- Distributed refresh: 2,048 Refresh Cycles/32.8ms
- Package and Ordering Information: 72-pad SIMM, order as MB85396A–xxPJPBK (PJPBK = Gold Pad)

■ PACKAGE



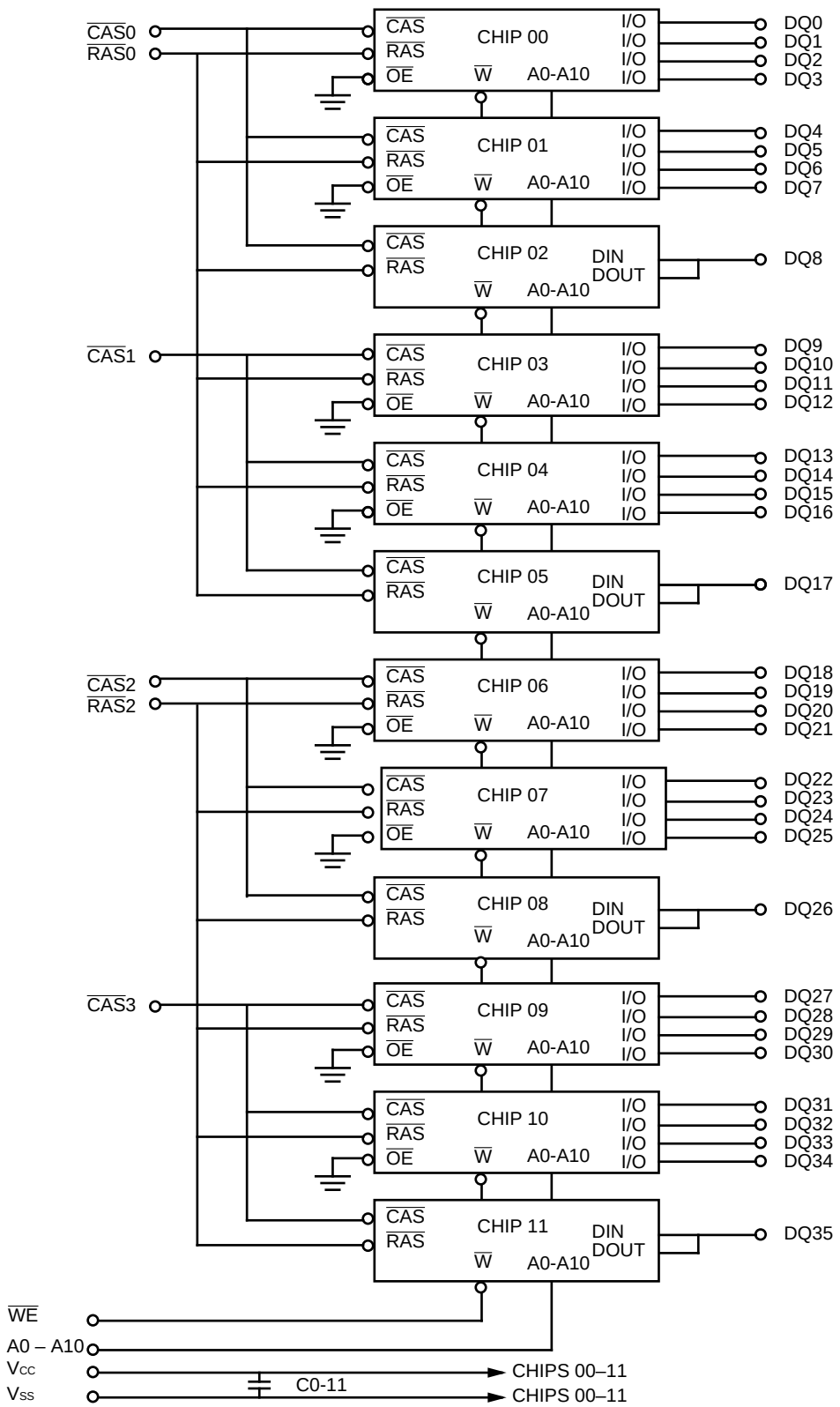
MSS-72P-P81

■ PIN ASSIGNMENT

DQ0	2	1	VSS
DQ1	4	3	DQ18
DQ2	6	5	DQ19
DQ3	8	7	DQ20
VCC	10	9	DQ21
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
DQ4	20	19	A10
DQ5	22	21	DQ22
DQ6	24	23	DQ23
DQ7	26	25	DQ24
A7	28	27	DQ25
VCC	30	29	NC
A9	32	31	A8
$\overline{RAS}$2	34	33	NC
DQ8	36	35	DQ26
DQ35	38	37	DQ17
$\overline{CAS}$0	40	39	VSS
$\overline{CAS}$3	42	41	$\overline{CAS}$2
$\overline{RAS}$0	44	43	$\overline{CAS}$1
NC	46	45	NC
NC	48	47	$\overline{WE}$
DQ27	50	49	DQ9
DQ28	52	51	DQ10
DQ29	54	53	DQ11
DQ30	56	55	DQ12
DQ31	58	57	DQ13
DQ32	60	59	VCC
DQ33	62	61	DQ14
DQ34	64	63	DQ15
NC	66	65	DQ16
PD2	68	67	PD1
PD4	70	69	PD3
VSS	72	71	NC

Pin #	Symbol	-60	-70
67	PD1	Vss	Vss
68	PD2	NC	NC
69	PD3	NC	Vss
70	PD4	NC	NC

FUNCTIONAL BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V
Input Low Voltage, all inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	25	70	°C

Note: *Undershoots of up to –2.0 volts with a pulse width not exceeding 10 ns are acceptable.

■ DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Test Condition	Min.	Max.	Unit
Output High Voltage*1		V_{OH}	I_{OH} = –5 mA	2.4	—	V
Output Low Voltage*1		V_{OL}	I_{OL} = 4.2 mA	—	0.4	V
Input Leakage Current	$\overline{RAS}$0 – $\overline{RAS}$2	$I_{I(L)}$	0 V ≤ V_{IN} ≤ 5.5 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, V_{SS} = 0 V, all other pins not under test = 0 V	–40	40	µA
	$\overline{CAS}$0 – $\overline{CAS}$3			–30	30	
	Address, $\overline{WE}$			–80	80	
Output Leakage Current		$I_{O(L)}$	0 V ≤ V_{OUT} ≤ 5.5 V, 4.5 V ≤ V_{CC} ≤ 5.5 V, Data out disabled	–20	20	µA
Operating Current*2 (Average power supply current)	MB85396A-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min.	—	1084	mA
	MB85396A-70			—	936	
Standby Current*2 (Power supply current)	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	24	mA
	CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC}–0.2 V	—	12	
Refresh Current #1*2 (Average power supply current)	MB85396A-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min.	—	1084	mA
	MB85396A-70			—	936	
Fast Page Mode Current*2	MB85396A-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{RC} = min.	—	724	mA
	MB85396A-70			—	668	
Refresh Current #2*2 (Average power supply current)	MB85396A-60	I_{CC5}	$\overline{RAS}$ = cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min.	—	1036	mA
	MB85396A-70			—	896	

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}, VIL > –0.3 V.
I_{CC1}, I_{CC3}, and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC4} is specified at one time of address change during one Page cycle.

■ AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85396A-60		MB85396A-70		Unit	Notes
			Min.	Max.	Min.	Max.		
1	Time Between Refresh	t_{REF}	—	32.8	—	32.8	ms	19
2	Random Read/Write Cycle Time	t_{RC}	110	—	130	—	ns	
3	Access Time from $\overline{RAS}$	t_{RAC}	—	60	—	70	ns	4, 7
4	Access Time from $\overline{CAS}$	t_{CAC}	—	15	—	20	ns	5, 7
5	Column Address Access Time	t_{AA}	—	30	—	35	ns	6, 7
6	Output Hold Time	t_{OH}	0	—	0	—	ns	
7	Output Buffer Turn On Delay Time	t_{ON}	0	—	0	—	ns	
8	Output Buffer Turn Off Delay Time	t_{OFF}	—	15	—	17	ns	8
9	Transition Time	t_T	3	50	3	50	ns	
10	$\overline{RAS}$ Precharge Time	t_{RP}	40	—	50	—	ns	
11	$\overline{RAS}$ Pulse Width	t_{RAS}	60	100000	70	100000	ns	
12	$\overline{RAS}$ Hold Time	t_{RSH}	15	—	20	—	ns	
13	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5	—	5	—	ns	
14	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	45	20	50	ns	9, 10
15	$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	ns	
16	$\overline{CAS}$ Hold Time	t_{CSH}	60	—	70	—	ns	
17	$\overline{CAS}$ Precharge Time (C-B-R Refresh)	t_{CPN}	10	—	10	—	ns	17
18	Row Address Setup Time	t_{ASR}	0	—	0	—	ns	
19	Row Address Hold Time	t_{RAH}	10	—	10	—	ns	
20	Column Address Setup Time	t_{ASC}	0	—	0	—	ns	
21	Column Address Hold Time	t_{CAH}	15	—	15	—	ns	
22	Column Address Hold Time from $\overline{RAS}$	t_{AR}	35	—	35	—	ns	
23	$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	11
24	Column Address to $\overline{RAS}$ Lead Time	t_{RAL}	30	—	35	—	ns	
25	Column Address to $\overline{CAS}$ Lead Time	t_{CAL}	30	—	35	—	ns	
26	Read Command Setup Time	t_{RCS}	0	—	0	—	ns	
27	Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	12
28	Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	ns	12
29	Write Command Setup Time	t_{WCS}	0	—	0	—	ns	13
30	Write Command Hold Time	t_{WCH}	15	—	15	—	ns	

(Continued)

■ AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Symbol	MB85396A-60		MB85396A-70		Unit	Notes
			Min.	Max.	Min.	Max.		
31	Write Command Hold Time from $\overline{RAS}$	t_{WCR}	35	—	35	—	ns	
32	$\overline{WE}$ Pulse Width	t_{WP}	15	—	15	—	ns	
33	Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15	—	18	—	ns	
34	Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15	—	18	—	ns	
35	DIN Setup Time	t_{DS}	0	—	0	—	ns	
36	DIN Hold Time	t_{DH}	15	—	15	—	ns	
37	Data Hold Time from $\overline{RAS}$	t_{DHR}	35	—	35	—	ns	
38	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)	t_{RPC}	5	—	5	—	ns	
39	$\overline{CAS}$ Setup Time (C-B-R Refresh)	t_{CSR}	0	—	0	—	ns	
40	$\overline{CAS}$ Hold Time (C-B-R Refresh)	t_{CHR}	10	—	12	—	ns	
41	$\overline{WE}$ Setup Time from $\overline{RAS}$	t_{WSR}	0	—	0	—	ns	18
42	$\overline{WE}$ Hold Time from $\overline{RAS}$	t_{WHR}	10	—	10	—	ns	18
43	DIN to $\overline{CAS}$ Delay Time	t_{DZC}	0	—	0	—	ns	15
44	Fast Page Mode $\overline{RAS}$ Pulse Width	t_{RASP}	—	100000	—	100000	ns	
45	Fast Page Mode Read/Write Cycle Time	t_{PC}	40	—	45	—	ns	
46	Access Time from $\overline{CAS}$ Precharge	t_{CPA}	—	35	—	40	ns	7, 16
47	Fast Page Mode $\overline{CAS}$ Precharge Time	t_{CP}	10	—	10	—	ns	
48	Fast Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35	—	40	—	ns	

Notes: 1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ =V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

2. AC characteristics assume t_T = 5 ns.
3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).
4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} exceeds the value shown.
5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.
6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.
7. Measured with a load equivalent to two TTL loads and 100 pF.
8. t_{OFF} and t_{OEZ} are specified that output buffer change to high impedance state.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
10. t_{RCD} (min) = t_{RAH} (min)+ 2 t_T + t_{ASC} (min).
11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.
12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.
14. Assumes that $t_{WCS} < t_{WCS}$ (min).
15. Either t_{DZC} or t_{DZO} must be satisfied.
16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} become long, t_{CPA} also become longer than t_{CPA} (max).
17. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
18. Assumes that test mode function.
19. t_{REF} is for distributed refresh (2,048 refresh cycles/32.8 ms).

*Source: See MB8117400A Data Sheet for details on the electricals.

■ CAPACITANCE

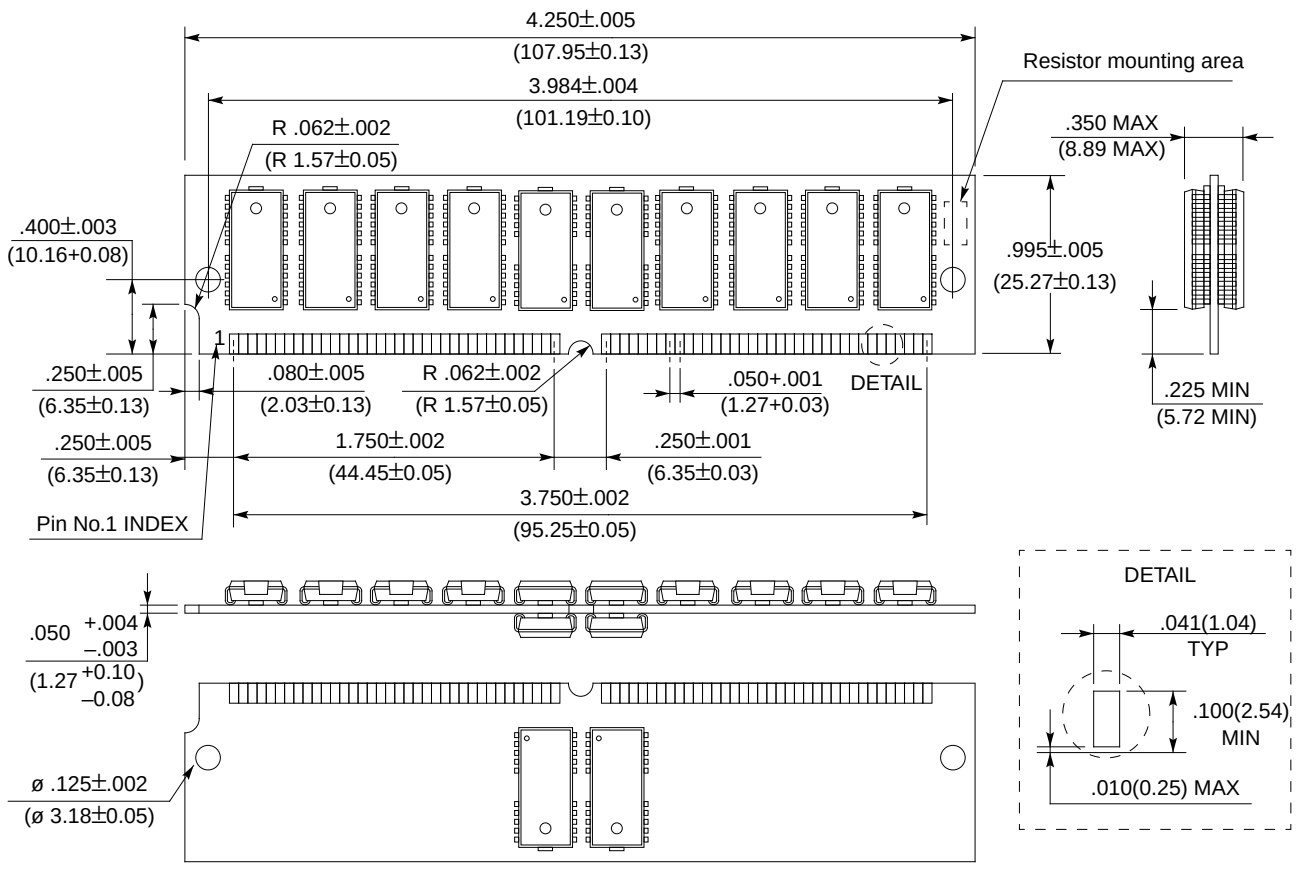
(T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Min.	Max.	Unit
Input Capacitance, A0 to A10	C_{IN1}	—	85	pF
Input Capacitance, $\overline{RAS}$0 and $\overline{RAS}$2	C_{IN2}	—	46	pF
Input Capacitance, $\overline{CAS}$0 to $\overline{CAS}$3	C_{IN3}	—	27	pF
Input Capacitance, $\overline{WE}$	C_{IN4}	—	83	pF
I/O Capacitance, (DQ0-7, DQ9-16, DQ18-25, DQ27-34)	C_{DQ1}	—	12	pF
I/O Capacitance, (DQ8, DQ17, DQ26, DQ35)	C_{DQ2}	—	13	pF

■ PACKAGE DIMENSIONS

(Suffix: PJPBK)

72-PAD PLASTIC SINGLE IN-LINE TYPE MODULE
(CASE No.: MSS-72P-P81)



Dimensions in inches (millimeters)

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