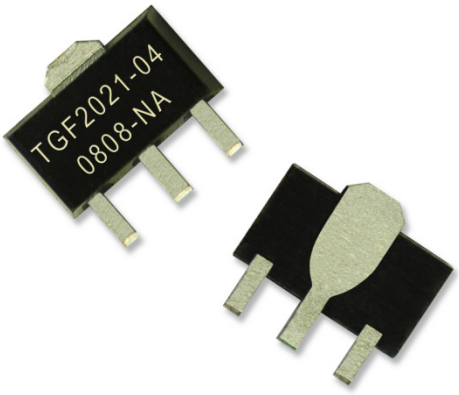
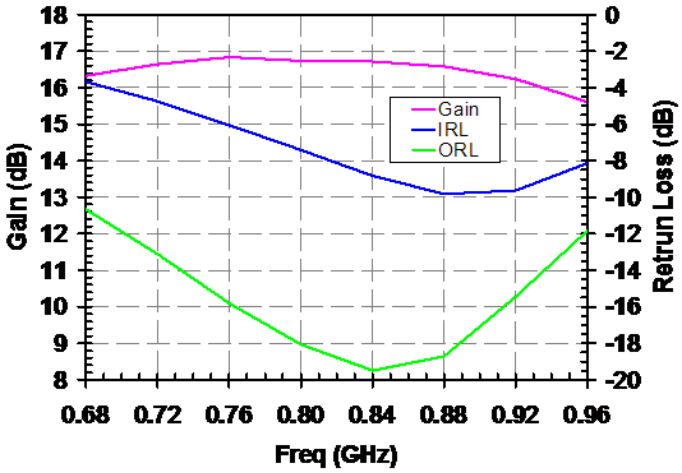
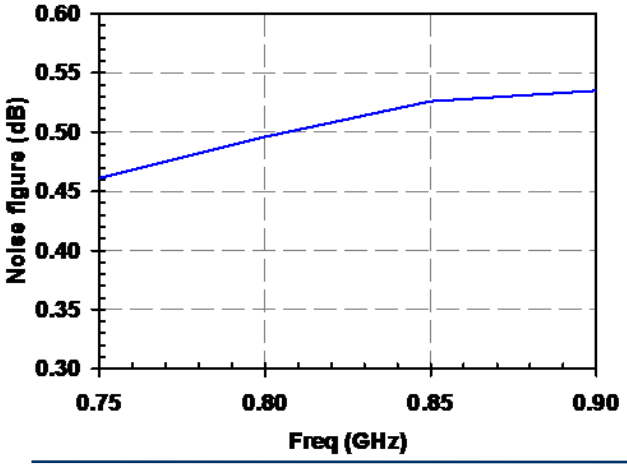
DC-4 GHz Packaged Power pHEMT



900 MHz Low Noise Application Board Performance

Bias conditions: Vd = 5 V, Idq = 150 mA, Vg = -0.8 V Typical





Key Features

- Frequency Range: DC-4 GHz
- Package Dimensions: 4.5 x 4 x 1.5 mm

Nominal 900 MHz Low Noise Application Board Performance:

- OTOI: 39.5 dBm
- Noise Figure: 0.6dB
- Gain: 16dB
- P1dB: 26dBm
- Input Return Loss: -8 dB
- Output Return Loss: -18 dB
- Bias: Vd = 5 V, Id = 150 mA, Vg = -0.8 V (Typical)

Primary Applications

- Cellular Base Stations
- WiMAX
- Wireless Infrastructure
- Low Noise Amplifiers

Product Description

The TGF2021-04-SD is a high performance pseudomorphic High Electron Mobility GaAs Transistor (pHEMT) housed in a low cost SOT89 surface mount package.

The device's ideal operating point for low noise operation is at a drain bias of 5 V and 150 mA. At this bias at 900 MHz when matched into 50 ohms using external components, this device is capable of 16 dB gain, 0.6dB noise figure, and 39.5 dBm output IP3.

The combination of high gain, low noise, and excellent linearity makes this an ideal component for use in a 3G or 4G receive chain.

Evaluation boards at 900 MHz are available.

RoHS and Lead-Free compliant

Datasheet subject to change without notice.

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Table I
Absolute Maximum Ratings 1/

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	15.0 V	
Vd	Drain Voltage	12.0 V	2/
Vg	Gate Voltage Range	-5 to 0 V	
Id	Drain Current	1800 mA	2/
|Ig|	Gate Current Range	28 mA	
Tch	Channel Temperature	200 °C	1/
Pin	Input Continuous Wave Power	31 dBm	2/

1/ These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

2/ Combinations of supply voltage, supply current, input power, and output power shall not exceed the maximum power dissipation listed in Table IV.

Table II
Recommended Low Noise Operating Conditions

Symbol	Parameter 1/	Typical Value
Vd	Drain Voltage	5 V
Idq	Drain Current	150 mA
Vg	Gate Voltage	-0.8 V

1/ See assembly diagram for bias instructions.

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Table III
RF Characterization Table

Bias: Vd = 5 V, Idq = 150 mA, Vg = -0.8 V, typical

SYMBOL	PARAMETER	TEST CONDITIONS	NOMINAL	UNITS	NOTES
Gain	Small Signal Gain	900 MHz	16	dB	1/
IRL	Input Return Loss	900 MHz	-8	dB	1/
ORL	Output Return Loss	900 MHz	-18	dB	1/
Psat	Saturated Output Power	900 MHz	27.3	dBm	1/
P1dB	Output Power @ 1dB Compression	900 MHz	26	dBm	1/
TOI	Output TOI	900 MHz	39.5	dBm	1/
NF	Noise Figure	900 MHz	0.6	dB	1/

1/ Using 900 MHz Application Board.

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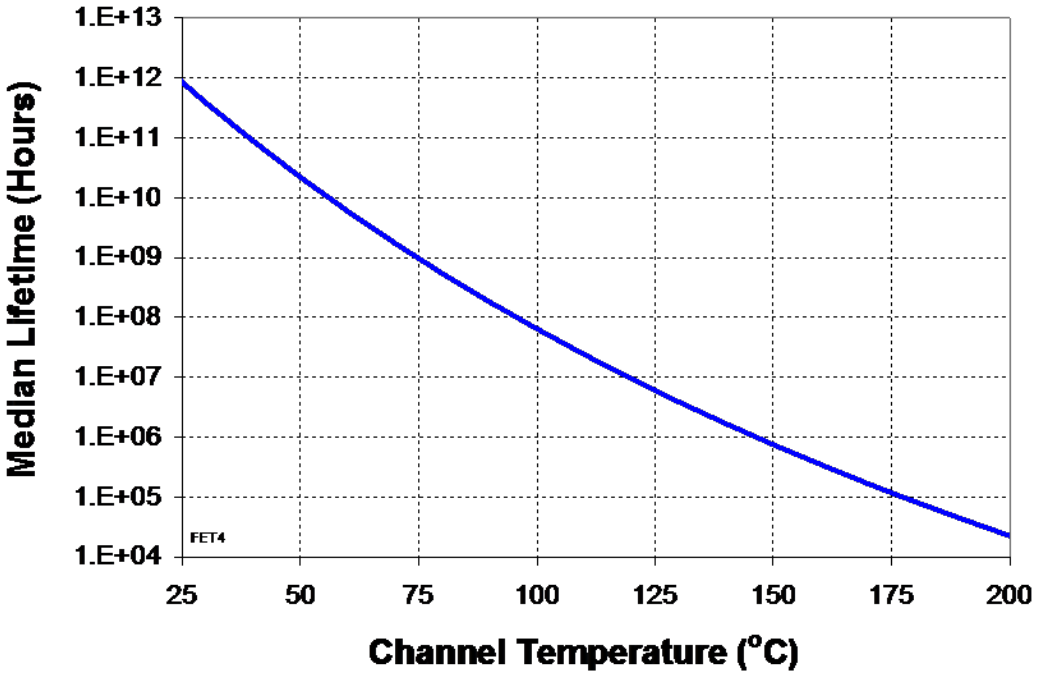
Table IV
Power Dissipation and Thermal Properties

THERMAL INFORMATION

Parameter	Test Conditions	T_{CH} (°C)	θ_{JC} (°C/W)	Tm (hrs)
θ_{JC} Thermal Resistance (Channel to Backside of Package)	V_D = 4.5 V I_D = 150 mA P_{DISS} = 0.675 W T_{BASE} = 85 °C	98	19	8E+07

Note: Heat transfer is conducted through the bottom of the TGF2021-04-SD package into the printed circuit board. Thermal resistance of board is application dependent and is not included above.

Median Lifetime (Tm) vs. Channel Temperature



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Device S-Parameters (device mounted as shown on Page 15)
Bias conditions Vd=5V, Ids=150mA, Vg=-0.8V typical

FREQ GHZ	MAG[S11]	ANG[S11]	MAG[S21]	ANG[S21]	MAG[S12]	ANG[S12]	MAG[S22]	ANG[S22]
0.2	0.932	-123.072	21.427	115.942	0.021	28.395	0.646	-162.037
0.3	0.923	-144	15.412	103.793	0.024	20.995	0.687	-168.797
0.4	0.925	-156.561	11.895	96.265	0.024	17.704	0.712	-173.53
0.5	0.919	-165.822	9.652	90.224	0.025	14.82	0.714	-177.448
0.6	0.921	-173.012	8.124	85.625	0.025	9.321	0.722	179.593
0.7	0.919	-178.888	6.922	81.155	0.027	7.333	0.724	177.605
0.8	0.917	176.252	6.152	76.901	0.026	7.538	0.723	175.297
0.9	0.917	171.831	5.473	74.167	0.027	5.507	0.729	173.971
1	0.91	167.67	4.914	71.157	0.026	5.744	0.728	171.727
1.1	0.913	164.057	4.492	67.99	0.027	2.806	0.729	169.556
1.2	0.91	159.687	4.141	64.777	0.027	3.81	0.731	167.568
1.3	0.911	156.568	3.772	61.779	0.027	2.984	0.729	166.375
1.4	0.911	153.572	3.559	58.565	0.027	1.561	0.728	164.845
1.5	0.909	150.565	3.298	55.316	0.027	1.23	0.731	163.193
1.6	0.909	147.435	3.09	52.976	0.029	1.256	0.73	162.211
1.7	0.908	144.315	2.925	50.204	0.028	-0.611	0.729	160.552
1.8	0.91	140.46	2.782	47.128	0.029	-0.344	0.726	159.282
1.9	0.909	138.172	2.636	44.653	0.029	-1.169	0.73	157.476
2	0.909	135.405	2.493	41.763	0.03	-2.66	0.724	155.587
2.1	0.914	132.151	2.382	39.061	0.03	-4.208	0.732	154.236
2.2	0.901	129.373	2.296	36.38	0.031	-4.136	0.728	152.488
2.3	0.907	126.779	2.208	34.013	0.03	-5.268	0.734	151.519
2.4	0.908	123.836	2.1	31.669	0.032	-6.796	0.729	149.732
2.5	0.904	120.979	2.031	27.603	0.031	-8.985	0.728	148.29
2.6	0.908	118.128	1.97	25.477	0.032	-8.646	0.724	146.869
2.7	0.902	115.242	1.878	23.232	0.033	-8.753	0.717	145.427
2.8	0.899	111.949	1.84	20.16	0.033	-10.664	0.718	144.608
2.9	0.905	109.87	1.772	17.535	0.034	-12.762	0.719	142.216
3	0.904	106.959	1.72	14.591	0.034	-13.733	0.724	140.595
3.1	0.903	104.385	1.657	11.908	0.034	-15.628	0.719	139.267
3.2	0.908	101.359	1.631	9.029	0.035	-16.881	0.727	137.618
3.3	0.903	98.561	1.567	6.636	0.035	-17.376	0.72	135.872
3.4	0.898	95.964	1.516	4.466	0.036	-19.167	0.723	134.591
3.5	0.901	93.255	1.48	1.046	0.036	-20.739	0.72	132.781
3.6	0.902	90.562	1.452	-0.991	0.037	-20.869	0.721	131.451
3.7	0.906	87.974	1.403	-3.95	0.037	-21.813	0.709	130.368
3.8	0.905	84.898	1.378	-6.245	0.038	-23.159	0.716	128.457
3.9	0.9	82.083	1.336	-9.121	0.039	-24.762	0.719	127.044
4	0.897	79.696	1.311	-11.46	0.039	-27.234	0.722	125.654
4.1	0.908	77.169	1.305	-14.814	0.039	-28.915	0.725	123.914
4.2	0.904	74.425	1.265	-16.441	0.039	-29.261	0.717	121.907
4.3	0.901	71.483	1.238	-20.308	0.04	-31.042	0.72	120.176
4.4	0.893	68.717	1.194	-22.153	0.04	-34.044	0.716	118.433
4.5	0.895	66.877	1.2	-25.013	0.041	-35.162	0.714	116.198
4.6	0.9	63.721	1.157	-27.589	0.041	-37.19	0.704	114.38
4.7	0.898	60.691	1.135	-30.031	0.04	-37.632	0.713	112.974
4.8	0.896	57.165	1.119	-32.131	0.041	-38.749	0.721	111.711
4.9	0.89	55.163	1.102	-34.891	0.042	-40.297	0.724	109.731
5	0.892	51.923	1.083	-38.623	0.042	-43.138	0.718	108.428

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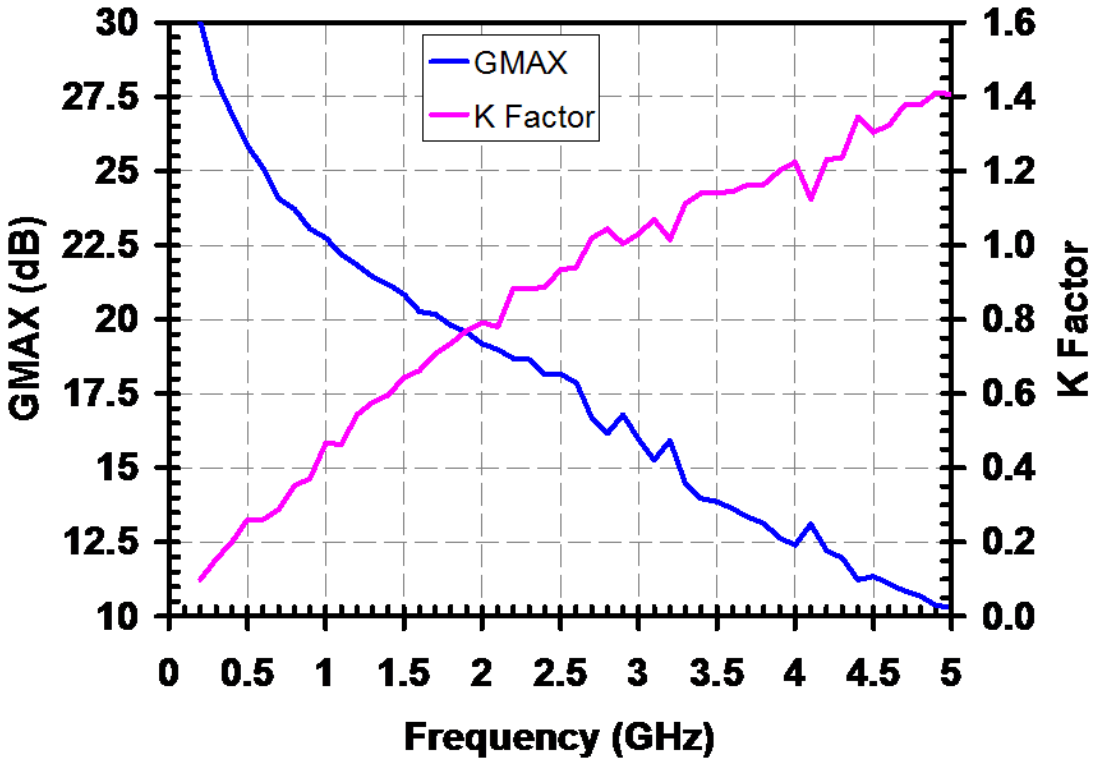
Gmax and K factor

Device mounted as shown on Page 15

Bias conditions: Vd = 5 V, Idq = 150 mA, Vg = -0.8 V Typical



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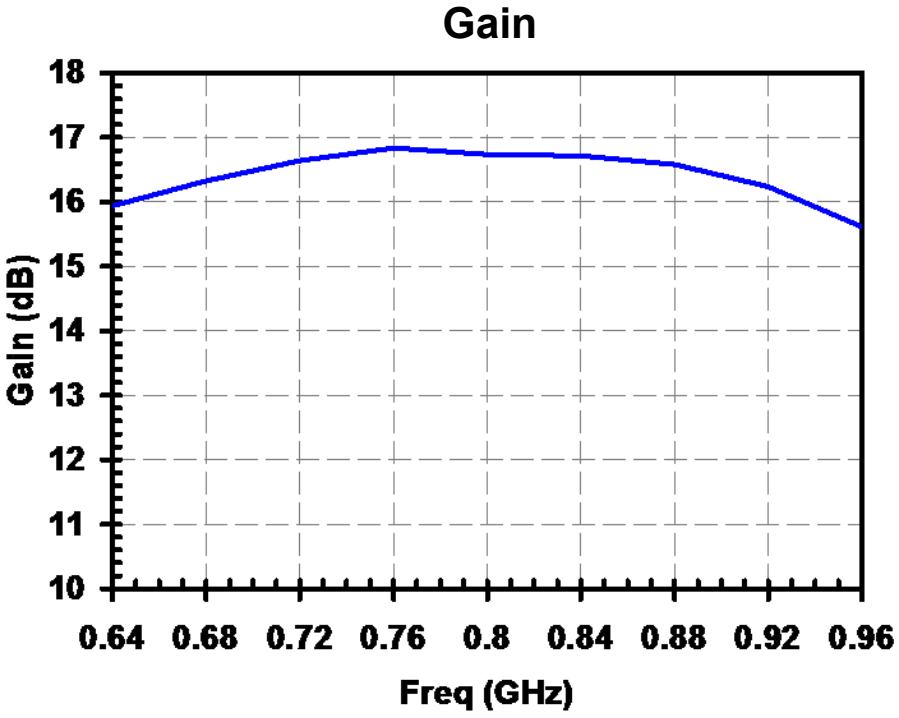
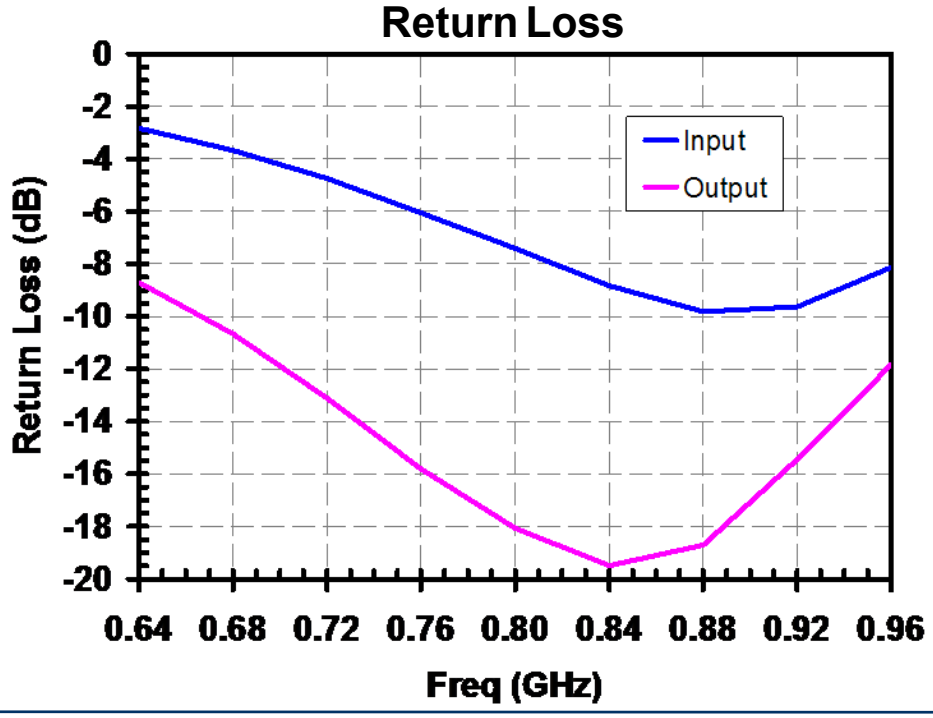
Measured Data 900 MHz Application Board

Bias conditions: Vd = 5 V, Id = 150 mA, Vg = -0.8 V Typical





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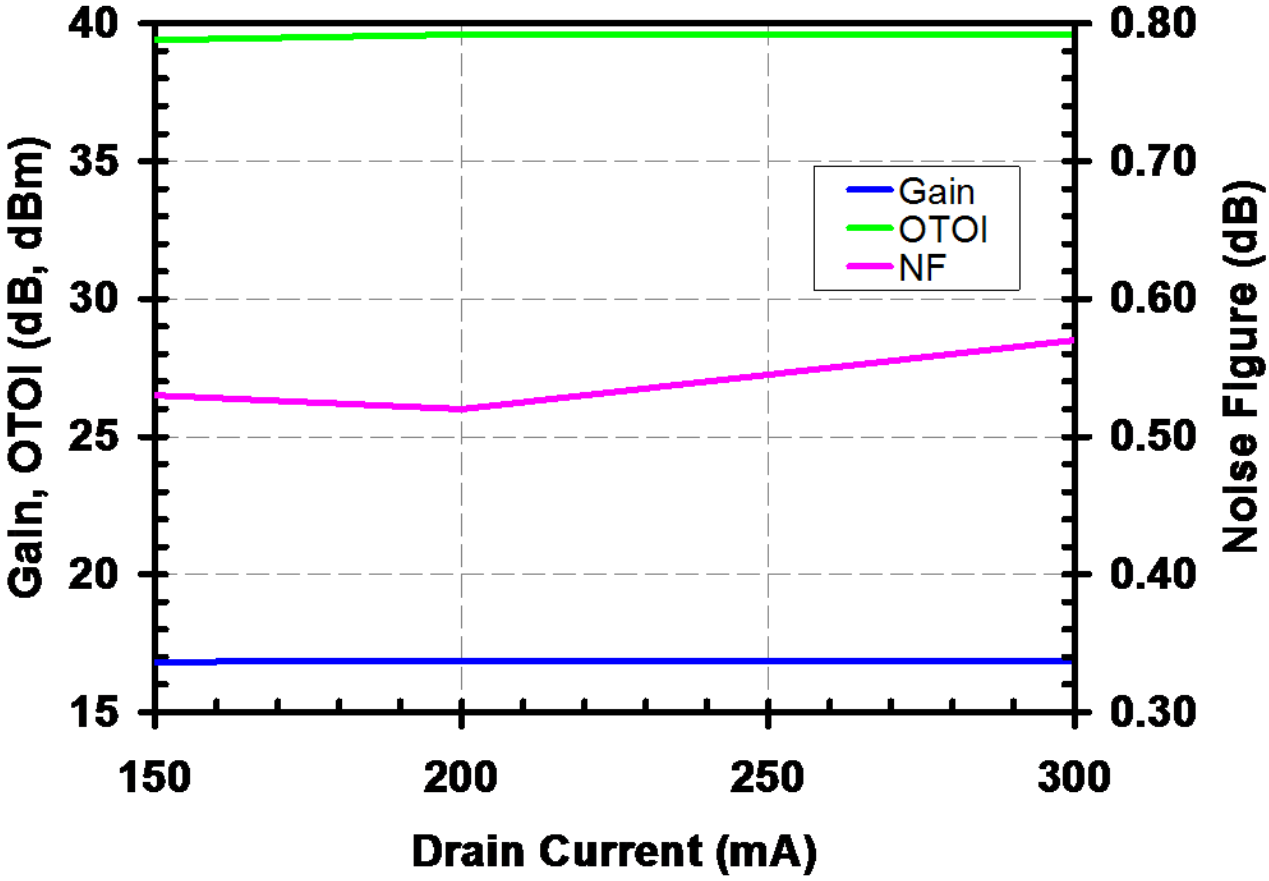
Measured Data, 900 MHz Application Board (at 850MHz)

Bias Conditions: V_{dd} = 5V

Gain, Noise Figure and OTOI vs. Ids



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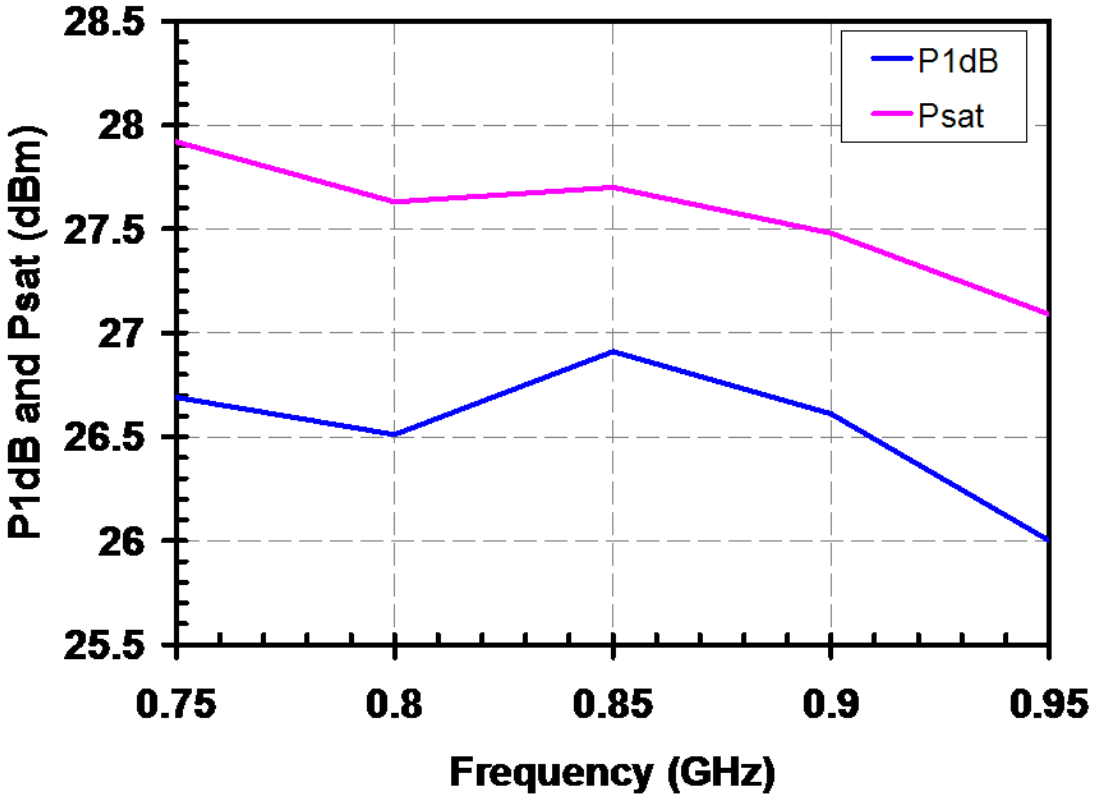
Measured Data 900 MHz Application Board

Bias conditions: Vd = 5 V, Idq = 150 mA, Vg = -0.8 V Typical

P1dB and Psat vs. Frequency



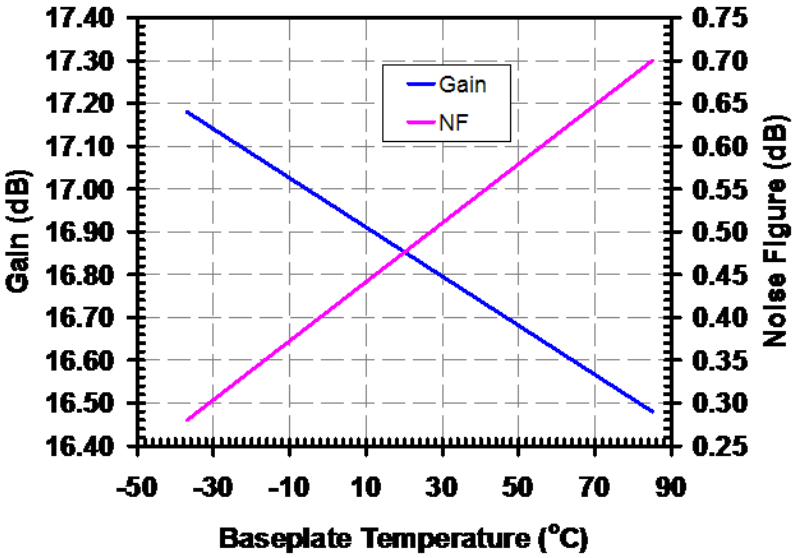
Measured Data 900 MHz Application Board

Bias conditions: Vd = 5 V, Idq = 150 mA

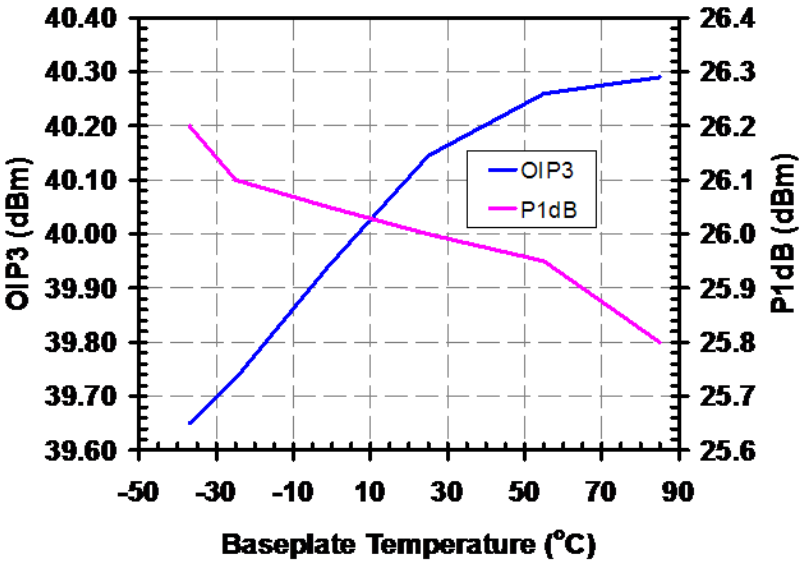
(measured at constant drain current using active bias circuit)

Device case temperature = 30°C above baseplate

Gain and noise figure vs. temperature (at 850MHz)



OIP3 and P1dB vs. temperature (at 850MHz)



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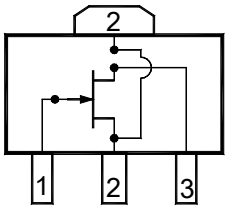
Electrical Schematic



Pin	Signal
1	RF In (Gate)
2	Gnd (Source)
3	RF Out (Drain)

Bias Procedures

Bias-up Procedure

- Vg set to -2.5 V
- Vd set to +5 V
- Adjust Vg more positive until Idq is 150 mA. This will be at approximately Vg = -0.8 V
- Apply RF signal to input

Bias-down Procedure

- Turn off RF signal at input
- Reduce Vg to -2.5V. Ensure Id ~ 0 mA
- Turn Vd to 0 V
- Turn Vg to 0 V

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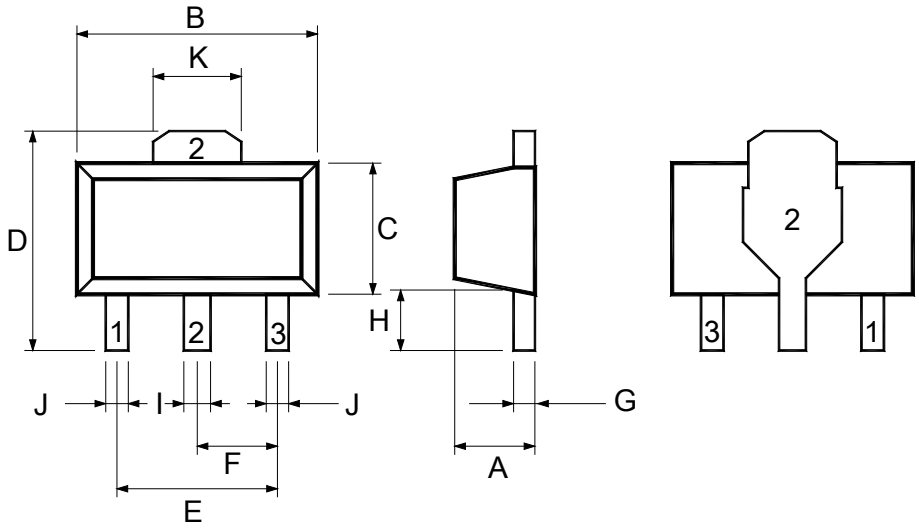
Mechanical Drawing



Dim	Millimeters	
	Min	Max
A	1.40	1.60
B	4.40	4.60
C	2.29	2.60
D	3.94	4.25
E	3.00 Center-Center	
F	1.50 Center-Center	
G	0.35	0.44
H	0.89	1.20
I	1.02	1.14
J	0.36	0.48
K	1.50	1.83

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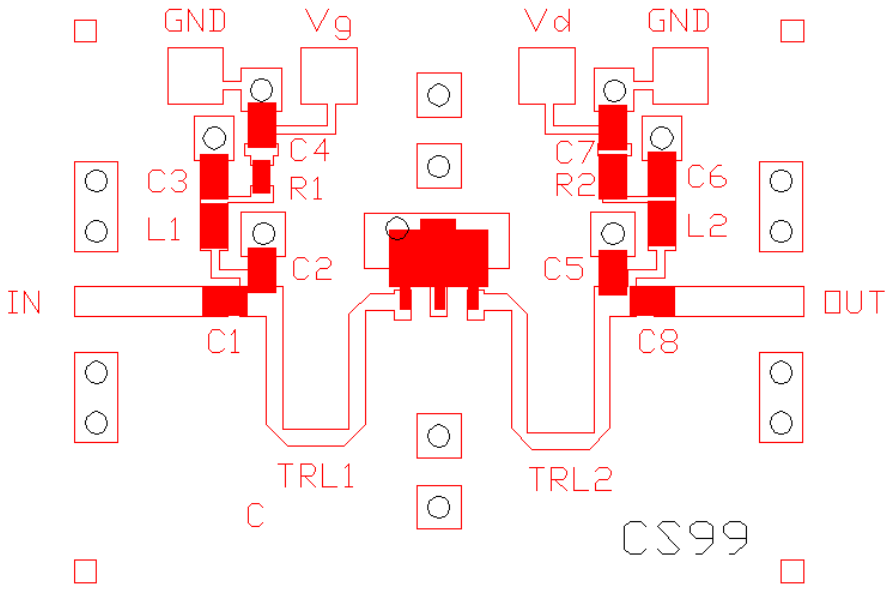
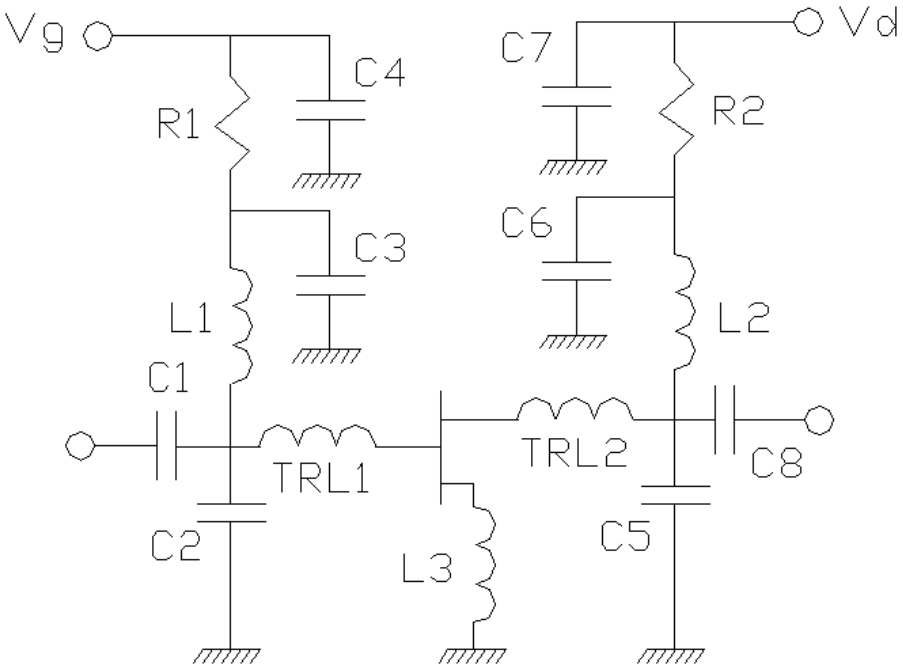
Evaluation Board Layout



Board dimensions: 33.0 x 25.4mm

Evaluation Board Schematic – 900 MHz



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Evaluation Board Bill of Materials

C1: 4.7pF 0805 AVX 08052U4R7CAT2A
C2: 2.7pF 0805 AVX 08052U2R7BAT2A
C3 27pF 0805 AVX 08052U270GAT2A
C4: 0.47uF 0805
C5: 3.3pF 0805 AVX 08052U3R3BAT2A
C6: 27pF 0805 AVX 08052U270GAT2A
C7: 1.0uF 0805
C8: 27pF 0805 AVX 08052U270GAT2A
R1: 47R 0603
R2: 3R3 0805
L1: 22nH 0805 AVX L0805220JESTR
L2: 22nH 0805 AVX L0805220JESTR
L3: ~0.5nH, realised on board with one source via
TRL1: transmission line: w=0.75mm, l=15.8mm
TRL2: transmission line: w=0.75mm, l=16.1mm
Board material – FR4, 0.79mm thick

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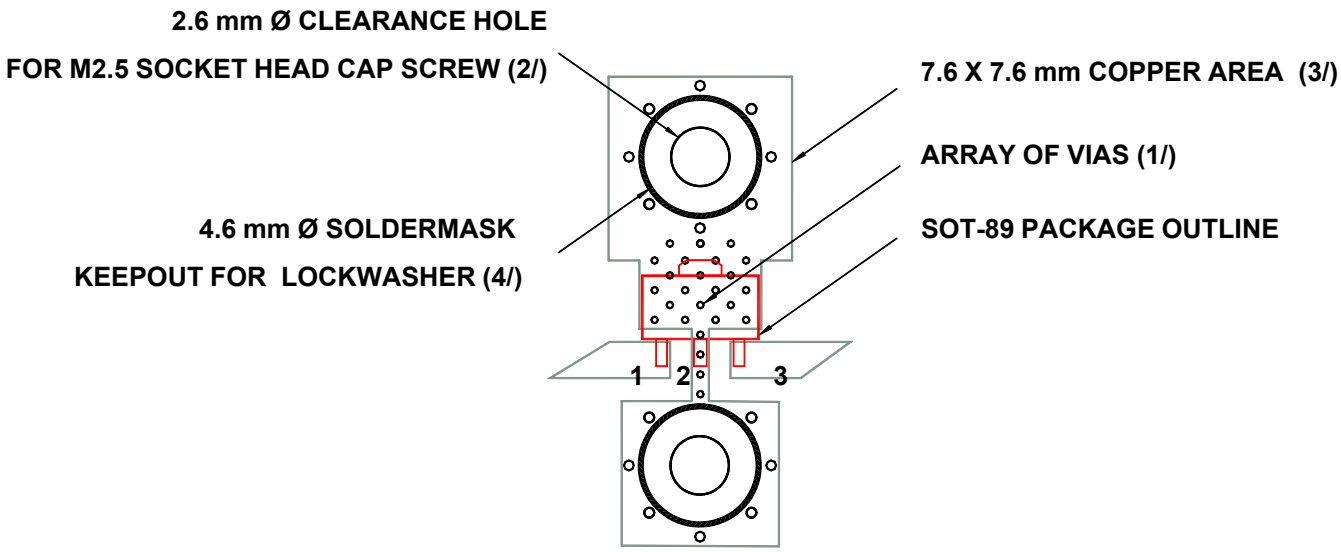
Recommended Assembly Diagram



Assembly Notes

1/ The lowest possible thermal and electrical resistance for Pin 2 is critical for optimal performance. The array of vias under Pin 2 should be as small and as dense as the PC board fabrication permits. 0.30 mm diameter vias on 0.60 mm center to center spacing is recommended.

2/ Mounting screws in the vicinity of the package improve heat transfer to the chassis or to a heat spreader located on the backside of the PC board. Shown are clearance holes and solder mask keepout zone for an M2.5 socket head cap screw. Use of a split lockwasher and proper torque on the screw will prevent compression damage to the PC board.

3/ Use of 1 oz copper (min) in the PC board construction is recommended.

4/ For lowest thermal resistance, solder mask must be removed where the copper traces on the PC board contact the heat spreader. In this example, this would be a) backside of the PC board and b) front of the PC board around package pin 2.

GaAs FET devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

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Recommended Surface Mount Package Assembly

Proper ESD precautions must be followed while handling packages.

Clean the board and rinse with alcohol. Allow the circuit to fully dry.

TriQuint recommends using solder paste for attachment. Follow solder paste and reflow oven vendors' recommendations when developing a solder reflow profile. Typical solder reflow profiles are listed in the table below.

Solder paste can be applied using a stencil printer or dot placement. The volume of solder paste depends on PCB and component layout and should be well controlled to ensure consistent mechanical and electrical performance.

Clean the assembly with alcohol after soldering.

Typical Solder Reflow Profiles

Reflow Profile	SnPb	Pb Free
Ramp-up Rate	3 °C/sec	3 °C/sec
Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C	60 – 180 sec @ 150 – 200 °C
Time above Melting Point	60 – 150 sec	60 – 150 sec
Max Peak Temperature	240 °C	260 °C
Time within 5 °C of Peak Temperature	10 – 20 sec	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec	4 – 6 °C/sec

Ordering Information

Part	Package Style
TGF2021-04-SD	SOT-89, BULK
TGF2021-04-SD-T/R	SOT-89, TAPE AND REEL

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