

**SWITCHING  
N-CHANNEL POWER MOS FET  
INDUSTRIAL USE**

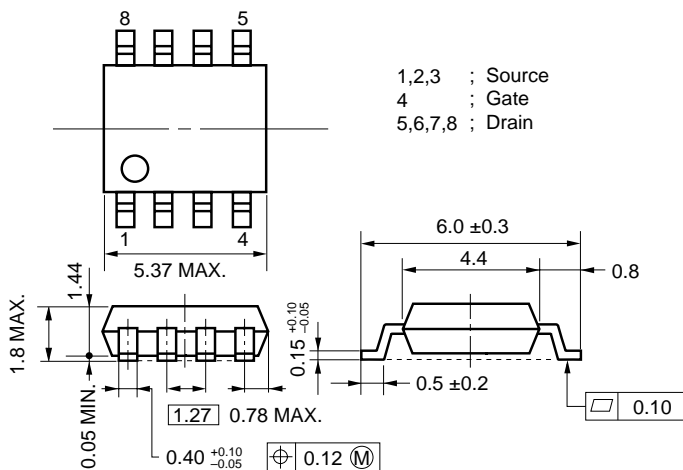
**DESCRIPTION**

The  $\mu$ PA1726 is N-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and so on.

**FEATURES**

- 2.5-V gate drive and low on-resistance  
 $R_{DS(on)1} = 9.1 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 6.0 \text{ A)}$   
 $R_{DS(on)2} = 10.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 6.0 \text{ A)}$   
 $R_{DS(on)3} = 12.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_D = 6.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 2700 \text{ pF TYP.}$
- Built-in G-S protection diodes
- Small and surface mount package (Power SOP8)

**PACKAGE DRAWING (Unit : mm)**



**ORDERING INFORMATION**

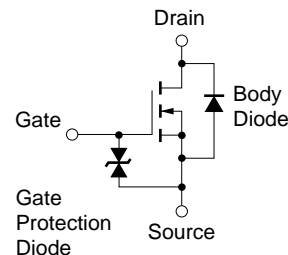
PART NUMBER	PACKAGE
$\mu$ PA1726G	Power SOP8

**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C, All terminals are connected.)**

Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	20	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±12	V
Drain Current (DC)	I <sub>D(DC)</sub>	±12	A
Drain Current (pulse) <sup>Note1</sup>	I <sub>D(pulse)</sub>	±48	A
Total Power Dissipation (T <sub>A</sub> = 25°C) <sup>Note2</sup>	P <sub>T</sub>	2.0	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C

- Notes**
1. PW ≤ 10 μs, Duty Cycle ≤ 1 %
  2. Mounted on ceramic substrate of 1200mm<sup>2</sup> x 2.2 mm

**EQUIVALENT CIRCUIT**



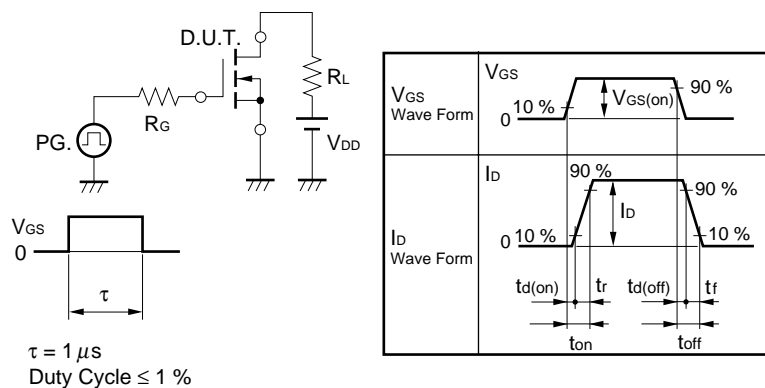
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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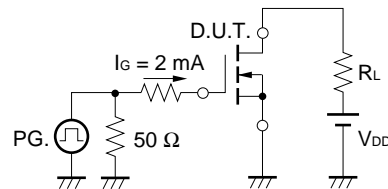
**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, All terminals are connected.)**

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R <sub>DS(on)1</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.0 A		7.2	9.1	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 6.0 A		7.5	10.0	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 6.0 A		9.1	12.5	mΩ
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA	0.5	1.0	1.5	V
Forward Transfer Admittance	y <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6.0 A	12	24		S
Drain Leakage Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V			10	μA
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V			±10	μA
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 10 V		2700		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		880		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		460		pF
Turn-on Delay Time	t <sub>d(on)</sub>	I <sub>D</sub> = 6.0 A		50		ns
Rise Time	t <sub>r</sub>	V <sub>GS(on)</sub> = 4.5 V		170		ns
Turn-off Delay Time	t <sub>d(off)</sub>	V <sub>DD</sub> = 10 V		100		ns
Fall Time	t <sub>f</sub>	R <sub>G</sub> = 10 Ω		190		ns
Total Gate Charge	Q <sub>G</sub>	I <sub>D</sub> = 12 A		25		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>DD</sub> = 16 V		4		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 4.5 V		11		nC
Body Diode Forward Voltage	V <sub>F(S-D)</sub>	I <sub>F</sub> = 12 A, V <sub>GS</sub> = 0 V		0.8		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 12 A, V <sub>GS</sub> = 0 V		50		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 100 A/ μs		50		nC

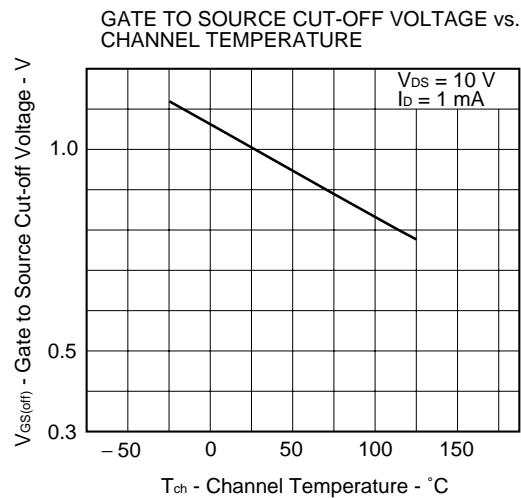
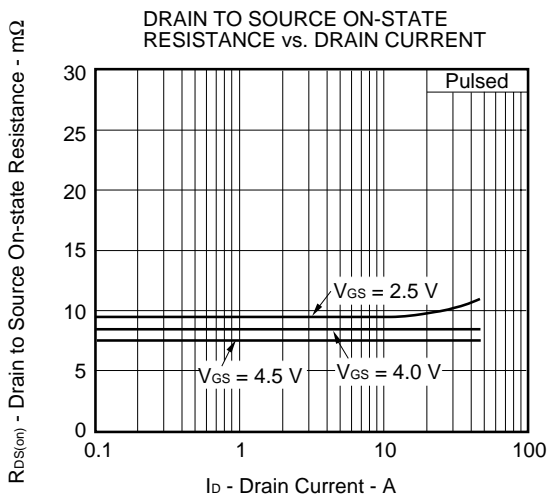
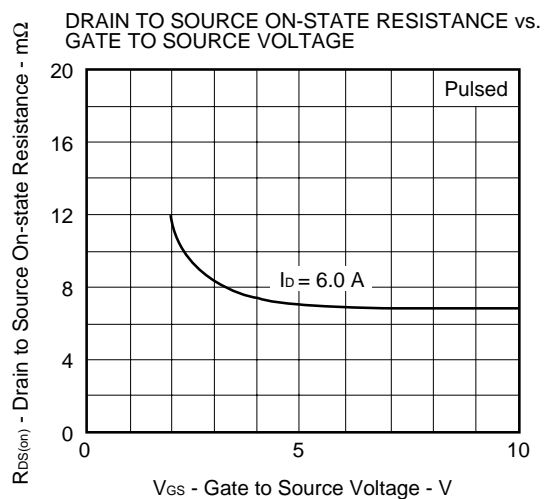
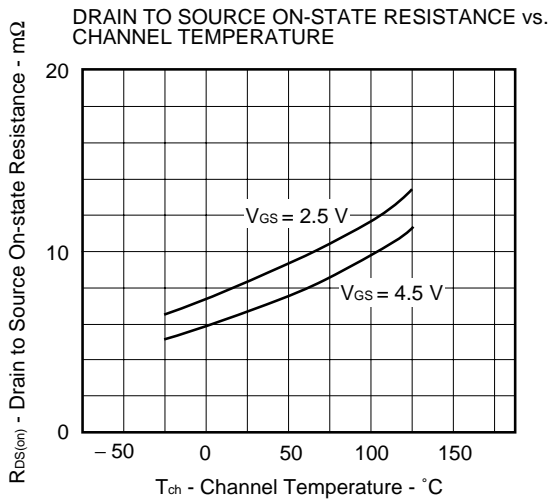
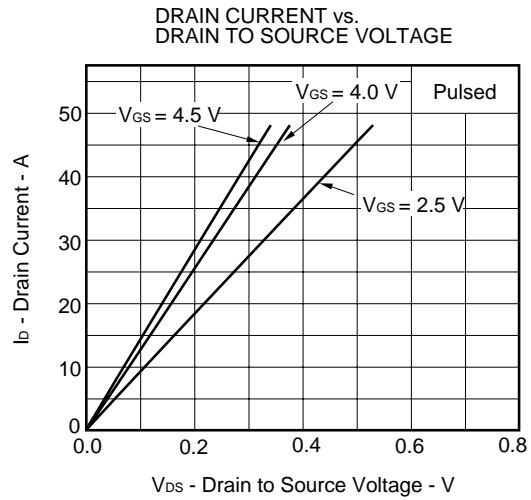
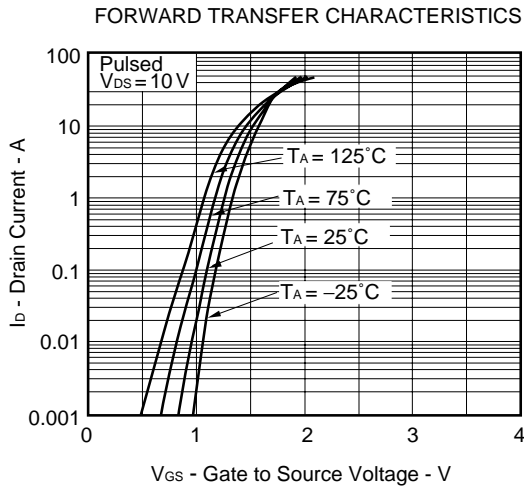
**TEST CIRCUIT 1 SWITCHING TIME**

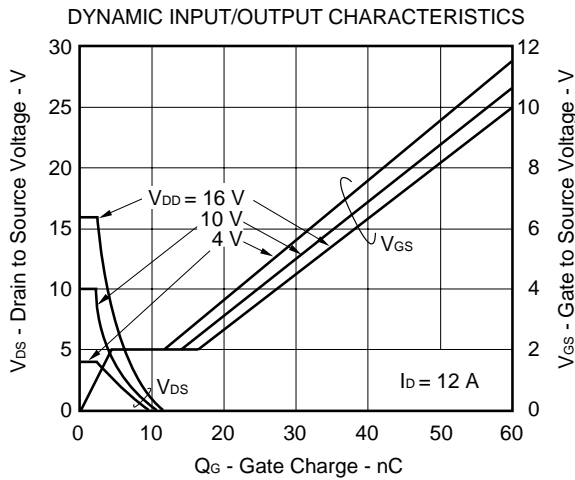
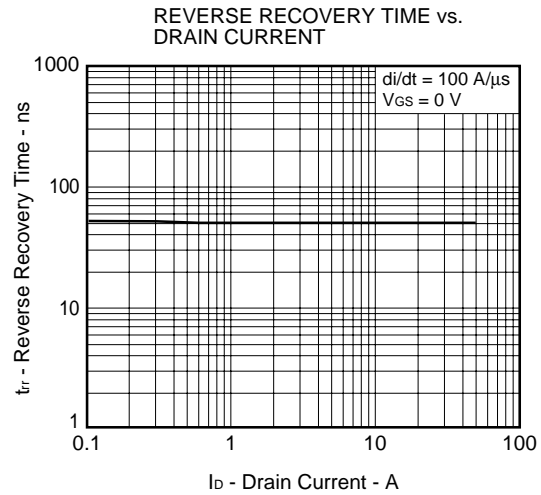
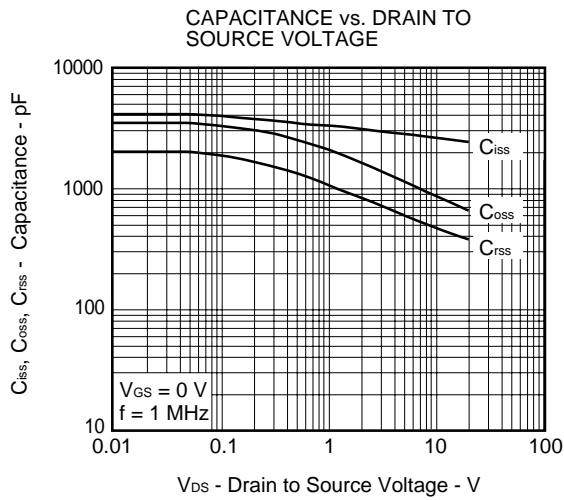
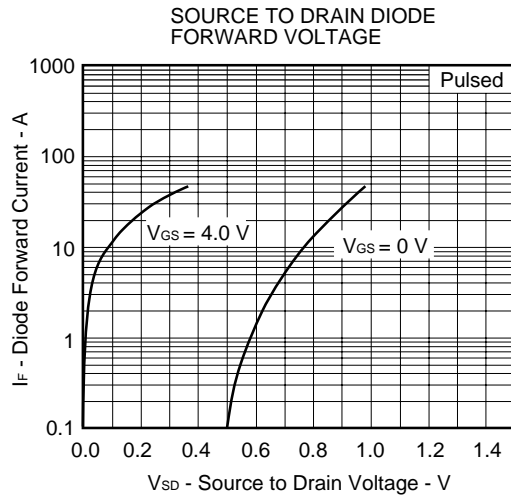
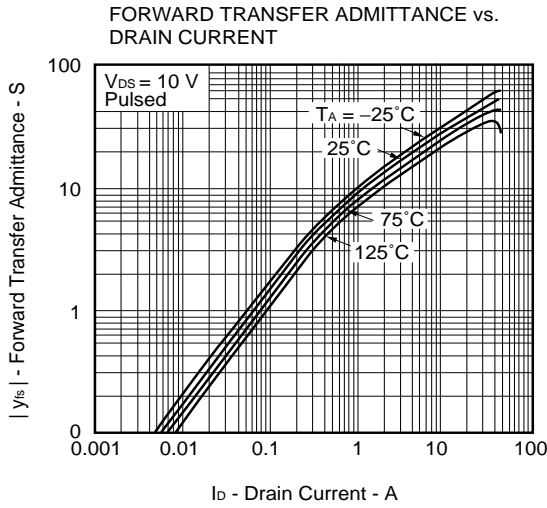


**TEST CIRCUIT 2 GATE CHARGE**

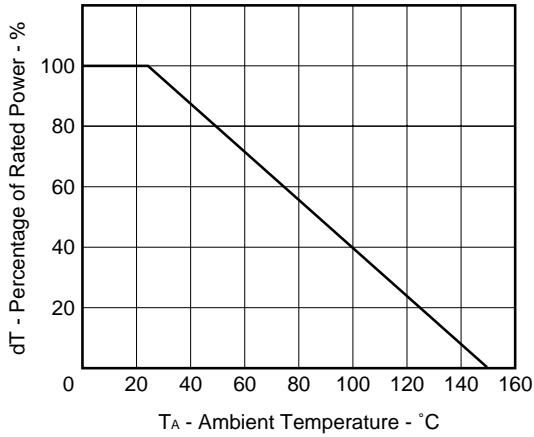


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

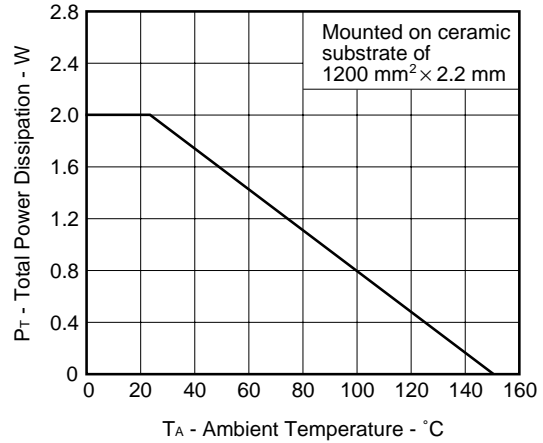




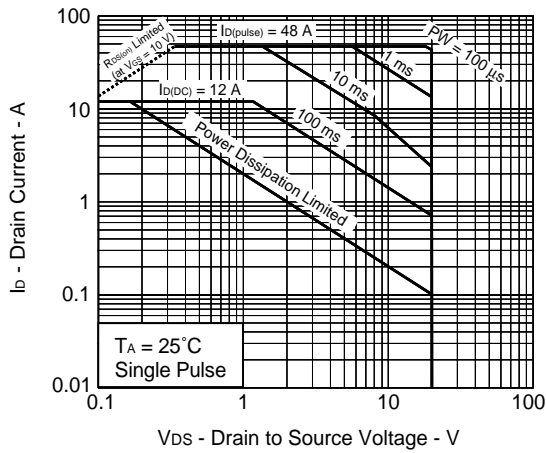
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



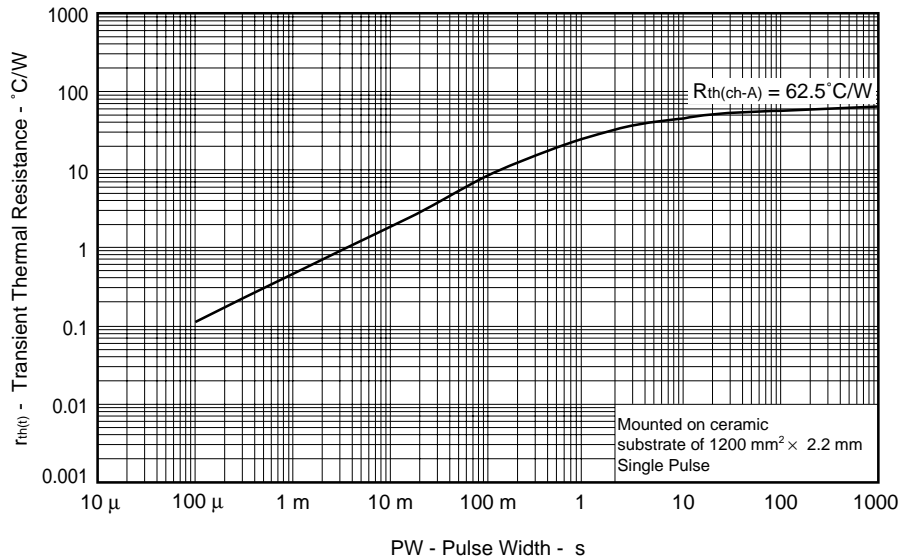
★ FORWARD BIAS SAFE OPERATING AREA



**Remark**

Mounted on ceramic substrate of 1200 mm<sup>2</sup> × 2.2 mm

TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



[MEMO]

[MEMO]

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