



## SY89297U

2.5/3.3V, 3.2Gbps Precision CML  
Dual-Channel Programmable Delay

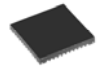
### General Description

The SY89297U is a DC-3.2Gbps programmable, two-channel delay line. Each channel has a delay range from 2ns to 7ns (5ns delta delay) in programmable increments as small as 5ps. The delay step is extremely linear and monotonic over the entire programming range, with 15ps INL over temperature and voltage.

The delay varies in discrete steps based on a serial control word provided by the 3-pin serial control (SDATA, SCLK, and SLOAD). The control word for each channel is 10-bits. Both channels are programmed through a common serial interface. For increased delay, multiple SY89297U delay lines can be cascaded together.

The SY89297U provides two independent 3.2Gbps delay lines in an ultra-small 4mm x 4mm, 24-pin QFN package. For other delay line solutions, consider the SY89295U and SY89296U single-channel delay lines. Evaluation boards are available for all these parts.

Datasheets and support documentation can be found on Micrel's web site at: [www.micrel.com](http://www.micrel.com).



Precision Edge®

### Features

- Dual-channel, programmable delay line
- Serial programming interface (SDATA, SCLK, SLOAD)
- Guaranteed AC performance over temperature and voltage:
  - > 3.2Gbps/1.6GHz  $f_{MAX}$
- Programming Accuracy:
  - Linearity: -15ps to +15ps INL
  - Monotonic: -5ps to +25ps
  - Resolution: 5ps programming increments
- Low-jitter design: 1ps<sub>RMS</sub> typical random jitter
- Programmable delay range: 5ns delay range
- Cascade capability for increased delay
- Flexible voltage operation:
  - $V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$
- Industrial temperature range: -40°C to +85°C
- Available in 24-pin (4mm x 4mm) QFN

### Applications

- Clock de-skewing
- Timing adjustments
- Aperture centering
- System calibration

### Markets

- Automated test equipment
- Digital radio and video broadcasting
- Closed caption encoders/decoders
- Test and measurement

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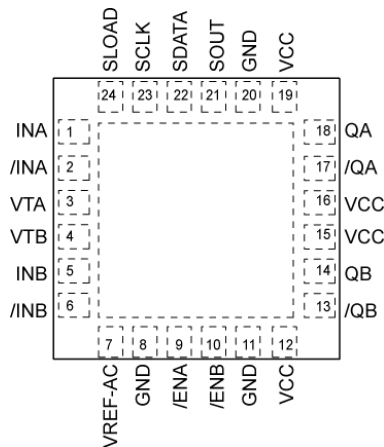
## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY89297UMG	QFN-24	Industrial	297U with Pb-Free Bar Line Indicator	Pb-Free NiPdAu
SY89297UMGTR <sup>(2)</sup>	QFN-24	Industrial	297U with Pb-Free Bar-Line Indicator	Pb-Free NiPdAu

**Notes:**

- Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
- Tape and Reel.

## Pin Configuration



24-Pin QFN

## Truth Tables

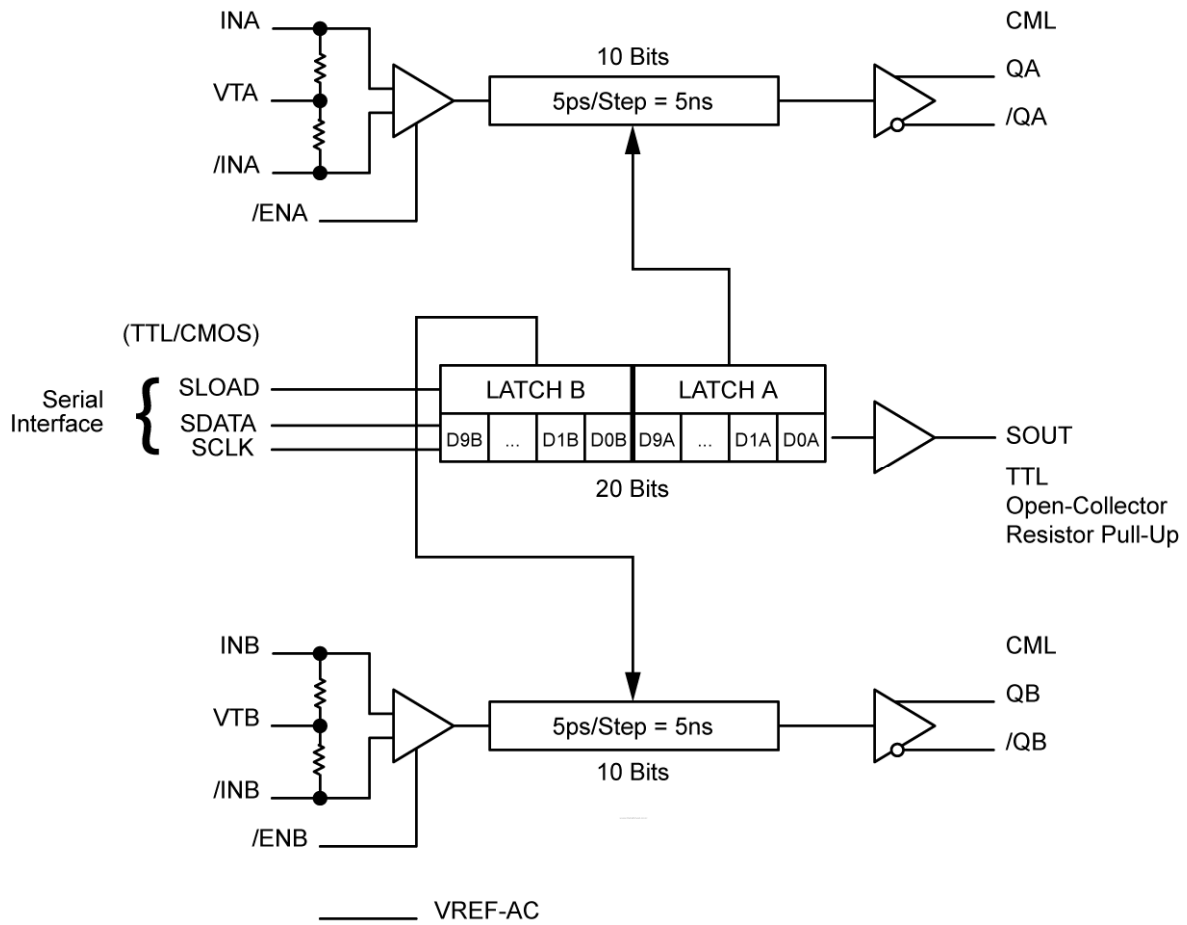
Inputs		Outputs	
INA, INB	/INA, /INB	QA, QB	/QA, /QB
0	1	0	1
1	0	1	0

Table 1. Inputs/Outputs

/ENA, /ENB	Q, /Q (A, B)
1	Q = Low, /Q = HIGH
0	IN, /IN Delayed (normal operation)

Table 2. Input Enable (Latches Outputs)

### Functional Block Diagram



## Pin Description

Pin Number	Pin Name	Pin Function
1 2	INA /INA	Channel A Differential Input: INA and /INA pins receive the Channel A data. QA and /QA are the delayed product of INA and /INA. Each input is internally terminated to VTA through a 50Ω resistor (100Ω across INA and /INA).
3	VTA	Input A Termination Center-Tap: Each side of the differential input pair terminates to this pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section.
4	VTB	Input B Termination Center-Tap: Each side of the differential input pair terminates to this pin. This pin provides a center-tap to a termination network for maximum interface flexibility. See "Input Interface Applications" section.
5 6	INB /INB	Channel B Differential Input: INB and /INB pins receive the Channel B data. QB and /QB are the delayed product of INB and /INB. Each input is internally terminated to VTB through a 50Ω resistor (100Ω across INB and /INB).
7	VREF-AC	Reference Voltage Output: For AC-coupled input signals, this pin can bias the inputs IN and /IN. Connect VREF-AC directly to the VT input pin for each channel. De-couple to V <sub>CC</sub> using a 0.01μF capacitor. Maximum sink/source current is ±0.5mA. For DC-coupled input applications, leave VREF-AC pin floating.
8, 11, 20	GND, Exposed Pad	Negative Supply: Exposed pad must be connected to a ground plane that is the same potential as the ground pins.
9	/ENA	CMOS/TTL-Compatible Enable Input: When the /ENA pin is pulled HIGH, QA is held LOW and /QA goes HIGH after the programmed delay propagates through the part. /ENA contains a 67kΩ pull-down resistor and defaults LOW when left floating. Logic threshold level is V <sub>CC</sub> /2
10	/ENB	CMOS/TTL-Compatible Enable Input: When the /ENB pin is pulled HIGH, QB is held LOW and /QB goes HIGH after the programmed delay propagates through the part. /ENB contains a 67kΩ pull-down resistor and defaults LOW when left floating. Logic threshold level is V <sub>CC</sub> /2
12, 15, 16, 19	VCC	Power Supply: Bypass each supply pin with 0.1μF/0.01μF low-ESR capacitors. See DC Electrical Characteristics table for more details. 2.5V ±5% or 3.3V ±10%.
13 14	/QB QB	CML Differential Output: QB and /QB are the delayed product of INB, /INB. CML outputs are terminated at the destination with 100Ω across the pair. See "CML Output Termination" section.
17 18	/QA QA	CML Differential Output: QA and /QA are the delayed product of INA, /INA. CML outputs are terminated at the destination with 100Ω across the pair. See "CML Output Termination" section.
23 22	SCLK SDATA	CMOS/TTL-compatible 3-pin serial programming control inputs: The 3-pin serial control sets each channel's IN to Q delay. DA(0:9) control channel A delay. DB(0:9) control channel B. To program the two channels, insert a 20-bit word (DA0:DA9 and DB0:DB9) into SDATA and clock in the control bits with SCLK. Maximum input frequency to SCLK is 40MHz. Data is loaded into the serial registers on the L-H transition of SCLK. After all 20-bits are clocked in, SLOAD latches the new delay bits. These pins have internal pull-downs at the inputs. See "AC Electrical Characteristics" for delay values. Logic threshold level is V <sub>CC</sub> /2. SCLK and SDATA contain a 67kΩ pull-down resistor and default LOW when left floating.
24	SLOAD	CMOS/TTL-compatible 3-pin serial programming control input: SLOAD controls the latches that transfer scanned data to the delay line. These latches are transparent when SLOAD is high. Data transfers from the latch to the delay line on a L-H transition of SLOAD. SLOAD has to transition H-L before new data is loaded in the scan chain. When SLOAD is high, the latches are transparent and SCLK cannot switch. Otherwise, new data will immediately transfer to the scan chain. Logic threshold level is V <sub>CC</sub> /2. SLOAD contains a 67kΩ pull-down resistor and defaults LOW when left floating.
21	SOUT	CMOS/TTL-compatible output: This pin is used to support cascading multiple SY89297U delay lines. Serial data is clocked into the SDATA input and is clocked out of SOUT into the next SY89297U delay line. SOUT pin includes an internal 550Ω pull-up resistor.

### Absolute Maximum Ratings<sup>(1)</sup>

Supply Voltage ( $V_{CC}$ ) ..... -0.5V to +4.0V  
 Input Voltage ( $V_{IN}$ ) ..... -0.5V to  $V_{CC}$   
 CML Output Voltage ( $V_{OUT}$ ) .....  $V_{CC} - 1.0V$  to  $V_{CC} + 0.5V$   
 Current ( $V_T$ )  
     Source or Sink Current on VT pin .....  $\pm 70mA$   
 Input Current  
     Source or Sink Current on (IN, /IN) .....  $\pm 35mA$   
 Current ( $V_{REF}$ )  
     Source or sink current on  $V_{REF-AC}$ <sup>(2)</sup> .....  $\pm 0.5mA$   
 Maximum operating Junction Temperature ..... 125°C  
 Lead Temperature (soldering, 20sec.) ..... 260°C  
 Storage Temperature ( $T_s$ ) ..... -65°C to +150°C

### Operating Ratings<sup>(3)</sup>

Supply Voltage ( $V_{CC}$ )  
      $T_A$  (-40°C to +85°C) ..... +2.375V to +2.625V  
      $T_A$  (-40°C to +75°C) ..... +3.0V to 3.6V  
 Ambient Temperature ( $T_A$ ) ..... -40°C to +85°C  
 Package Thermal Resistance<sup>(4)</sup>  
 QFN ( $\theta_{JA}$ )  
     Still-Air ..... 43°C/W  
 QFN ( $\psi_{JB}$ )  
     Junction-to-Board ..... 30.5°C/W

### DC Electrical Characteristics<sup>(5)</sup>

$T_A = -40^\circ C$  to  $+85^\circ C$ , Channels A and B, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{CC}$	Power Supply Voltage Range	$T_A: -40^\circ C$ to $+85^\circ C$	2.375	2.5	2.625	V
		$T_A: -40^\circ C$ to $+75^\circ C$	3.0	3.3	3.6	V
		$T_A: -40^\circ C$ to $+85^\circ C$ , Airflow = 500 LFPM	3.0	3.3	3.6	V
$I_{CC}$	Power Supply Current	Maximum $V_{CC}$ , Both Channels Combined, Output Load Included		195	250	mA
$R_{IN}$	Input Resistance (IN-to-VT, /IN-to-VT)		45	50	55	$\Omega$
$R_{DIFF\_IN}$	Differential Input Resistance (IN-to-/IN)		90	100	110	$\Omega$
$V_{IH}$	Input HIGH Voltage (IN, /IN)		1.2		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage (IN, /IN)		0		$V_{IH} - 0.1$	V
$V_{IN}$	Input Voltage Swing (IN, /IN)	See Figure 5a	0.1		1.0	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing ( $ IN - /IN $ )	See Figure 5b	0.2			V
$V_{REF-AC}$	Output Reference Voltage		$V_{CC} - 1.3$	$V_{CC} - 1.2$	$V_{CC} - 1.1$	V
$V_{T\_IN}$	Voltage from Input to $V_T$				1.28	V

**Notes:**

1. Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to "Absolute Maximum Rating" conditions for extended periods may affect device reliability.
2. Due to the limited drive capability, use for input of the same package only.
3. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
4. Thermal performance on QFN packages assumes exposed pad is soldered (or equivalent) to the device most negative potential (GND).
5. The circuit is designed to meet the DC specifications shown in the table after thermal equilibrium has been established.

## CML Outputs DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = +2.5V \pm 5\%$  or  $+3.3V \pm 10\%$ ,  $R_L = 100\Omega$  across the outputs;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{OH}$	Output HIGH Voltage	$R_L = 50\Omega$ to $V_{CC}$	$V_{CC}-0.020$	$V_{CC}-0.010$	$V_{CC}$	V
$V_{OUT}$	Output Voltage Swing	See Figure 5a	325	400		mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	See Figure 5b	650	800		mV
$R_{OUT}$	Output Source Impedance		45	50	55	$\Omega$

## LVTTL/CMOS DC Electrical Characteristics<sup>(6)</sup>

$V_{CC} = +2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V
$I_{IH}$	Input HIGH Current	$V_{IH} = V_{CC}$			150	$\mu A$
$I_{IL}$	Input LOW Current	$V_{IL} = 0.8V$			50	$\mu A$
$V_{OL}$	Output LOW Voltage	SOUT Pin; $I_{OL}=1mA$			0.55	V
	Output High Leakage Current	SOUT = $V_{CC}$			100	$\mu A$

### Note:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

## AC Electrical Characteristics<sup>(7)</sup>

$T_A = -40^\circ C$  to  $+85^\circ C$ , Channels A and B, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{MAX}$	Maximum Operating Frequency	Clock: $V_{out}$ Swing $\geq 200mV_{pk}$	1.6			GHz
		NRZ Data	3.2			Gbps
$t_{pd}$	Propagation Delay	IN to Q; D[0-9]=0 IN to Q; D[0-9]=1023 /EN to Q; D[0-9]=0; $V_{TH} = V_{CC}/2$ SDATA to SOUT (D0-D9=Low), No load	1000 5500 1000 2000		2000 7500 2500 4500	ps
$t_{RANGE}$	Programmable Range $t_{pd} (max) - t_{pd} (min)$		4150	5115		ps
$t_{SKEW}$	Duty Cycle Skew $t_{PHL} - t_{PLH}$	Note 8	45		55	%

## AC Electrical Characteristics<sup>(7)</sup>

T<sub>A</sub> = -40°C to +85°C, Channels A and B, unless otherwise stated.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Δt	Step Delay					
		D0 High D1 High D2 High D3 High D4 High D5 High D6 High D7 High D8 High D9 High D0-D9 High		5 10 20 40 80 160 320 640 1280 2560 5115		ps
	Monotonic		-5		25	
INL	Integral Non-Linearity	Note 9	-15		+15	ps
t <sub>S</sub>	Setup Time					
		SDATA to SCLK SCLK to SLOAD	Note 10	400 400		ps
		/EN to IN	Note 11	300		
t <sub>H</sub>	Hold Time					
		SLOAD to SCLK IN to /EN	Note 12 Note 13	300 -100		ps
		SCLK to SDATA		200		
t <sub>PW</sub>	Pulse Width	SLOAD	1000			ps
t <sub>R</sub>	Release Time	/EN to IN	800			ps
t <sub>JITTER</sub>	Cycle-to-Cycle Jitter	Note 15			2	ps <sub>RMS</sub>
	Total Jitter	Note 16			20	ps <sub>PP</sub>
	Random Jitter	Note 17			2	ps <sub>RMS</sub>
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Time	20% to 80% (Q)	30	55	80	ps
	Duty Cycle	Input Frequency = 1.6GHz	45		55	%

### Notes:

- High frequency AC electricals are guaranteed by design and characterization.
- Duty cycle skew guaranteed only for differential operation measured from the cross point of the input to the crosspoint of the output.
- INL (Integral Non-Linearity) is defined from its corresponding point on the ideal delay versus D[9:0] curve as the deviation from its ideal delay. The maximum difference is the INL. Theoretical Ideal Linearity (TIL) = (measured maximum delay - measured minimum delay) ÷ 1023. INL = measured delay - (measured minimum delay + (step number x TIL)).
- SCLK has to transition L-H a setup time before the SLOAD H-L transition to ensure the valid data is properly latched. See timing diagram "Setup and Hold Time: SCLK and SLOAD."
- This setup time is the minimum time that /EN must be asserted prior to the next transition of IN //IN to prevent an output response greater than ±75 mV to that IN or /IN transition. See timing diagram Setup, Hold and Release Time: IN and /EN."
- SCLK has to transition L-H a hold time after the SLOAD H-L transition to ensure that the valid data is properly latched before starting to load new data. See timing diagram "Setup and Hold Time: SCLK and SLOAD."
- This hold time is the minimum time that /EN must remain asserted after a negative going transition of IN to prevent an output response greater than ±75mv to the IN transition. See timing diagram "Setup, Hold, and Release Time: IN and /EN."
- This release time is the minimum time that /EN must be de-asserted prior to the next IN //IN transition to affect the propagation delay of IN to Q less than 1ps. See timing diagram "Setup, Hold, and Release Time: IN and /EN."
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles over a random sample of adjacent cycle pairs.  
T<sub>jitter\_cc</sub> = T<sub>n</sub> - T<sub>n+1</sub>, where T is the time between rising edges of the output signal.
- Total jitter definition: With an ideal clock input, no more than one output edge in 10<sup>12</sup> output edges will deviate by more than the specified peak-to-peak jitter value.
- Random jitter definition: Jitter that is characterized by a Gaussian distribution, unbounded and is quantified by its standard deviation and mean. Random jitter is measured with a K28.7 comma defect pattern, measured at 1.5Gbps.

## Timing Diagrams

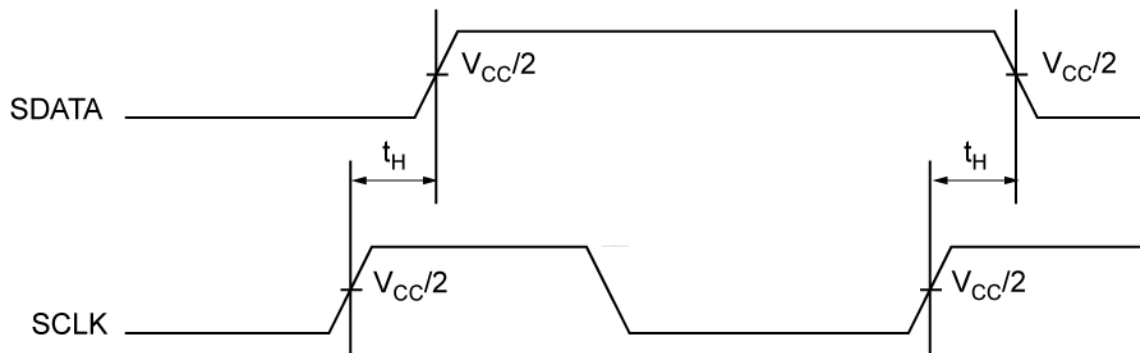
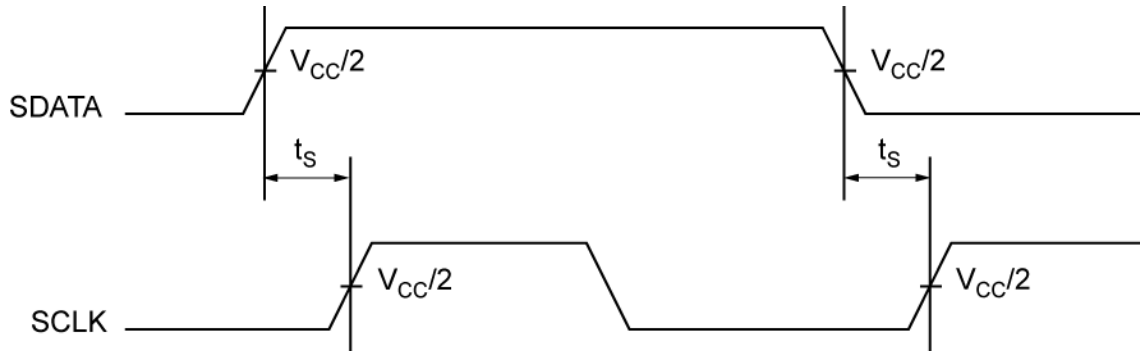


Figure 1. Setup and Hold Time: SDATA and SCLK

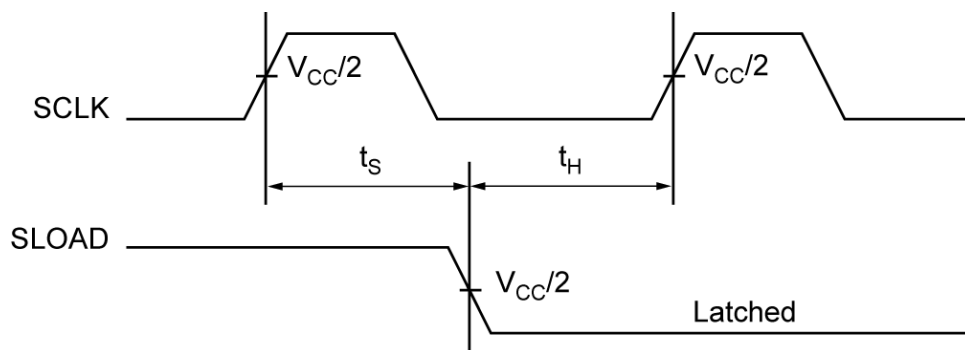
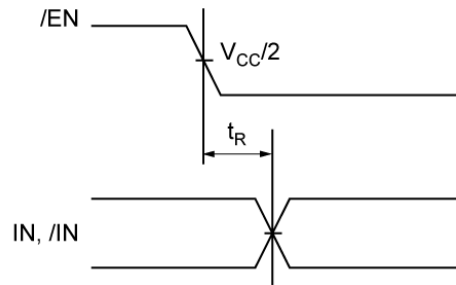
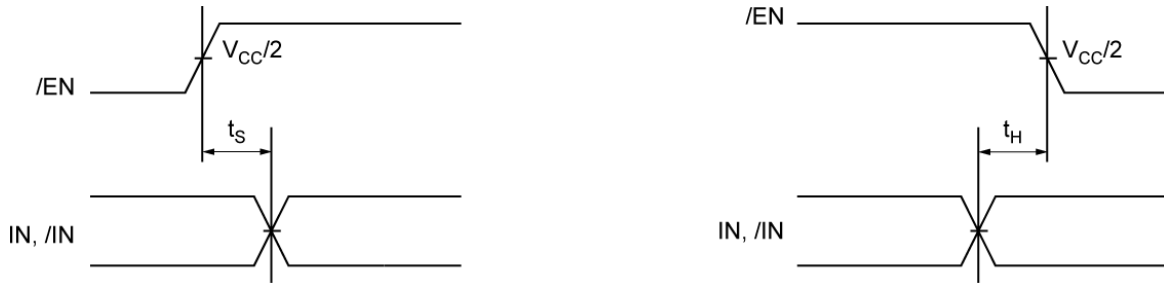


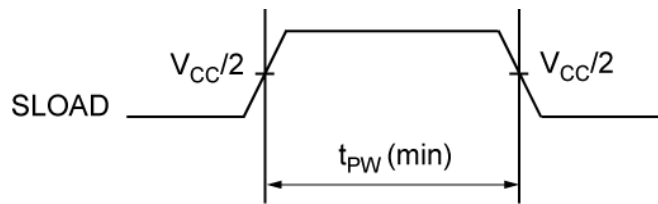
Figure 2. Setup and Hold Time: SCLK and SLOAD



**Timing Diagrams (Continued)**



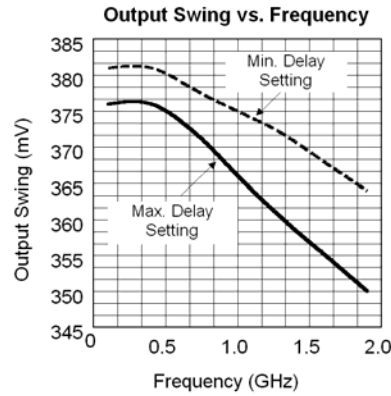
**Figure 3. Set-Up, Hold, and Release Time: IN and /EN**



**Figure 4. SLOAD Pulse Width (TPW)**

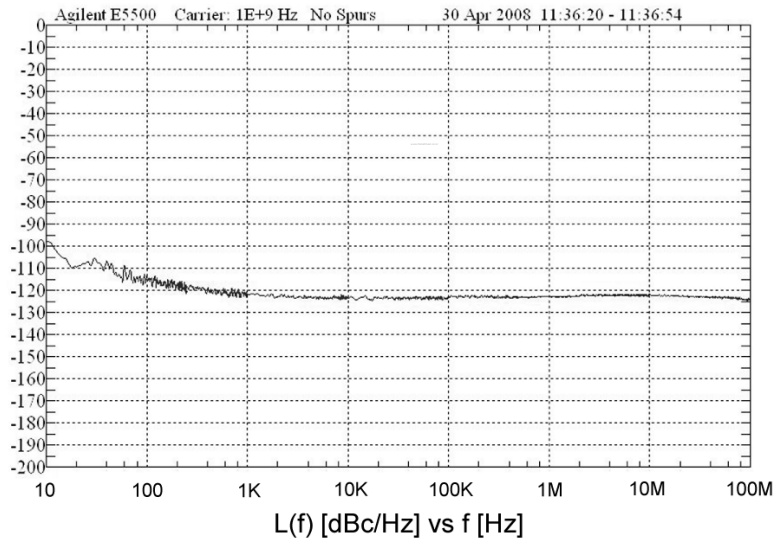
### Typical Operating Characteristics

$V_{CC} = +2.5V$ ,  $GND = 0V$ ,  $V_{IN} = 100mV$ ,  $R_L = 100\Omega$  across the outputs,  $T_A = 25^\circ C$ .



### Phase Noise Chart

$V_{CC} = +2.5V$ ,  $GND = 0V$ ,  $V_{IN} = 100mV$ ,  $R_L = 100\Omega$  across the outputs,  $T_A = 25^\circ C$ .

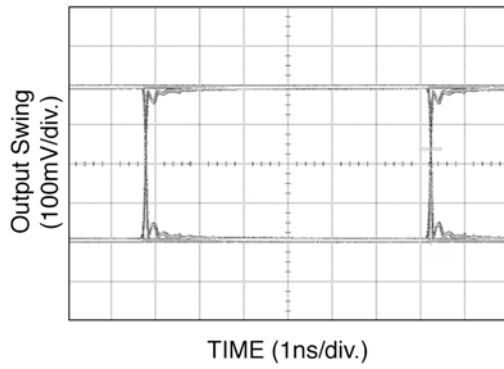


**f<sub>c</sub>: 1GHz Delay Setting: 00001 00110 (2ns)**

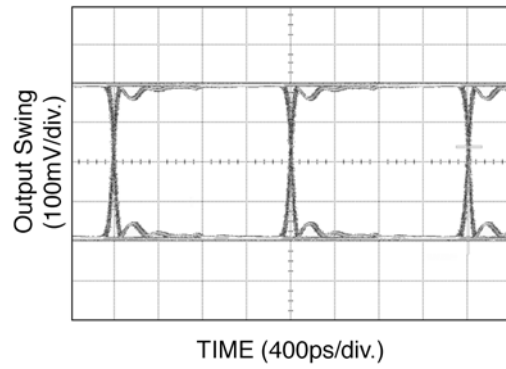
### Functional Operating Characteristics

$V_{CC} = 2.5V$  or  $3.3V$ ,  $GND = 0V$ ,  $V_{IN} = 100mV$ ,  $R_L = 100\Omega$  across the outputs,  $T_A = 25^\circ C$ , Maximum Delay (D0–D9 = High).

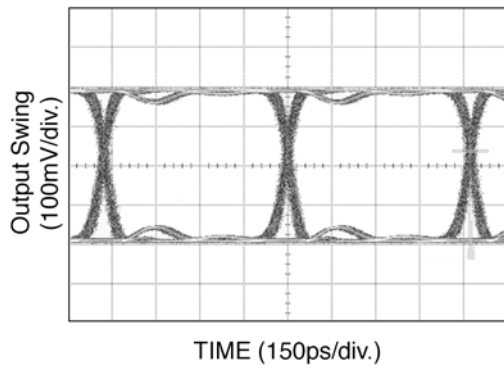
**155Mbps Clock**



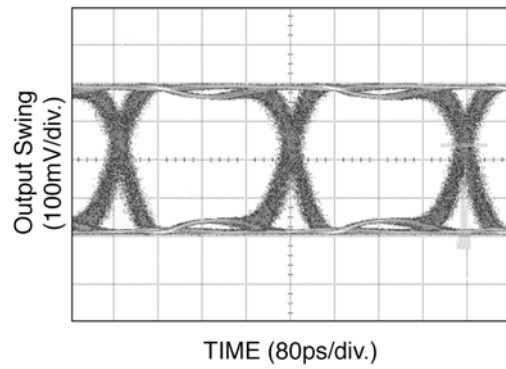
**622Mbps Clock**



**1.6Gbps Clock**



**3.2Gbps Clock**



## Single-Ended and Differential Swings

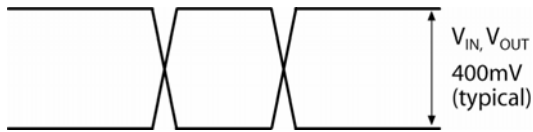


Figure 5a. Single-Ended Voltage Swing

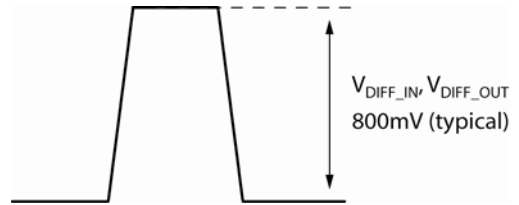


Figure 5b. Differential Voltage Swing

## Input and Output Stages

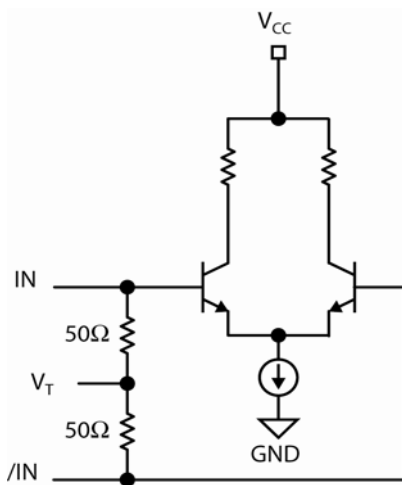


Figure 6. Input Stage

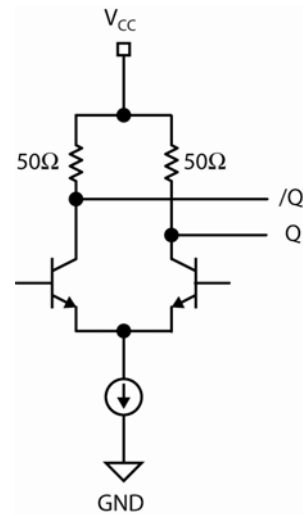
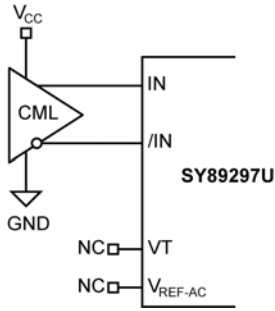


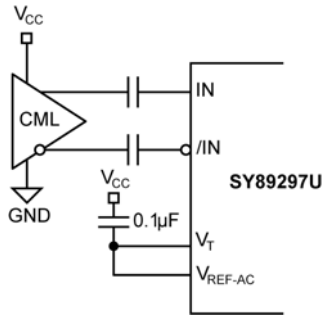
Figure 7. CML Output Stage

# Input Interface Applications

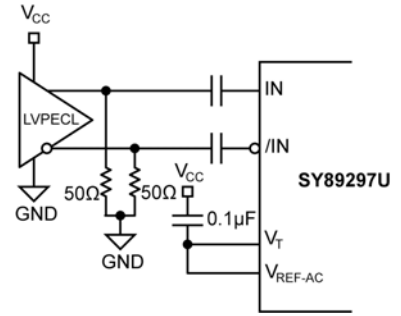


Option: May connect  $V_T$  to  $V_{CC}$

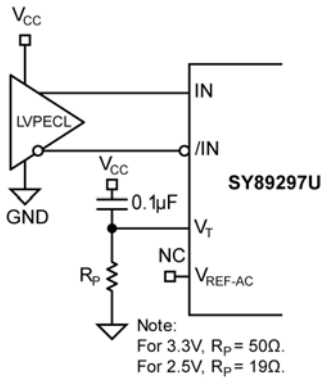
**Figure 8a. CML Interface (DC-Coupled)**



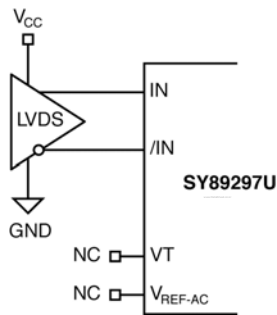
**Figure 8b. CML Interface (AC-Coupled)**



**Figure 8c. LVPECL Interface (AC-Coupled)**

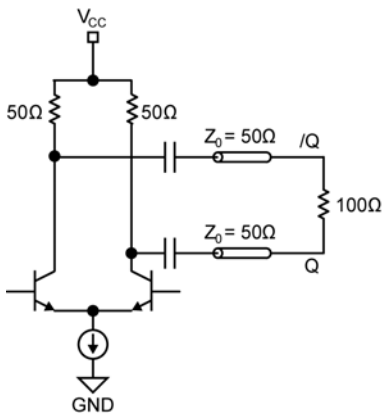


**Figure 8d. LVPECL Interface (DC-Coupled)**

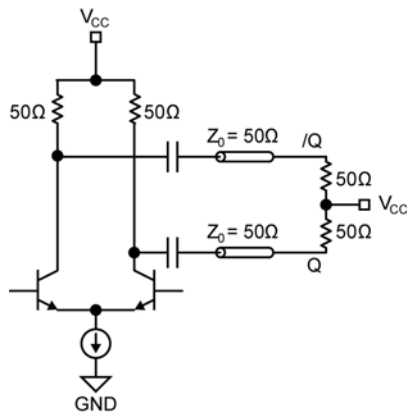


**Figure 8e. LVDS Interface (DC-Coupled)**

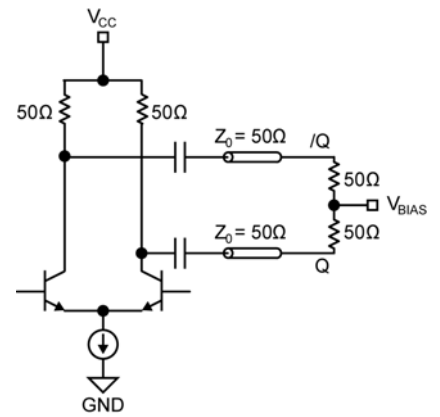
## CML Output Termination



**Figure 9a. CML AC-Coupled Termination - 100Ω Differential**

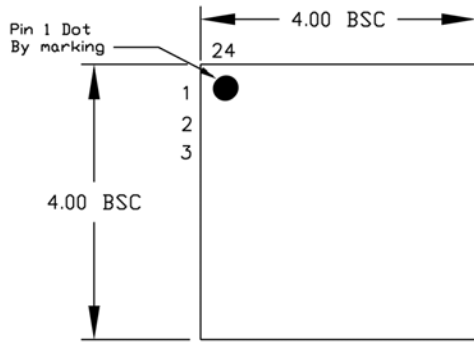


**Figure 9b. CML AC-Coupled Termination - 50Ω to V<sub>CC</sub>**

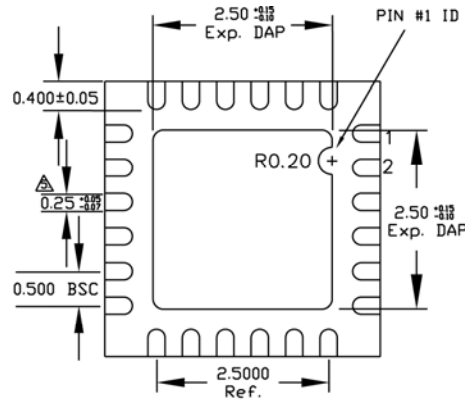


**Figure 9c. CML AC-Coupled Termination - 50Ω to V<sub>BIAS</sub>**

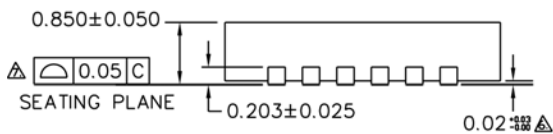
**Package Information**



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
- △ DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
- △ APPLIED ONLY FOR TERMINALS.
- △ APPLIED FOR EXPOSED PAD AND TERMINALS.

**24-Pin (4mm x 4mm) QFN**

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