Data Sheet | October 30, 2008 | FN6230.1

High-Speed 18V CMOS Comparators

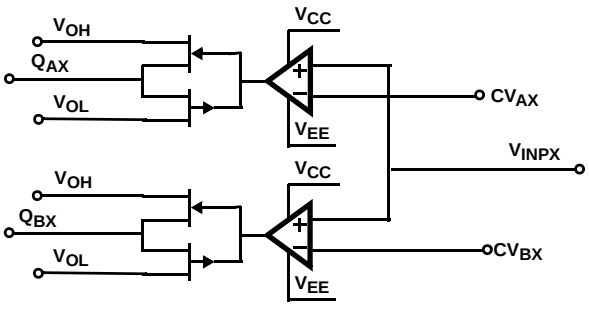
ISL55141, ISL55142, ISL55143 integrated circuits are high-speed, wide input common-mode range comparators. They provide three-state window comparators in a high voltage CMOS process (18V). Each comparator has dual receive thresholds, CV_A and CV_B, for establishing minimum 1-V_{IH} and maximum 0-V_{IL} voltage levels. These devices can accept inputs from a number of logic families, such as TTL, ECL, CMOS, LVCMOS, LVDS and CML. Two bits of output per comparator provide the test controller with qualification of a comparator input into three states. The two output bits work with a separate user supply to establish V_{OH}, V_{OL} levels compatibility with the system's controller logic levels.

Fast propagation delay (9.5ns typical at ±50mV overdrive) makes this family compatible with high-speed digital test systems. The 18V range enables the comparator input to operate over a wide input range. Two references per input enable and three state digitalization of input with voltage swings of up to 13V common mode. The operating frequency of these devices is typically 65MHz.

High voltage CMOS process makes these devices ideal for large voltage swing applications, such as special test voltages levels associated with Flash devices or power supervision applications and may avoid the need for test bus isolation relay(s).

Functional Block Diagram

DUAL LEVEL COMPARATOR - RECEIVERS



Note: x denotes 1, 2 or 4 channels for ISL55141, ISL55142 and ISL55143, respectively

Features

- 18V I/O Range
- 65MHz Operation
- 9.5ns Typical Propagation Delay
- Programmable Input Thresholds
- User Defined Comparator OutputLlevels
- Common-Mode Range Includes Negative Rails
- Small Footprints in QFN Packages
- Power-Down Current <10µA
- Pb-Free (RoHS compliant)

Applications

- Burn in ATE
- Low Cost ATE
- Fast Supervisory Power Control
- Instrumentation

Ordering Information

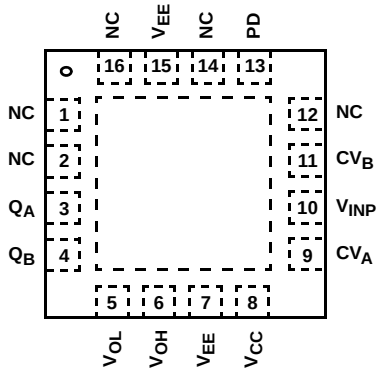
PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL55141IRZ*	55 141IRZ	-40 to +85	16 Ld QFN	L16.4X4A
ISL55141IVZ*	55141 IVZ	-40 to +85	14 Ld TSSOP	M14.173
ISL55142IRZ*	55142 IRZ	-40 to +85	20 Ld QFN	L20.5x5
ISL55142IVZ*	55142 IVZ	-40 to +85	20 Ld TSSOP	M20.173
ISL55143IRZ*	55143 IRZ	-40 to +85	36 Ld TQFN	L36.6X6

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

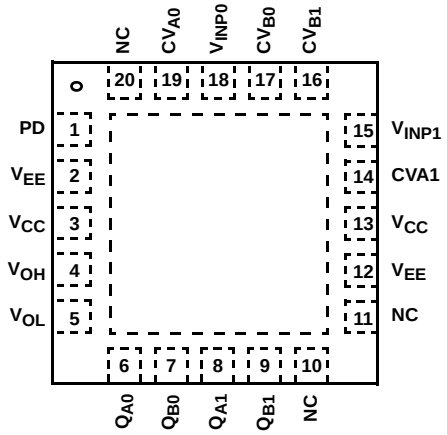
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

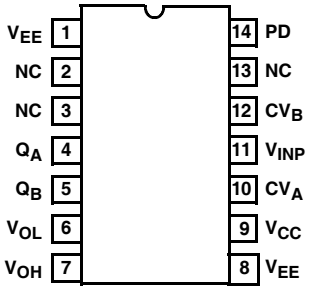
ISL55141 SINGLE DEVICE
(16 LD 4X4 QFN)
TOP VIEW



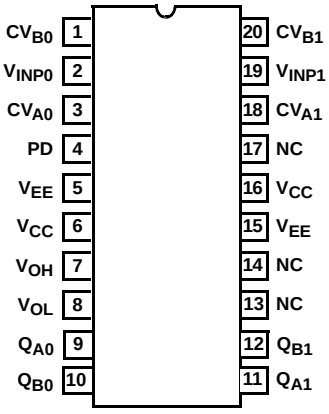
ISL55142 SINGLE DEVICE
(20 LD 5X5 QFN)
TOP VIEW



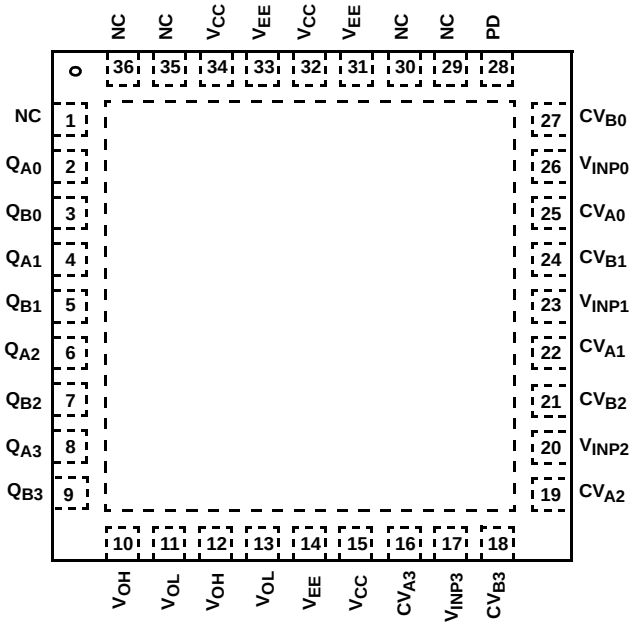
ISL55142
(20 LD TSSOP)
TOP VIEW



ISL55141
(14 LD TSSOP)
TOP VIEW



ISL55143 QUAD DEVICE
(36 LD6X6 TQFN)
TOP VIEW



Pin Descriptions

PIN	FUNCTION
V_{EE}	Negative supply input
Q_{AX}	Channel A, CV_{AX} reference driven. Comparator output.
Q_{BX}	Channel B, CV_{BX} reference driven. Comparator output.
V_{OL}	Comparator output logic low supply. Unbuffered analog input that sets all Q_{AX}, Q_{BX} “low” voltage level.
V_{OH}	Comparator output logic high supply. Unbuffered analog input that sets all Q_{AX}, Q_{BX} “high” voltage level.
VCC	Positive supply input.
CV_{AX}	Channel A comparator reference analog input.
V_{INPX}	Window comparator input. Common to both Channel Ax and Channel Bx.
CV_{BX}	Channel B comparator reference analog input.
PD	Power-down logic input (connect to V_{EE} if not used for power-down).
NC	No internal connection.

TABLE 1. CV_A-Q_A AND CV_B-Q_B BASIC COMPARATOR TRUTH TABLE

INPUT		OUTPUTS*	
V_{INPX}		Q_{AX}	Q_{BX}
$<CV_{AX}$	$<CV_{BX}$	0	0
$<CV_{AX}$	$>CV_{BX}$	0	1
$>CV_{AX}$	$<CV_{BX}$	1	0
$>CV_{AX}$	$>CV_{BX}$	1	1
* When Q_{AX}/Q_{BX} = 1, Output is connect to V_{OH}			
* When Q_{AX}/Q_{BX} = 0, Output is connect to V_{OL}			

Absolute Maximum Ratings

V_{CC} to V_{EE} . . . . . -0.5V to 19V
Input Voltages
PD, CV_{AX}, CV_{BX}, V_{INPX}, V_{OH}, V_{OL}
. . . . . (V_{EE} -0.5V) to (V_{CC} +0.5V)
Output Voltage
Q_{AX}, Q_{BX} . . . . . (V_{OL} -0.5V) to (V_{OH} +0.5V)

Thermal Information

Thermal Resistance (Typical, Note 1, 2)	θ_{JA} (°C/W)
16 Ld QFN Package	75
14 Ld TSSOP Package	90
20 Ld QFN Package	65
20 Ld TSSOP Package	80
36 Ld TQFN Package	45

Maximum Junctin Temperature (Plastic Plackage) . . . 150°
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. Device temperature is closely tied to data-rates, driver loads and overall pin activity. Review Power Dissipation Considerations for more information.

Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Device Power	V_{CC}-V_{EE}	10	15	18	V
Comparator Output High Rail	V_{OH}	V_{EE}+1		V_{CC}-0.5	V
Comparator Output Low Rail	V_{OL}	V_{EE}+0.5		V_{EE}+6	V
Common Mode Input Voltage Range	V_{CM}	V_{EE}		V_{CC}-5	V
Ambient Temperature	T_A	-40	27	+85	°C
Junction Temperature	T_J			+125	°C

Electrical Specifications

Test Conditions: V_{CC} = 12V, V_{EE} = -3V, V_{OH} = 5V, V_{OL} = 0V, PD = V_{EE}, C_{LOAD} = 15pF, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DC CHARACTERISTICS						
Input Offset Voltage	V_{OS}	CV_{AX} = CV_{BX} = 1.5V	-50		50	mV
Input Bias Current	I_{BIAS}	V_{INPX} - $CV_{(A/B)X}$ = ±5V		10	25	nA
Power-down Current	I_{PD}	PD = V_{CC}		8	25	µA
Power-down Time (Note 5)	t_{PD}			10		µs
Power-up Time (Note 5)	t_{PU}			15		µs
TIMING CHARACTERISTICS						
Propagation Delay	t_{pd}		4.0	9.5	15	ns
Rise Time (Note 5)	t_r			1.4		ns
Fall Time (Note 5)	t_f			1.5		ns
Propagation Delay Mismatch	Δt_{pd}			0.5	2	ns
Maximum Operating Frequency	F_{MAXR}	Symmetry 50%		65		MHz
Min Pulse Width	t_{WIDR}			7.7		ns
COMPARATOR INPUT						
Input Current	I_{IN}	V_{INPX} = V_{CC} or V_{EE}	-100	0	100	nA
Input Capacitance (Note 5)	C_{IN}			2.5		pF

Electrical Specifications Test Conditions: V_{CC} = 12V, V_{EE} = -3V, V_{OH} = 5V, V_{OL} = 0V, PD = V_{EE}, C_{LOAD} = 15pF, T_A = 25°C, unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
DIGITAL OUTPUTS Q_{AX}, Q_{BX}						
Output Resistance	RoutR		18	27	37	Ω
Output Logic High Voltage	V_{OH}	V_{OH} = 5V, I_{SOURCE} = 1mA	4.9	4.95	5.0	V
Output Logic Low Voltage	V_{OL}	V_{OL} = 0V, I_{SINK} = 1mA	0.00	0.05	0.1	V
POWER SUPPLIES, STATIC CONDITIONS						
Positive Supply DC Current/Comparator	I_{CC}	No input data		+8.25	12.5	mA
Negative Supply Current/Comparator	I_{EE}	No input data	-12.5	-8.25		mA
Total Power Dissipation/Comparator	P (Note 6)	Input data at 40MHz		670		mW

NOTES:

3. Lab characterization, room temperature, timing parameters matched stimulus/loads, channel-to-channel skew < 500ps, 1ns maximum by design
4. Note about I_{CC} measurement input can approach 140mA (single comparator) at maximum pattern rates
5. Limits should be considered typical and are not production tested.
6. Total Power dissipation per comparator can be approximately calculated from the following:
   $P = (V_{CC}-V_{EE})*8.25mW + 90pF*(V_{CC}-V_{EE})^2*f + C_L*(V_{CC}-V_{EE})^2*f$, where f is the operating frequency and C_L is the load capacitance. Because the ISL55142 has two comparators, the power dissipation would be twice of P calculated from this equation. The ISL55143 would be four times P.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms

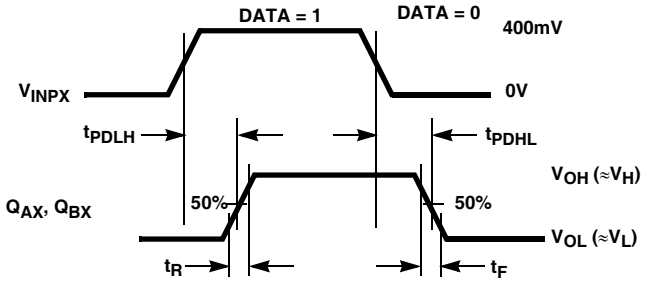
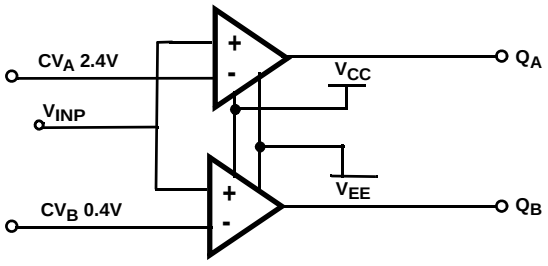


FIGURE 1. COMPARATOR PROPAGATION DELAY AND TRANSITION TIME MEASUREMENT POINTS



Although there is no electrical difference between the CV_A and CV_B Inputs, if one defines CV_A as being the high threshold and CV_B being the low threshold, it becomes easier to understand the utilization of a dual threshold comparator. Essentially this enables the qualification of an incoming signal into three states. In Figure 2, the three states are Valid Low <0.4V, No-man's-land (between 0.4 and 2.4V), Valid High >2.4V. Table 1 shows how the Q_A/Q_B truth table would be utilized in the real world.

TABLE 1. Q_A/Q_B TRUTH TABLE

V_{INP}	Q_A	Q_B	COMMENT
<0.4V	0	0	Valid 0
>0.4 and <2.4V	0	1	Invalid
>2.4V	1	1	Valid 1

FIGURE 2. THREE-STATE WINDOW COMPARATOR FUNDAMENTALS

Test Circuits and Waveforms (Continued)

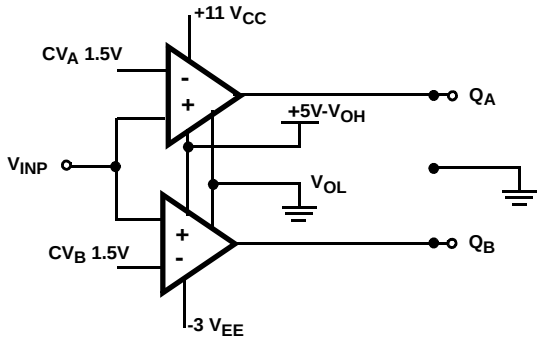


FIGURE 3. t_{PD} RECEIVER SWITCHING TEST CIRCUIT

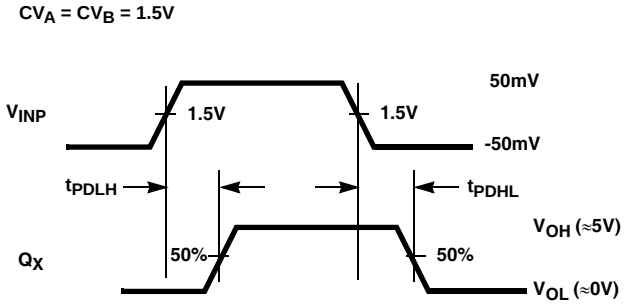


FIGURE 4. t_{PD} RECEIVER PROPAGATION DELAY MEASUREMENT POINTS

Application Information

The ISL55141, ISL55142, ISL55143 provide 1, 2 and 4 dual threshold, three-state window comparator(s) in TSSOP or QFN footprints. They offer a combination of speed (10ns Tpd and wide voltage range (18V). This product directly addresses the need for unique common-mode characteristics while supplying a power-down feature.

Figures 3 and 4 show the stimulus setup and measurement points for an example propagation delay measurement. Typical room temperature results are displayed in Figure 11.

Figure 4 shows a V_{INP} range of 50mV. In Figure 11 the offset is increased in the horizontal axis from 50mV above and below the reference (1.5V) up to 2.5V above and below the 1.5V reference.

Two lines are displayed in Figure 11. One represents the rising-to-rising delay (t_{PDLH}) and the other the falling-to-falling delay (t_{PDHL}).

Comparator Features

These three-state window comparators feature high output current capability, and user defined high and low output levels to interface with a wide variety of logic families. Each receiver comprises two comparators and each comparator has an independent threshold level input, making it easy to implement (Minimum1-V_{IH})/(Maximum 0-V_{IL}) logic level comparator functions. The CV_{AX} and CV_{BX} pins set the threshold levels of the A and B comparators respectively. V_{OH} and V_{OL} set all the comparator output levels, and V_{OH} must be more positive than V_{OL}. These two inputs are unbuffered supply pins, so the sources driving these pins must provide adequate current for the expected load. V_{OH} and V_{OL} typically connect to the power supplies of the logic device driven by the comparator outputs.

The truth table for the receivers is given in Table 1. Receiver outputs are not tri-statable, and do not incorporate any on-chip short circuit current protection. Momentary short circuits to GND, or any supply voltage, will not cause permanent damage, but care must be taken to avoid longer duration short circuits. If tolerable to the application, current limiting resistors can be inserted in series with the Q_{AX} and Q_{BX} outputs to protect the receiver outputs from damage due to overcurrent conditions.

Power-down Features

The ISL55141, ISL55142, ISL55143 PD pin provides a means of reducing current consumption when the device is not in use. Supply currents fall from ~7mA to less than 10µA in the power-down mode. The device requires approximately 10µs to power-down and 15µs to power-up.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_{EE} pin is connected to ground, one 0.1µF ceramic capacitor should be placed from the V_{CC} pin to ground. A 4.7µF tantalum capacitor should then be connected from the V_{CC} pin to ground. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Power Dissipation Considerations

Specifying continuous data rates, driver loads and driver level amplitudes are key in determining power supply requirements as well as dissipation/cooling necessities. Driver output patterns also impact these needs. The faster the pin activity, the greater the need to supply current and remove heat.

The maximum power dissipation allowed in a package is determined according to Equation 1.

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

Approximate Power Dissipation

(Typ) P = N*[(V_{CC}-V_{EE})*8.25mW + 90pF*(V_{CC}-V_{EE})^2*f + CL*(V_{OH}-V_{OL})^2*f]

where:
N is the number of comparators in the chip
(1 for ISL55141, 2 for ISL55142 and 4 for ISL55143).
(f) is the operating frequency.
CL is the load capacitor.

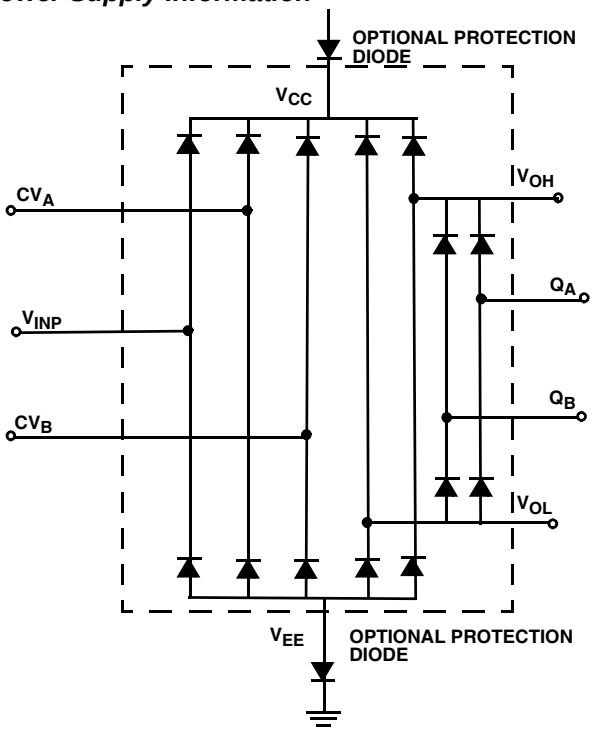
The power dissipation calculated from the above formula may have an error of ±20 to 25%.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads. Power also depends on the number of channels changing state and frequency of operation. The extent of continuous active pattern generation/reception will greatly affect dissipation requirements.

The user should evaluate various heat sink/cooling options in order to control the ambient temperature part of the equation. This is especially true if the user's applications require continuous, high-speed operation.

Note: The reader is cautioned against assuming the same level of thermal performance in actual applications. A careful inspection of conditions in your application should be conducted.

Power Supply Information



Circuit design must always take into account the internal EOS/ESD protection structure of the device.

Important Note: The QFN package metal plane is used for heat sinking of the device. It is electrically connected to the negative supply potential (V_{EE}). If V_{EE} is tied to ground, the thermal pad can be connected to ground. Otherwise, the thermal pad (V_{EE}) must be isolated from other power planes.

Power Supply Sequencing

The ISL55141, ISL55142, ISL55143 reference every supply with respect to V_{EE}. Therefore, apply V_{EE}, V_{OL} then V_{CC} followed by the CV_A and CV_B supplies. The comparator V_{INP} pin should not exceed V_{EE} or V_{CC} during power-up.

In cases where inputs may exceed voltage rails during power-up, series resistance should be employed to safeguard EOS to the ESD protection diodes.

Typical Performance Curves

Device installed on Intersil ISL55141, ISL55142, ISL55143 Evaluation Boards.

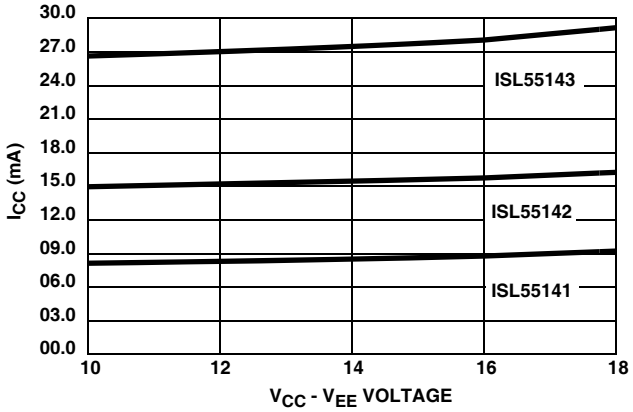


FIGURE 5. ISL55141, ISL55142, ISL55143 QUIESCENT CURRENT

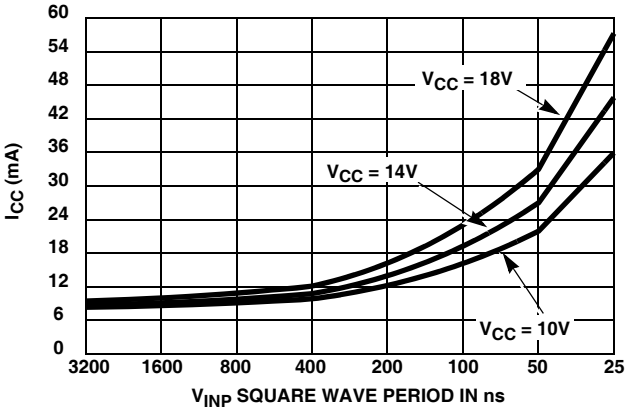


FIGURE 6. ISL55141 I_{CC} vs FREQUENCY @ 10V, 14V, AND 18V

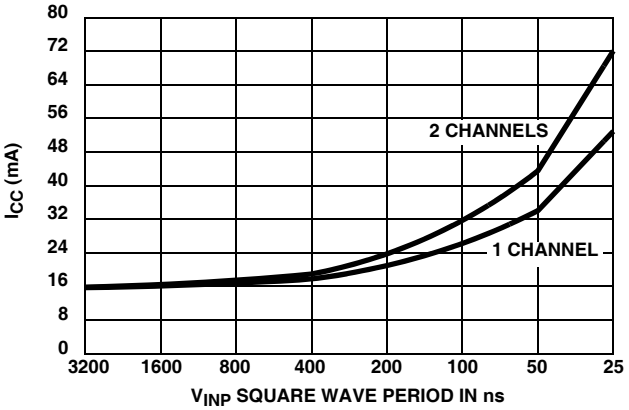


FIGURE 7. ISL55142 I_{CC} 1 AND 2 CHANNELS ACTIVE

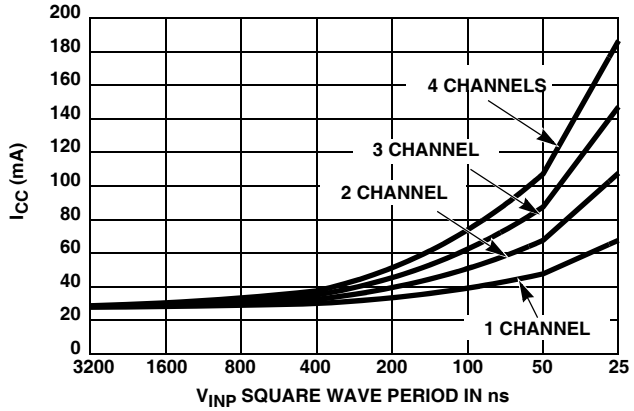


FIGURE 8. ISL55143 I_{CC} 1, 2, 3, 4 CHANNELS ACTIVE

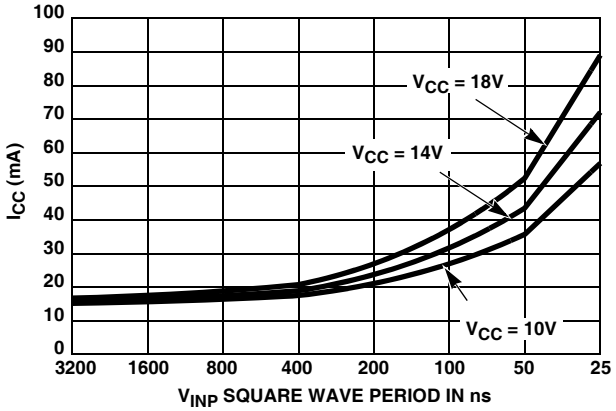


FIGURE 9. ISL55142 2-CHANNEL I_{CC} @ 10V, 14V, AND 18V

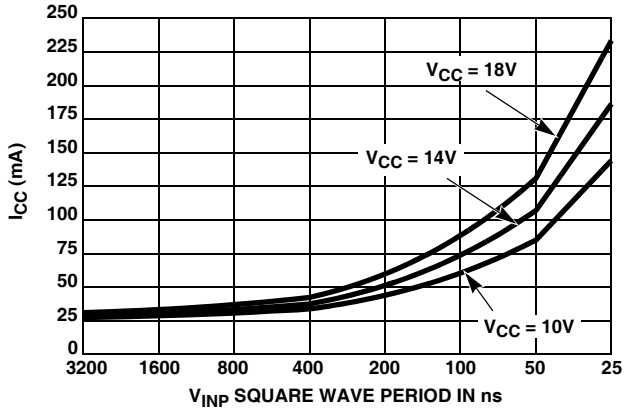


FIGURE 10. ISL55143 4-CHANNEL I_{CC} @ 10V, 14V, AND 18V

Typical Performance Curves Device installed on Intersil ISL55141, ISL55142, ISL55143 Evaluation Boards. **(Continued)**

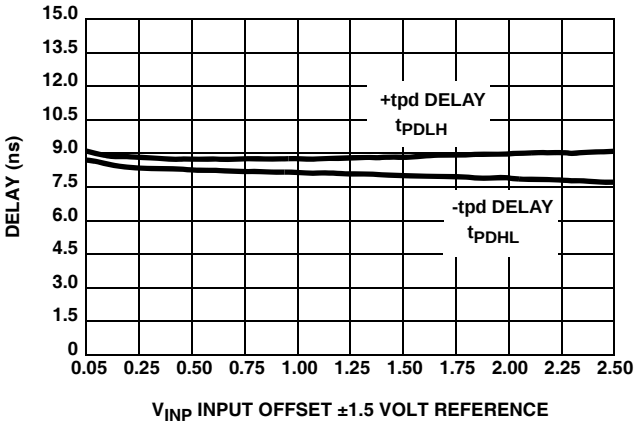


FIGURE 11. PROPAGATION DELAY @ 14V V_{CC}-V_{EE}

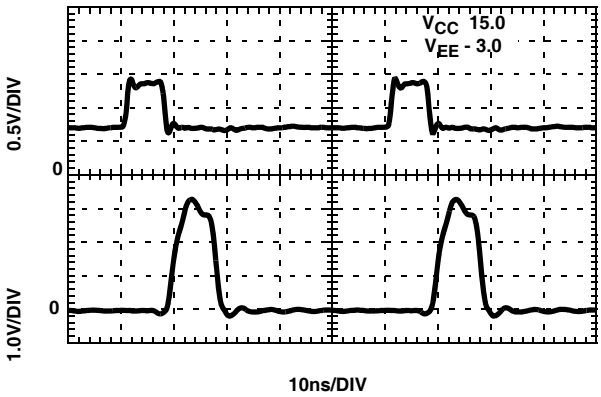
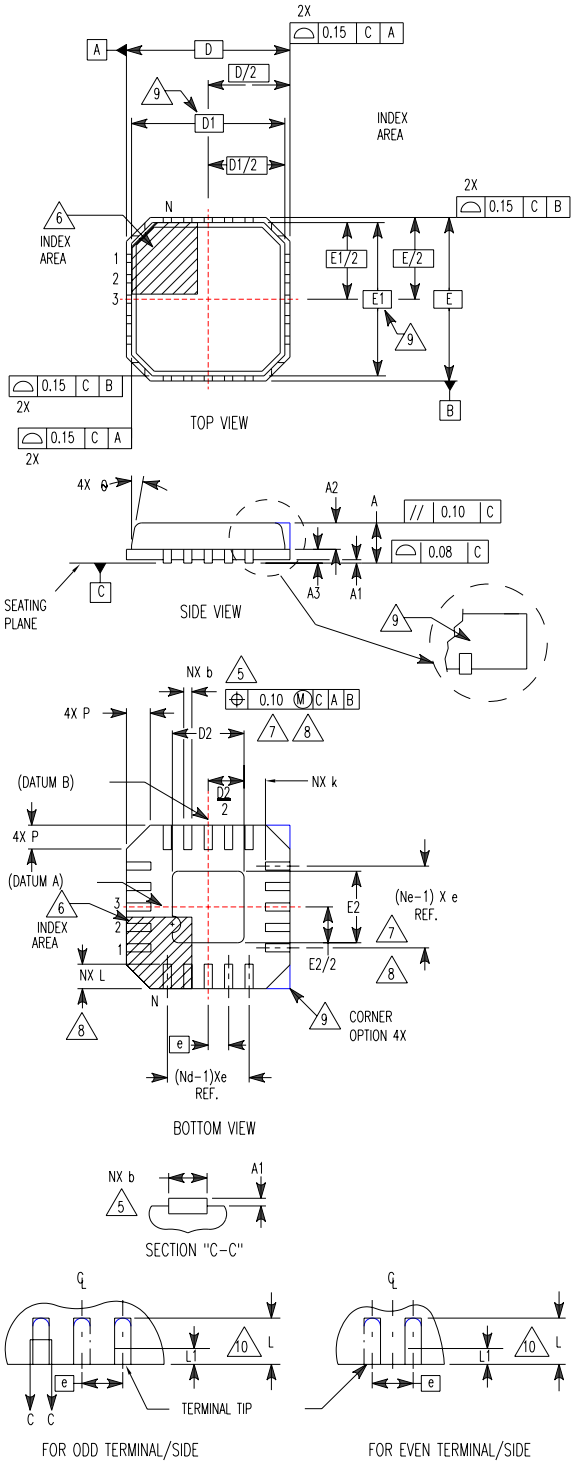


FIGURE 12. MINIMUM PULSE WIDTH RESPONSE

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4A

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGD-10)

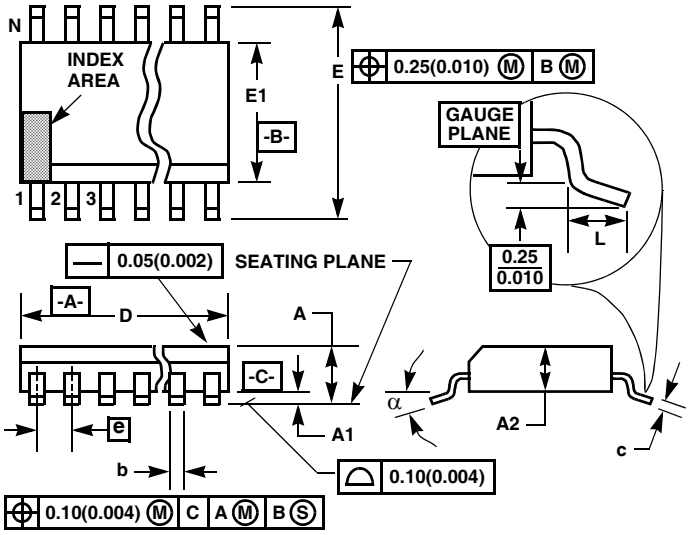
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	2.30	2.40	2.55	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	2.30	2.40	2.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.40	0.50	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 2 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

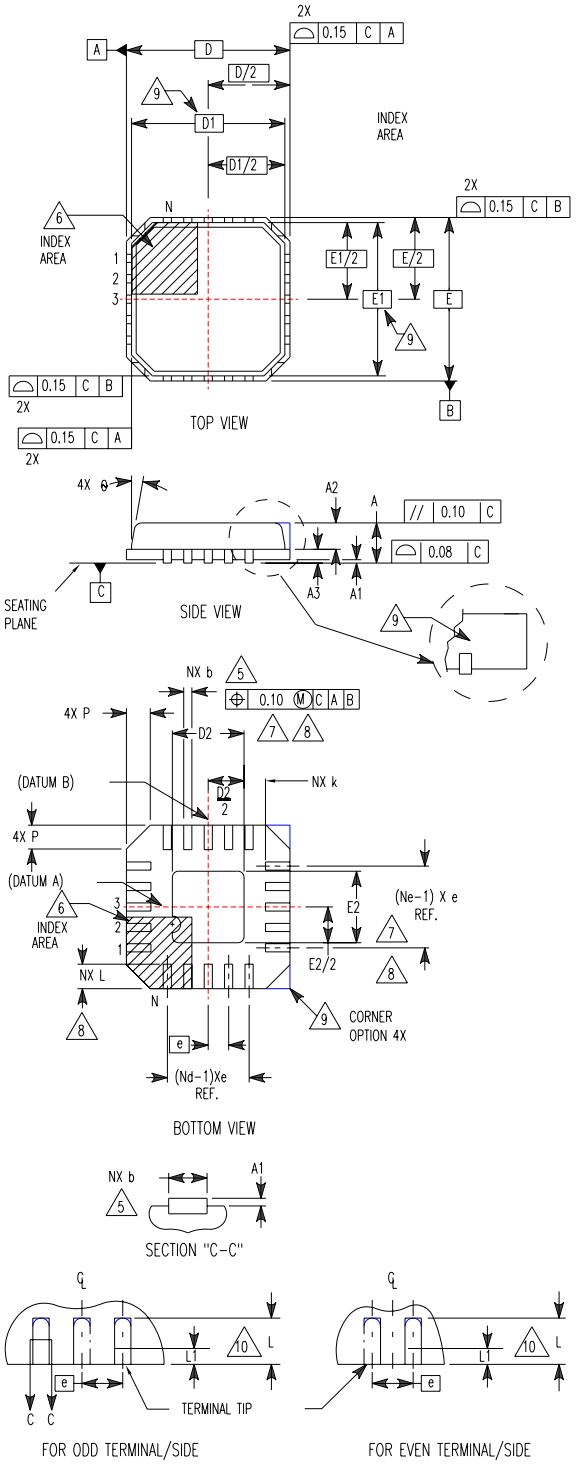
M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 4/06

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.5x5

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

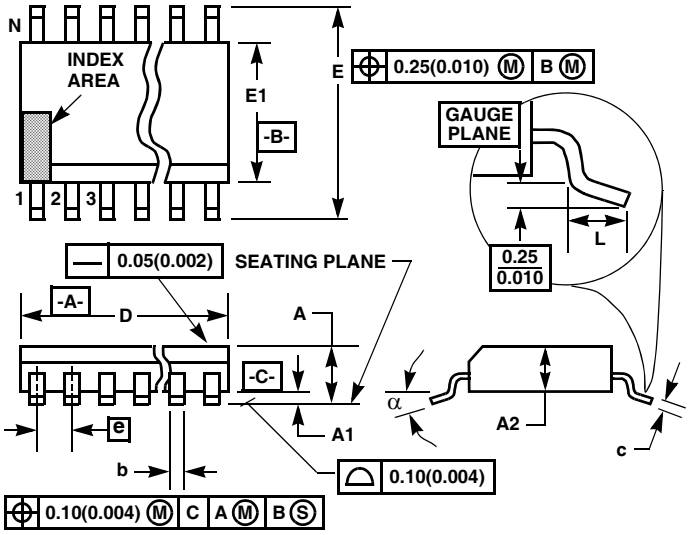
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	0.02	0.05	-
A2	-	0.65	1.00	9
A3		0.20 REF		9
b	0.23	0.30	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.20	-	-	-
L	0.35	0.60	0.75	8
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 4 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220VHHC Issue I except for the "b" dimension.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M20.173

20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

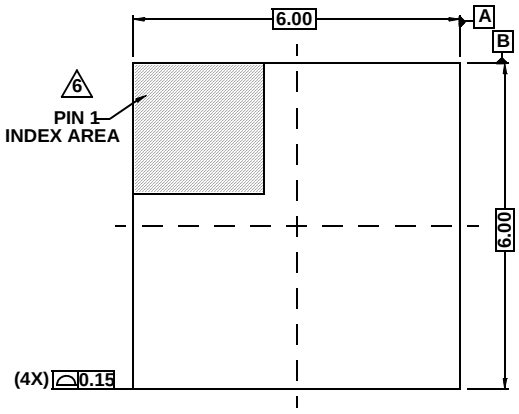
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.252	0.260	6.40	6.60	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

Rev. 1 6/98

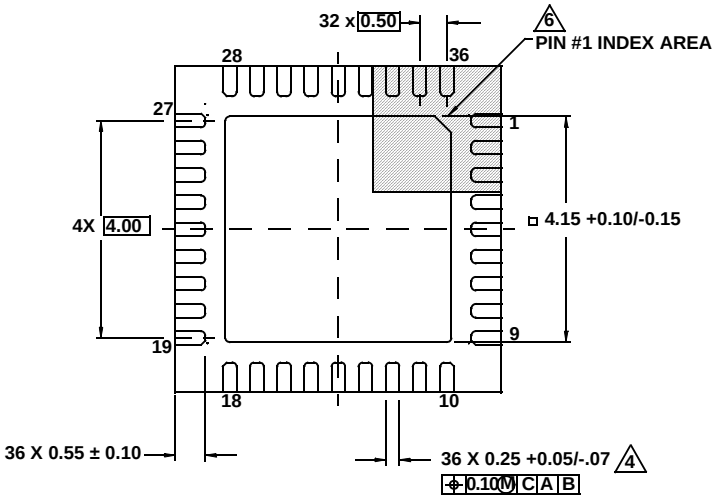
Package Outline Drawing

L36.6x6

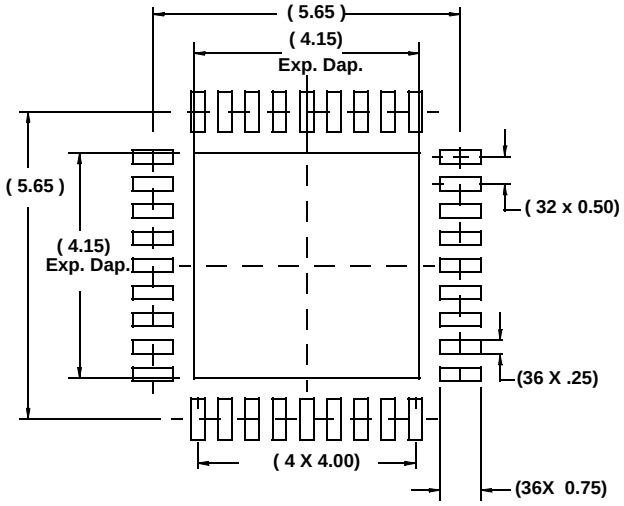
36 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 08/08



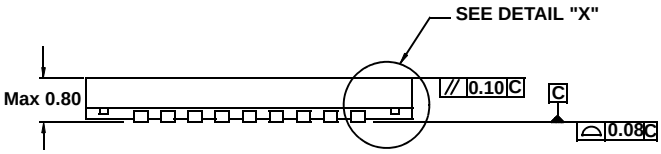
TOP VIEW



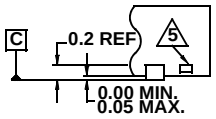
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSEY14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.