

### Features

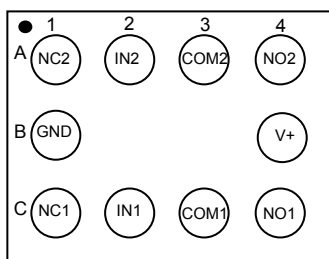
- Low Voltage Operation
- Low On-Resistance  $R_{on} = 0.4\Omega @ 2.7 V$
- $-69 dB O_{IRR} @ 2.7 V$ , 100 kHz MSOP-10 and DFN-10 Packages ESD Protection  $>2000 V$
- Latch-Up Current  $>300 mA$  (JESD 78)

### Benefits

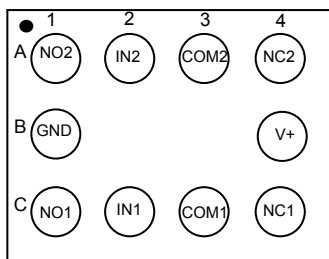
- Reduced Power Consumption
- High Accuracy
- Reduce Board Space
- 1.8-V Logic Compatible
- High Bandwidth

### Applications

- Cellular Phones
- Speaker Headset Switching Audio
- Video Signal Routing
- PCMCIA Cards
- Battery Operated Systems
- Relay Replacement
- USB1.1

**PA3535**


Top View

**PA3536**


Top View

### Truth Table

Logic	NC1 and NC2	NO1 and NO2
0	ON	OFF
1	OFF	ON

### Description

The PA3535/PA3536 are 0.4Ω dual SPDT analog switches designed for low voltage applications.

The PA3535/PA3536 has on-resistance matching (less than  $0.05\Omega @ 2.7 V$ ) and flatness (less than  $0.2\Omega @ 2.7 V$ ) that is guaranteed, over the entire voltage range. Additionally, low logic thresholds make the PA3535/PA3536 an ideal interface to low voltage DSP control signals.

The PA3535/PA3536 has fast switching speed with break-before-make guaranteed. In the On condition, all switching elements conduct equally in both directions. Off-isolation and crosstalk is  $-69 dB @ 100 kHz$ .

The PA3535/PA3536 contains the additional benefit of 2,000 Volt ESD protections.

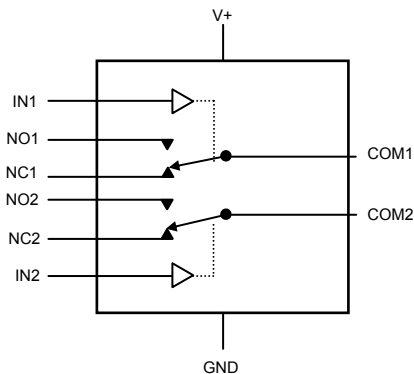
In space saving CSP (Pb-free) packages, the PA3535/PA3536 are high performance, low  $R_{on}$  switches for battery powered applications.

No (Pb) is used in the manufacturing process either inside the device/package or on the external terminations.

As a committed partner to the community and the environment, ProTek Analog manufactures this product with the lead (Pb)-free device terminations.

The different lead (Pb)-free materials are interchangeable and meet all JEDEC standards for reflow and MSL rating.

### Functional Diagram



### Ordering Information

7" Reel	Temp Range	Package	Part Number
3000	-40 to +80°C	Flip Chip 10 Bump	PA3535-LF-T7 PA3536-LF-T7

**Absolute Maximum Ratings**
*Reference to Ground*

V+	-0.3 to +6.0V
IN, COM, NC, NO	-0.3 to (V+ +0.3V)
Continuous Current (NO, NC, COM)	300mA
Peak Current	500mA
(Pulsed at 1mS, 10% Duty Cycle)	
Storage Temperature (D Suffix)	-65 to 150°C
ESD per Method 3015.7	> 2KV
Power Dissipation	457mWATT

**Recommended Operating Conditions**

Supply Voltage Operating (VCC)	1.65V to 5.5V
Control Input Voltage (VIN)	.0V to VCC
Switch Input Voltage (VIN)	.0V to VCC
Output Voltage (VOUT)	.0V to VCC
Operating Temperature (TA)	-40°C to +85°C
Input Rise and Fall Time (tr,tf)	
Control Input VCC = 2.3V - 3.6V	0ns/V to 10ns/V
Control Input VCC = 4.5V - 5.5V	0ns/V to 5ns/V
Thermal Resistance (ΘJA)	350°C/W

**NOTES**

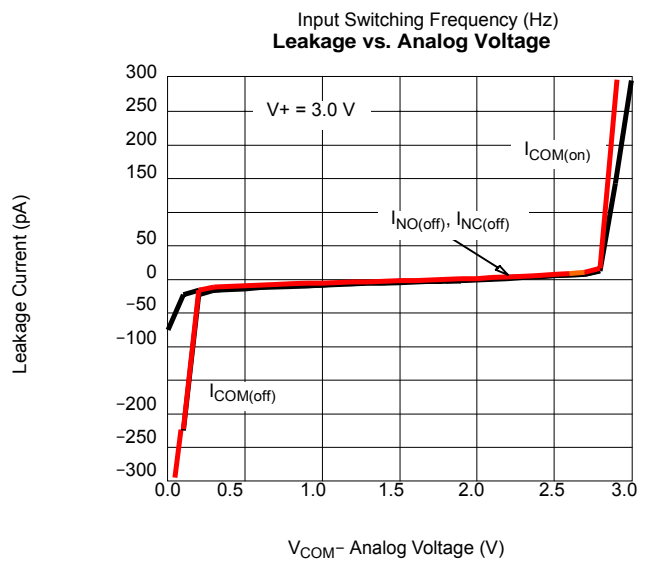
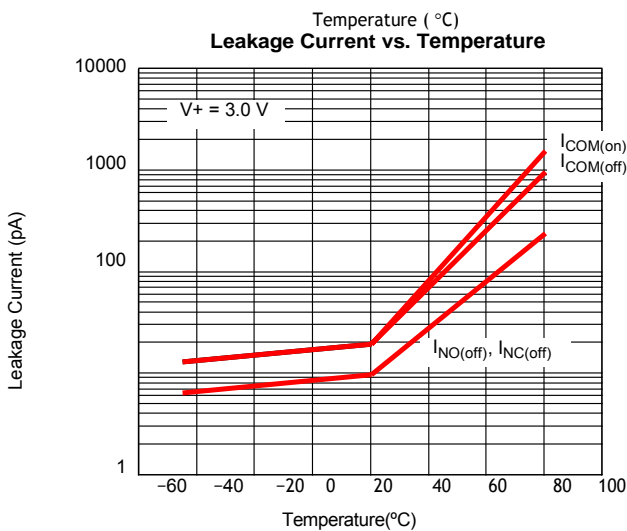
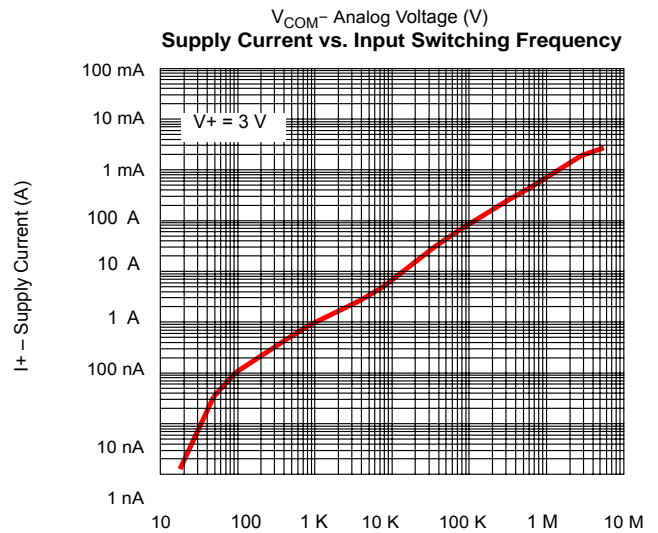
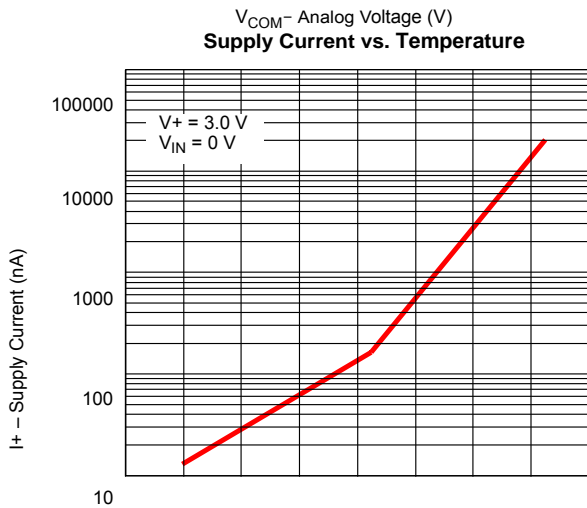
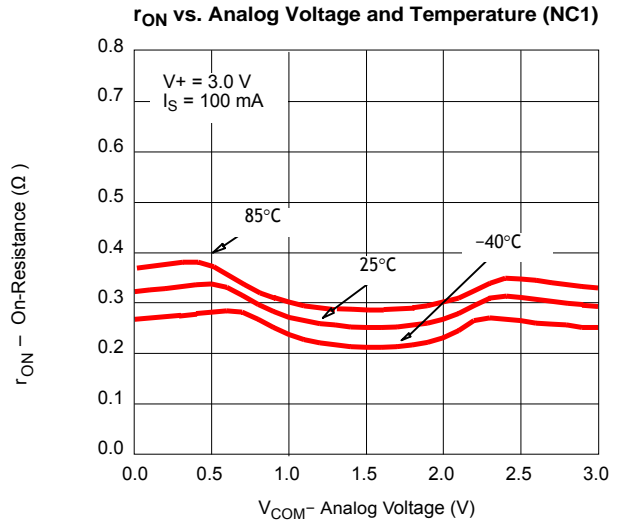
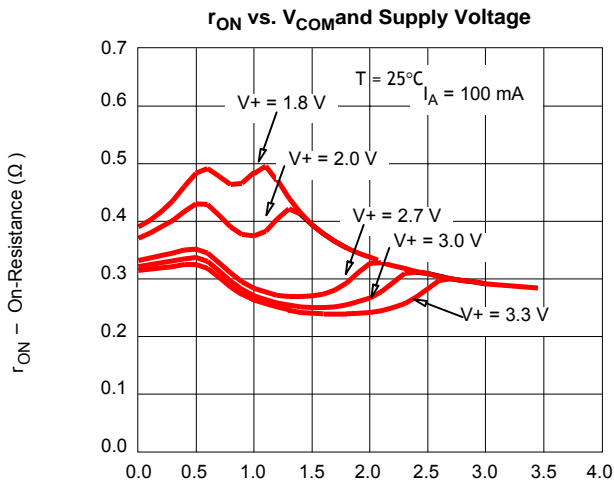
- Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads soldered to PC Board.
- Derate 5.7 mW/ °C above 70 °C

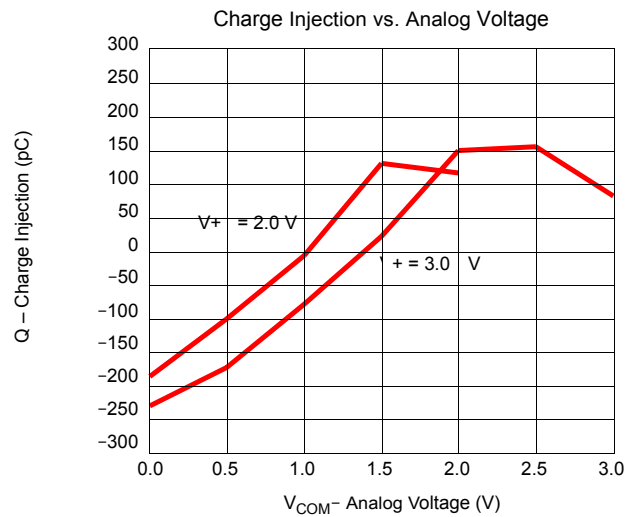
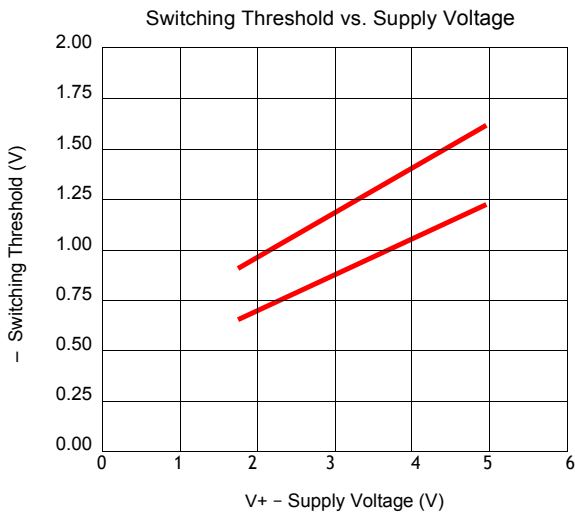
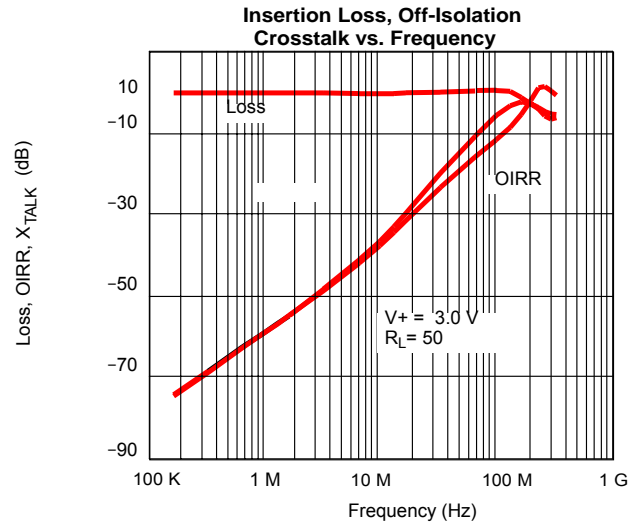
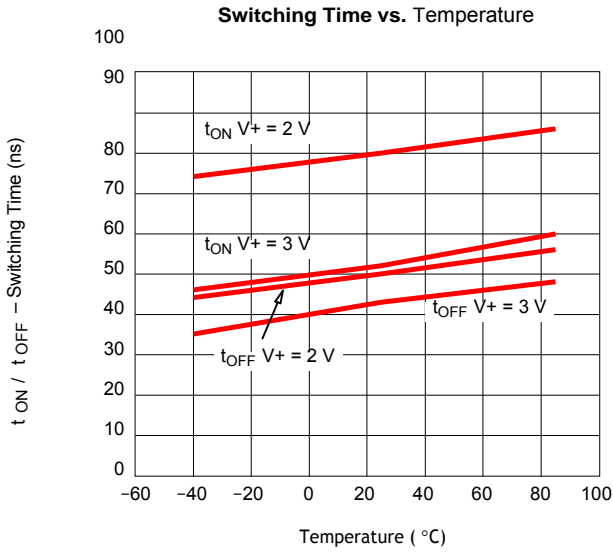
*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**Specification V+ = 3.0V** Test Conditions unless otherwise specified:  $V_+ = 3.0V \pm 10\%$ ,  $V_{IN} = 0.4 V$  or  $2.0V$

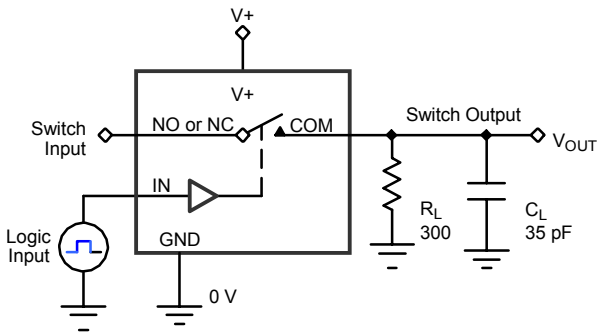
Parameter	Symbol	Test Conditions	Temp	Min	Typ	Max	Unit
<b>Analog Switch</b>							
Analog Signal Range	$V_{NO}, V_{NC}, V_{COM}$		Full	0.0		$V_{CC}$	V
On-Resistance	$R_{ON}$	$V_{CC} = 2.7V, V_{COM} = 0.9V - 1.5V$ $I_{NO}, I_{NC} = 50mA,$	Room		0.4	0.4	Ω
$R_{ON}$ Matching	$\Delta R_{ON}$		Full			0.05	
$R_{ON}$ Flatness	$R_{ON(FLAT)}$				0.09	0.15	
Switch Off Leakage Current	$I_{OFF(NO)}$ or $I_{OFF(NC)}$	$V_+ = 3.3 V,$ $V_{NO}, V_{NC} = 1.0 V/3.0 V, V_{COM} = 3.0 V/1.0 V$	Room	-1		-1	nA
	$I_{COM(OFF)}$		Full	-10		-10	
Channel On Leakage Current	$I_{COM(ON)}$	$V_+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1.0V/3.0 V$	Room	-1		-1	
Full			Full	-10		-10	
<b>Digital Control</b>							
Input High Voltage	$V_{INH}$		Full	2.0			V
Input Low Voltage	$V_{INL}$		Full			0.5	
Input Capacitance	$C_{in}$		Full		10		pF
Input Current	$I_{INL}$ or $I_{INH}$	$V_{IN} = 0$ or $V_+$	Full	1		1	μA
<b>Dynamic Characteristics</b>							
Turn On Time	$t_{ON}$	$V_{NO}$ or $V_{NC} = 2.0 V, R_L = 300 \Omega, C_L = 35 pF$	Room		52	82	nS
Turn Off Time	$t_{OFF}$		Full		43	73	
Break Before Make Time	$t_{BBM}$		Full	1	6	78	
Charge Injection	$Q_{INJ}$	$CL = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 \Omega$	Room		21		pC
Off Isolation	OIRR	$RL = 50 \Omega, CL = 5 pF, f = 1 MHz$	Room		-69		dB
Crosstalk	$X_{TALK}$		Room		-69		
NO, NC OFF Capacitance	$C_{NO(off)}$ $C_{NC(off)}$	$V_{IN} = 0$ or $V_+, f = 1 MHz$	Room		145		pF
Chanel On Capacitance	$C_{ON}$		Room		406		
<b>Power Supply</b>							
Supply Range	V+	$V_{IN} = 0$ or $V_+$		1.8		5.5	V
Supply Current	I+				0.01	1.0	μA

TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





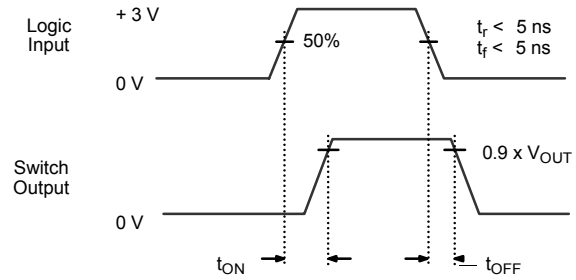
**Test Circuits**



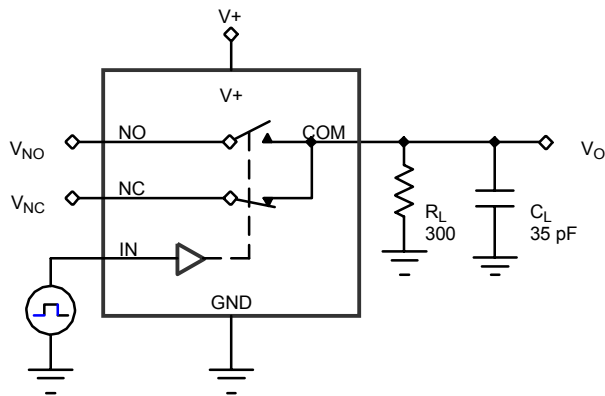
$C_L$  (includes fixture and stray capacitance)

$$V_{OUT} = V_{COM} \left( \frac{R_L}{R_L + R_{ON}} \right)$$

**Figure 1. Switching Time**

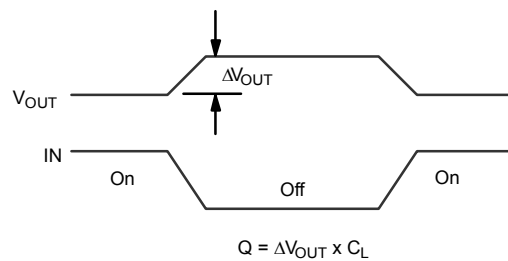
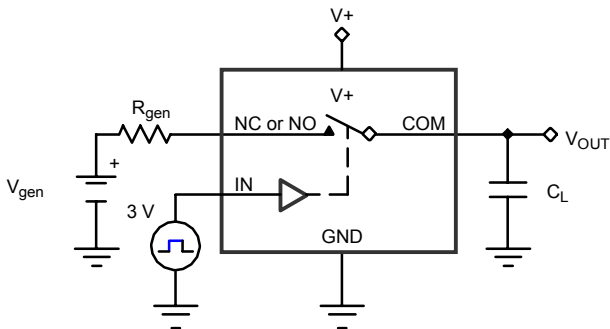
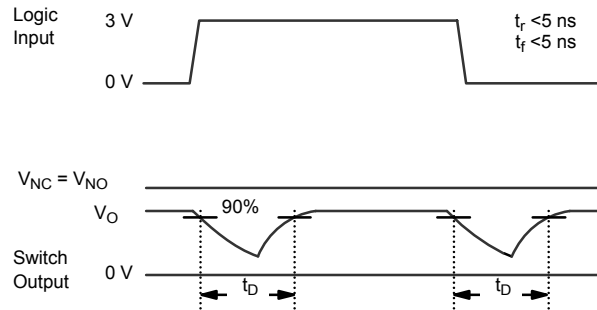


Logic "1" = Switch On  
Logic input waveforms inverted for switches that have the opposite logic sense.



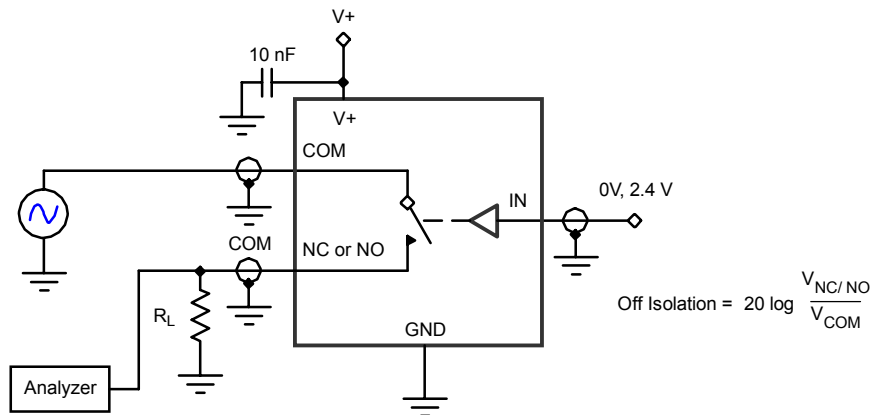
$C_L$  (includes fixture and stray capacitance)

**Figure 2. Break-Before-Make Interval**

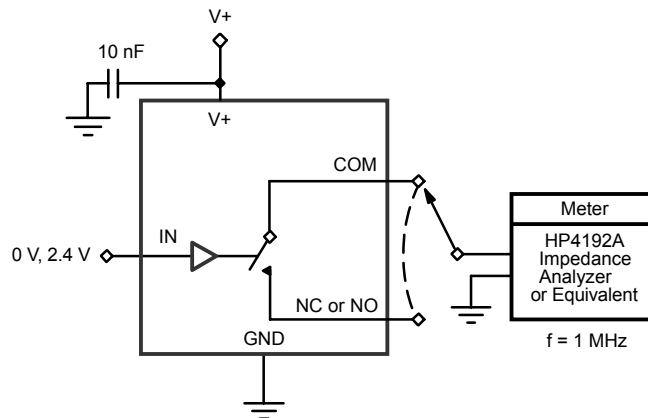


IN depends on switch configuration: input polarity determined by sense of switch.

**Figure 3. Charge Injection**

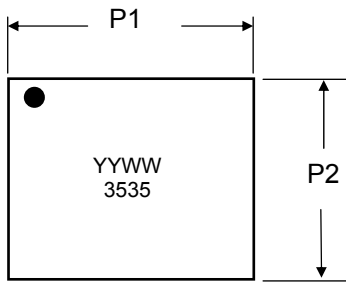


**Figure 4. Off-Isolation**

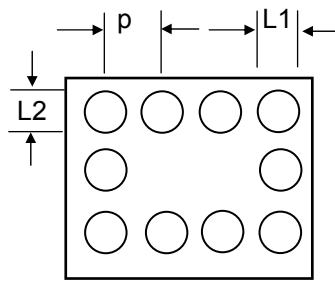


**Figure 5. Channel Off/On Capacitance**

**Package Outline and Dimensions Flip-Chip 10-Bump**

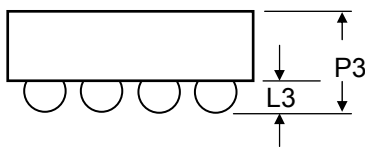


TOP VIEW

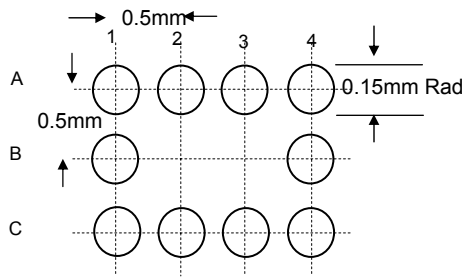


BOTTOM VIEW

Dim	MILLIMETERS		
	MIN	TYP	MAX
P1	1.98	2.00	2.02
P2	1.49	1.50	1.52
P3	0.68	0.71	0.75
L1	0.30	0.32	0.34
L2	0.30	0.32	0.34
L3	0.22	0.24	0.26
p	0.50	0.50	0.50



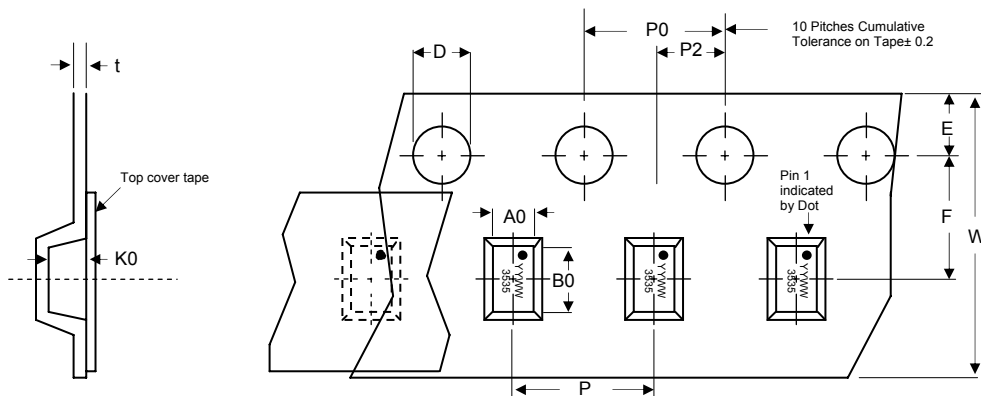
SIDE VIEW



Recommended Land Pattern

**Tape and Reel Specifications**

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	1.68±0.10	2.18±0.10	0.85±0.10	1.50±0.10	1.75±0.10	3.50±0.05	12.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25





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