



New Product

SUM55N03-16P

Vishay Siliconix

N-Channel 30-V (D-S) 175°C MOSFET

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.016 @ $V_{GS} = 10$ V	55
	0.024 @ $V_{GS} = 4.5$ V	45

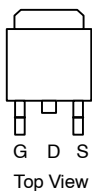
FEATURES

- TrenchFET® Power MOSFET
- 175°C Junction Temperature
- PWM Optimized
- 100% R_g Tested

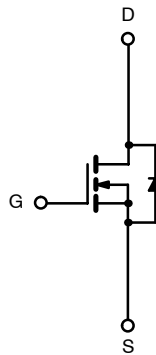
APPLICATIONS

- High-Side Core DC/DC
 - Desktop
 - Server
- DDR DC/DC Converter

TO-263



DRAIN connected to TAB



Ordering Information: SUM55N03-16P—E3 (Lead Free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	I_D	55	A
	$T_C = 100^\circ\text{C}$		39	
Pulsed Drain Current		I_{DM}	50	
Avalanche Current		I_{AR}	25	
Repetitive Avalanche Energy ^a	L = 0.1 mH	E_{AR}	31.25	mJ
Maximum Power Dissipation ^a	$T_C = 25^\circ\text{C}$	P_D	93 ^b	W
	$T_A = 25^\circ\text{C}$ ^d		3.75	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Limit	Unit
Junction-to-Ambient	PCB Mount ^c	R_{thJA}	40	$^\circ\text{C/W}$
Junction-to-Case		R_{thJC}	1.6	

Notes

- Duty cycle $\leq 1\%$.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

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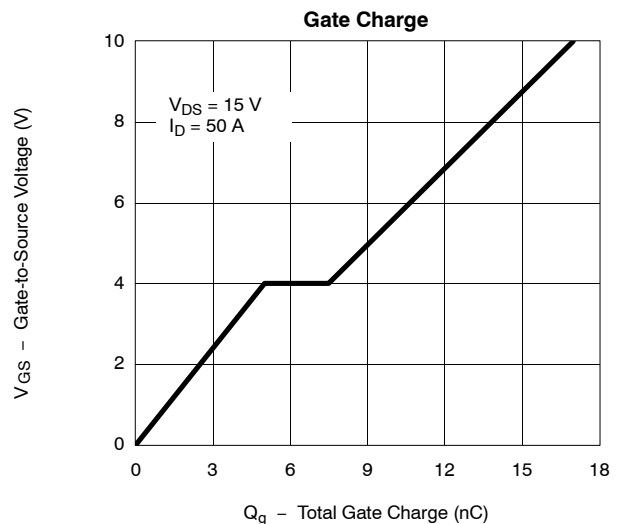
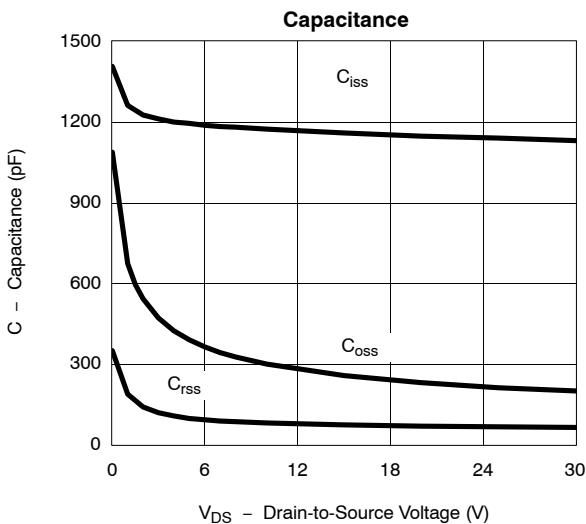
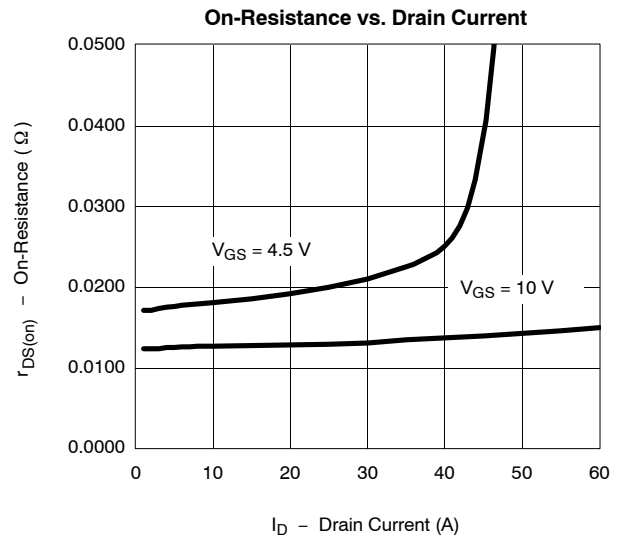
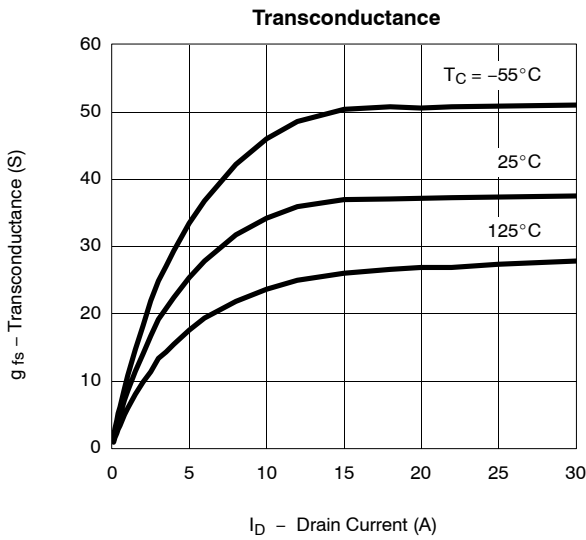
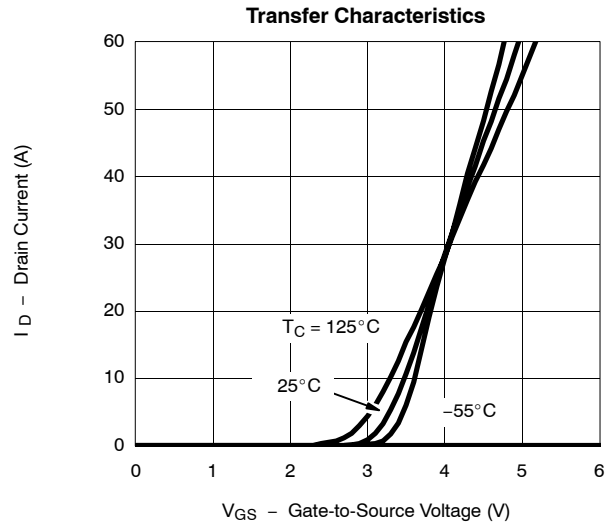
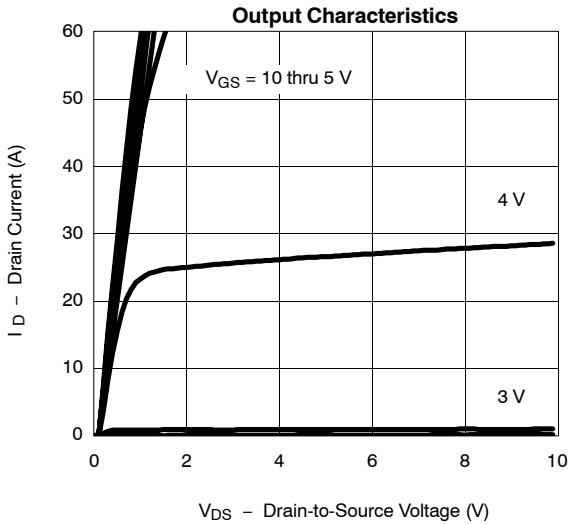
SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	30			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1		3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	50			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 15 A		0.0128	0.016	Ω
		V _{GS} = 10 V, I _D = 15 A, T _J = 125 °C			0.025	
		V _{GS} = 10 V, I _D = 15 A, T _J = 175 °C			0.031	
		V _{GS} = 4.5 V, I _D = 10 A		0.019	0.024	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	10			S
Dynamic^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz		1150		pF
Output Capacitance	C _{oss}			215		
Reverse Transfer Capacitance	C _{rss}			70		
Total Gate Charge ^b	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 50 A		17	26	nC
Gate-Source Charge ^b	Q _{gs}			5		
Gate-Drain Charge ^b	Q _{gd}			2.5		
Gate Resistance	R _g		2.7	5.5	8.25	Ω
Turn-On Delay Time ^b	t _{d(on)}	V _{DD} = 15 V, R _L = 0.3 Ω I _D ≅ 50 A, V _{GEN} = 10 V, R _g = 2.5 Ω		7	15	ns
Rise Time ^b	t _r			20	30	
Turn-Off Delay Time ^b	t _{d(off)}			25	40	
Fall Time ^b	t _f			12	20	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)^c						
Continuous Current	I _S				55	A
Pulsed Current	I _{SM}				50	
Forward Voltage ^a	V _{SD}	I _F = 20 A, V _{GS} = 0 V		1.0	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 40 A, di/dt = 100 A/μs		25	70	ns
Peak Reverse Recovery Current	I _{RM}			1.2	2.5	A
Reverse Recovery Charge	Q _{rr}			0.15	0.09	μC

Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Independent of operating temperature.
- c. Guaranteed by design, not subject to production testing.

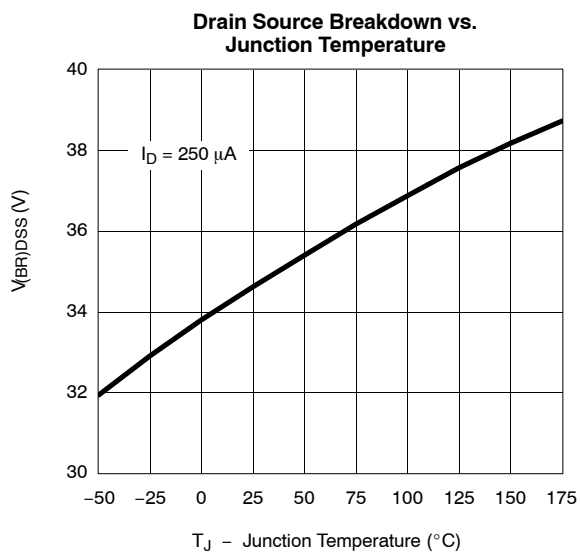
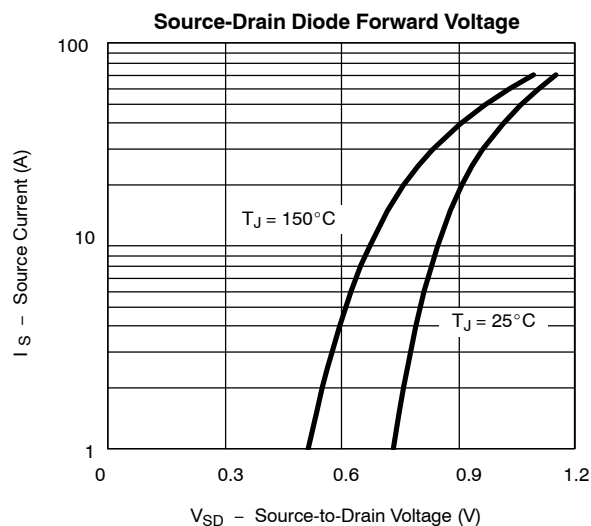
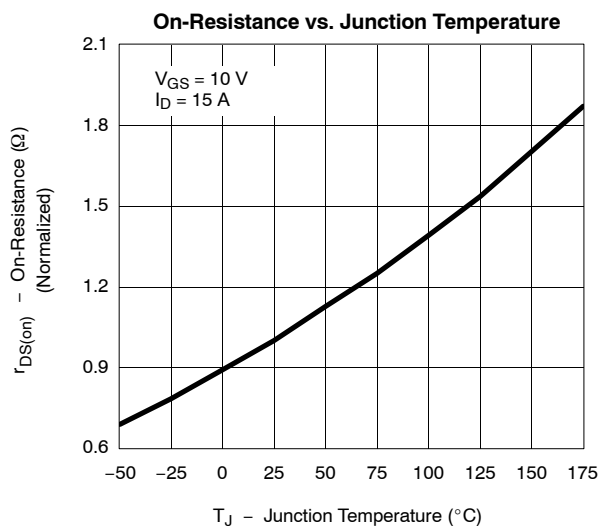


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





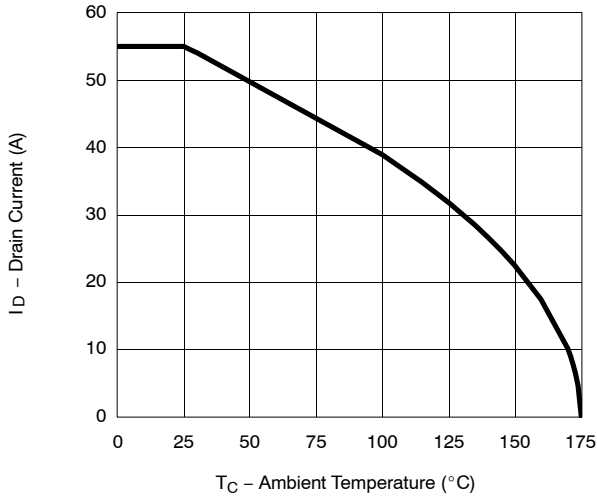
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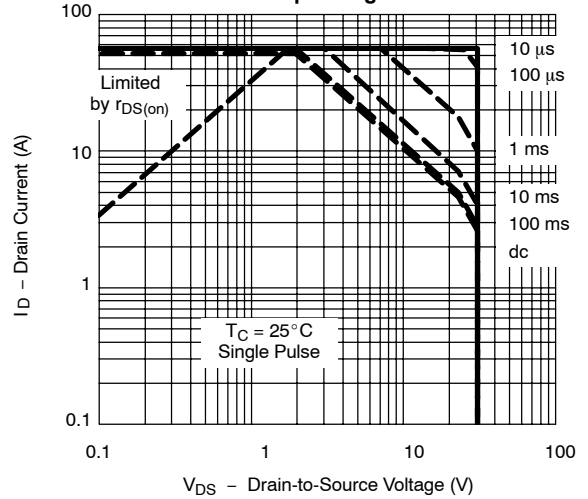


THERMAL RATINGS

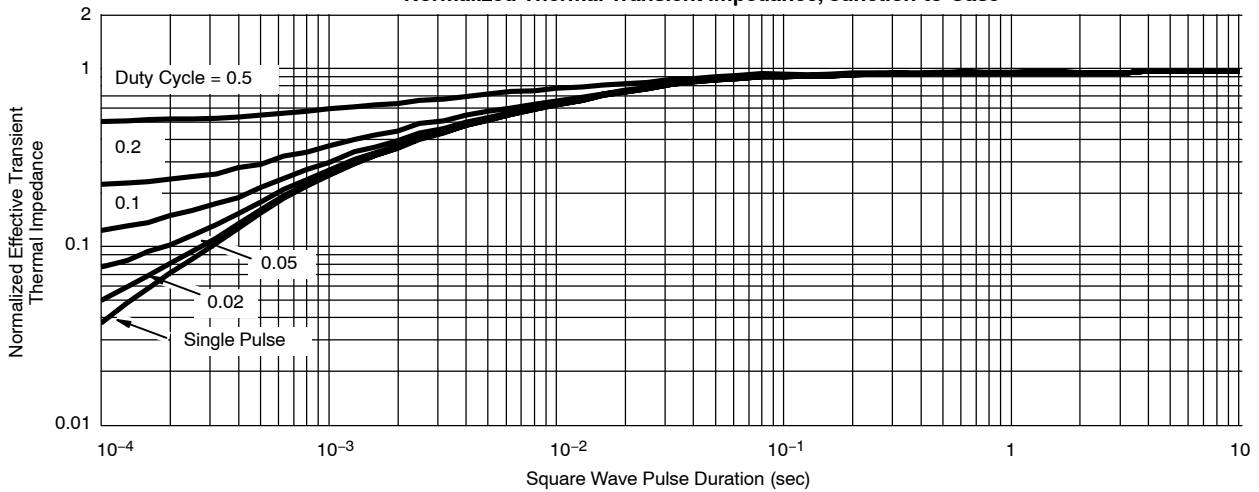
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case





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