3 VOLT ADVANCED+ STACKED CHIP SCALE PACKAGE MEMORY

16-Mbit Flash + 2-Mbit SRAM -- 28F1602C3

32-Mbit Flash + 4-Mbit SRAM -- 28F3204C3

- **Flash Memory Plus SRAM**
  - **Reduces Board Design Complexity**
- **Stacked Die, Chip Scale Package**
  - **Smallest Possible Memory Subsystem Footprint**
  - **16-Mbit Flash + 2-Mbit SRAM: 8 mm by 10 mm Area, 1.4 mm Height**
  - **32-Mbit Flash + 4-Mbit SRAM: 8 mm by 12 mm Area, 1.4 mm Height**
- **Industry Compatibility**
  - **Sourcing Flexibility**
- **Advanced SRAM Technology**
  - **70 ns Access Time**
  - **Low Power Consumption with 30 mA Read and 0.5 µA Standby Current**
- **Flash Data Integrator (FDI) Software Support**
  - **Real-Time Data Storage and Code Execution from the Same Device**
  - **No Constraints on Code/Data Partition Size**
  - **Full Flash File Manager Capability**
- **3 Volt Advanced+ Boot Block Flash Memory**
  - **90 ns 16-Mb Access Time at 2.7 V**
  - **100 ns 32-Mb Access Time at 2.7 V**
  - **Low Power Consumption with 9 mA Read and 10 µA Standby Current**
  - **Improved 12 V Production Programming**
  - **Optimized Block Sizes for Code+Data Storage with 8-Kbyte Parameter and 64-Kbyte Main Blocks**
  - **Ultra Fast Program and Erase Suspend for Code+Data Storage in Real-Time Applications**
  - **Flexible, Instantaneous Individual Block Locking**
  - **128-bit Flexible Protection Register**
  - **Minimum 100,000 Erase Cycles per Block**
  - **Manufactured on 0.25 µ ETOX™ VI Flash Technology with a Path to 0.18 µ Process**
- **Extended Temperature Operation**
  - **–40 °C to +85 °C**

The 3 Volt Advanced+ Stacked Chip Scale Package (Stacked-CSP) memory delivers a feature-rich solution for low-power applications. Stacked-CSP memory devices incorporate flash memory and static RAM in one package with low voltage capability to achieve the smallest system memory solution form-factor together with high-speed, low-power operations. The flash memory offers a protection register and flexible block locking to enable next generation security capability. Combined with the Intel-developed Flash Data Integrator (FDI) software, the Stacked-CSP memory provides you with a cost-effective, flexible, code plus data storage solution.

June 1999

Order Number: 290666-003

CONTENTS

PRODUCT PREVIEW

REVISION HISTORY

Date of Revision	Version	Description
03/30/1999	-001	Original version
04/26/99	-002	Corrected title headings in Appendix B Removed reference to 8-Mbit devices, Appendix B, Table B7, Device Geometry Definition Corrected 4-Mb SRAM I_{CC2} specification
06/15/99	-003	Removed extra SRAM standby mode Clarified *Operating Mode* Table (Section 4.1.2) Clarified *Locking Operations Flowchart* (Appendix A)

1.0 INTRODUCTION

This document contains the specifications for the 3 Volt Advanced+ Stacked Chip Scale Package (Stacked-CSP) memory. These memories are stacked memory solutions with 32-MB flash memory and 4-MB SRAM or 16-MB flash memory and 2-MB SRAM.

Throughout this document, the term “2.7 V” refers to the full voltage range 2.7 V–3.3 V (except where noted otherwise) and “F-V_{PP} = 12 V” refers to 12 V ±5%.

1.1 Product Overview

The Intel® Stacked-CSP memory provides secure low-voltage memory solutions for portable applications. This memory family combines two memory technologies, flash memory and SRAM, in one package. The flash memory delivers enhanced security features, a block locking capability that allows instant locking/unlocking of any flash block with zero-latency, and a 128-bit protection register that enable unique device identification, to meet the needs of next generation portable applications.

Discrete supply balls provide single voltage read, program, and erase capability at 2.7 V while also allowing 12 V F-V_{PP} for faster production flash programming. The improved 12 V production programming feature reduce external logic and simplifies board designs when combining 12 V production programming with 2.7 V in-field programming capability.

The 3 Volt Advanced+ Stacked-CSP memory products are available in the following densities:

- 16-Mbit flash memories organized as 1024 Kwords of 16 bits each with 2-Mbit SRAM memories organized as 128Kwords of 16 bits each.
- 32-Mbit flash memories organized as 2048 Kwords of 16 bits each with 4-Mbit SRAM memories organized as 256-Kwords of 16 bits each.

The flash has eight 8-KB parameter blocks located at either the top (denoted by -T suffix) or the bottom (-B suffix) of the address map in order to accommodate different microprocessor protocols for kernel code location. The remaining flash memory is grouped into 64-Kbyte main blocks. All flash blocks can be locked or unlocked instantly to provide complete protection for code or data (see Section 6.0 for details).

The Command User Interface (CUI) serves as the interface between the microprocessor or microcontroller and the internal operation of the flash memory. The flash’s internal Write State Machine (WSM) automatically executes the algorithms and timings necessary for program and erase operations, including verification, thereby unburdening the microprocessor or microcontroller.

The flash’s status register indicates the status of the WSM by signifying block erase or word program completion and status.

Flash program and erase automation allows program and erase operations to be executed using an industry-standard two-write command sequence to the CUI. Program operations are performed in word increments. Erase operations erase all locations within a block simultaneously. Both program and erase operations can be suspended by the system software in order to read from any other flash block. In addition, data can be programmed to another flash block during an erase suspend.

The 3 Volt Advanced+ Stacked-CSP memories offer two low-power savings features: Automatic Power Savings (APS) for flash memory and standby mode for flash and SRAM. The device automatically enters APS mode following the completion of a read cycle from the flash memory. Standby mode is initiated when the system deselects the device by driving F-CE# and S-CS_1# or S-CS_2 inactive. Power savings features significantly reduce power consumption.

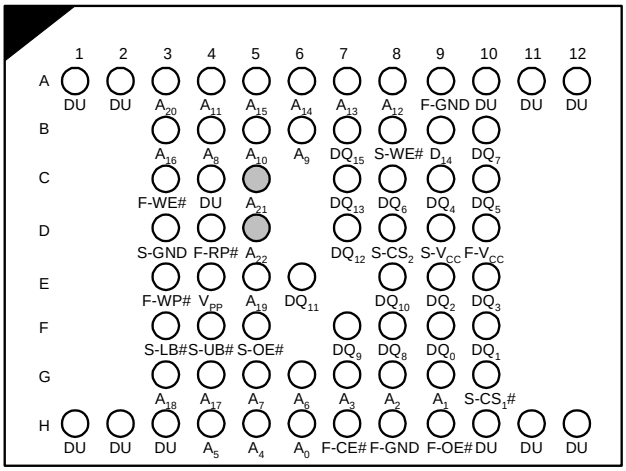
The flash memory can be reset by lowering F-RP# to GND. This provides CPU-memory reset synchronization and additional protection against bus noise that may occur during system reset and power-up/down sequences.

PRODUCT PREVIEW

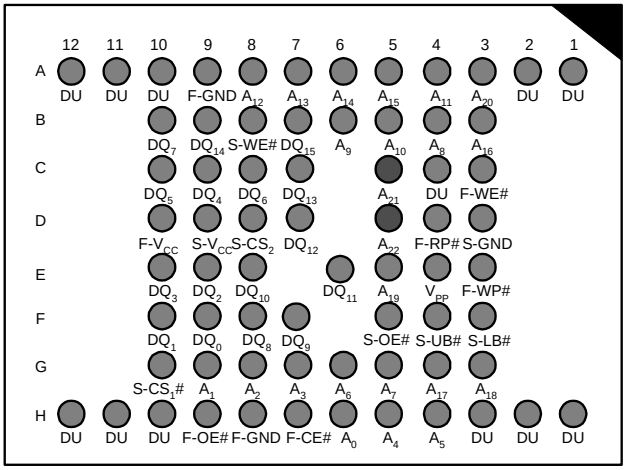
For complete current and voltage specifications, refer to Section 9.

2.0 PACKAGE BALLOUTS

This section provides device ball descriptions and package ballouts for the 3 Volt Advanced+ Stacked-CSP memory, which is available in a 72-ball (Figure 1) package. This family of products provides upgrade paths up to 32-Mbit flash memory with 4-Mbit static RAM density.



Top View, Balls Down



Bottom View, Balls Up

NOTE:

1. The upper address line, A_{20}, for the 32-Mbit flash with 4-Mbit SRAM device is defined. Flash upgrade address lines are also shown for A_{21} (64-Mbit flash) and A_{22} (128-Mbit flash) as well. In both the 32-Mbit flash with 4-Mbit SRAM and the 16-Mbit flash with 2-Mbit SRAM; 66 balls are populated (A_{21} and A_{22} are not populated).

Figure 1. 72-Ball Stacked Chip Scale Package

Table 1. 3 Volt Advanced+ Stacked-CSP Ball Descriptions

Symbol	Type	Name and Function
A_0–A_{20}	INPUT	**ADDRESS INPUTS** for memory addresses. Addresses are internally latched during a program or erase cycle. Flash: 16-Mbit x 16, A[0-19]; 32-Mbit x 16, A[0-20] SRAM: 2-Mbit x 16, A[0-16]; 4-Mbit x 16, A[0-17]
DQ_0–DQ_{15}	INPUT / OUTPUT	**DATA INPUTS/OUTPUTS:** Inputs array data for SRAM write operations and on the second F-CE# and F-WE# cycle during a flash Program command. Inputs commands to the flash's Command User Interface when F-CE# and F-WE# are active. Data is internally latched. Outputs array, configuration and status register data. The data balls float to tri-state when the chip is de-selected or the outputs are disabled.
F-CE#	INPUT	**FLASH CHIP ENABLE:** Activates the flash internal control logic, input buffers, decoders and sense amplifiers. F-CE# is active low. F-CE# high de-selects the flash memory device and reduces power consumption to standby levels.
S-CS_1#	INPUT	**SRAM CHIP SELECT1:** Activates the SRAM internal control logic, input buffers, decoders and sense amplifiers. S-CS_1# is active low. S-CS_1# high de-selects the SRAM memory device and reduces power consumption to standby levels.
S-CS_2	INPUT	**SRAM CHIP SELECT2:** Activates the SRAM internal control logic, input buffers, decoders and sense amplifiers. S-CS_2 is active high. S-CS_2 low de-selects the SRAM memory device and reduces power consumption to standby levels.
F-OE#	INPUT	**FLASH OUTPUT ENABLE:** Enables flash's outputs through the data buffers during a read operation. F-OE# is active low.
S-OE#	INPUT	**SRAM OUTPUT ENABLE:** Enables SRAM's outputs through the data buffers during a read operation. S-OE# is active low.
F-WE#	INPUT	**FLASH WRITE ENABLE:** Controls writes to flash's command register and memory array. F-WE# is active low. Addresses and data are latched on the rising edge of the second F-WE# pulse.
S-WE#	INPUT	**SRAM WRITE ENABLE:** Controls writes to the SRAM memory array. S-WE# is active low.
S-UB#	INPUT	**SRAM UPPER BYTE ENABLE:** Enable the upper bytes for SRAM (DQ_8–DQ_{15}). S-UB# is active low.
S-LB#	INPUT	**SRAM LOWER BYTE ENABLE:** Enable the lower bytes for SRAM (DQ_0–DQ_7). S-LB# is active low.
F-RP#	INPUT	**FLASH RESET/DEEP POWER-DOWN:** Uses two voltage levels (V_{IL}, V_{IH}) to control reset/deep power-down mode. **When F-RP# is at logic low, the device is in reset/deep power-down mode**, which drives the outputs to High-Z, resets the Write State Machine, and minimizes current levels (I_{CCD}). **When F-RP# is at logic high, the device is in standard operation**. When F-RP# transitions from logic-low to logic-high, the device resets all blocks to locked and defaults to the read array mode.

Table 1. 3 Volt Advanced+ Stacked-CSP Ball Descriptions (Continued)

Symbol	Type	Name and Function
F-WP#	INPUT	**FLASH WRITE PROTECT:** Controls the lock-down function of the flexible Locking feature. **When F-WP# is a logic low, the lock-down mechanism is enabled** and blocks marked lock-down cannot be unlocked through software. **When F-WP# is logic high, the lock-down mechanism is disabled** and blocks previously locked-down are now locked and can be unlocked and locked through software. After F-WP# goes low, any blocks previously marked lock-down revert to that state. See Section 6.0 for details on block locking.
F-V_{CC}	SUPPLY	**FLASH POWER SUPPLY:** [2.7 V–3.3 V] Supplies power for device operations.
S-V_{CC}	SUPPLY	**SRAM POWER SUPPLY:** [2.7 V–3.3 V] Supplies power for device operations.
F-V_{PP}	INPUT / SUPPLY	**FLASH PROGRAM/ERASE POWER SUPPLY:** [1.65 V–3.3 V or 11.4 V–12.6 V] Operates as a input at logic levels to control complete flash protection. Supplies power for accelerated flash program and erase operations in 12 V ± 5% range. This ball cannot be left floating. **Lower** F-$V_{PP} \leq V_{PPLK}$**, to protect all contents** against Program and Erase commands. **Set** F-V_{PP} **=** F-V_{CC} **for in-system read, program and erase operations**. In this configuration, F-V_{PP} can drop as low as 1.65 V to allow for resistor or diode drop from the system supply. Note that if F-V_{PP} is driven by a logic signal, V_{IH} = 1.65 V. That is, F-V_{PP} must remain above 1.65 V to perform in-system flash modifications. **Raise** F-V_{PP} **to 12 V ± 5% for faster program and erase** in a production environment. Applying 12 V ± 5% to F-V_{PP} can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. F-V_{PP} may be connected to 12 V for a total of 80 hours maximum.
F-GND	SUPPLY	**FLASH GROUND:** For all internal circuitry. All ground inputs **must** be connected.
S-GND	SUPPLY	**SRAM GROUND:** For all internal circuitry. All ground inputs **must** be connected.
DU		**DON'T USE: Do not drive ball to V_{IH} or V_{IL}. Leave unconnected.**

3.0 STACKED CHIP SCALE PACKAGE ORGANIZATION

The 3 Volt Advanced+ Stacked-CSP contains a flash and a SRAM component. The flash device is asymmetrically-blocked to enable system integration of code and data storage in a single device. Each flash block can be erased independently of the others up to 100,000 times. For the address locations of each flash block, see the memory maps in Appendix C.

Figure 2 illustrates the Stacked-CSP block diagram.

4.0 PRINCIPLES OF OPERATION

The 3 Volt Advanced+ Stacked-CSP incorporates flash and SRAM in a single package.

The flash memory utilizes a CUI and automated algorithms to simplify program and erase operations. The internal algorithms are controlled by an internal WSM. The CUI handles the interface to the data and address latches, as well as system status requests during WSM operation.

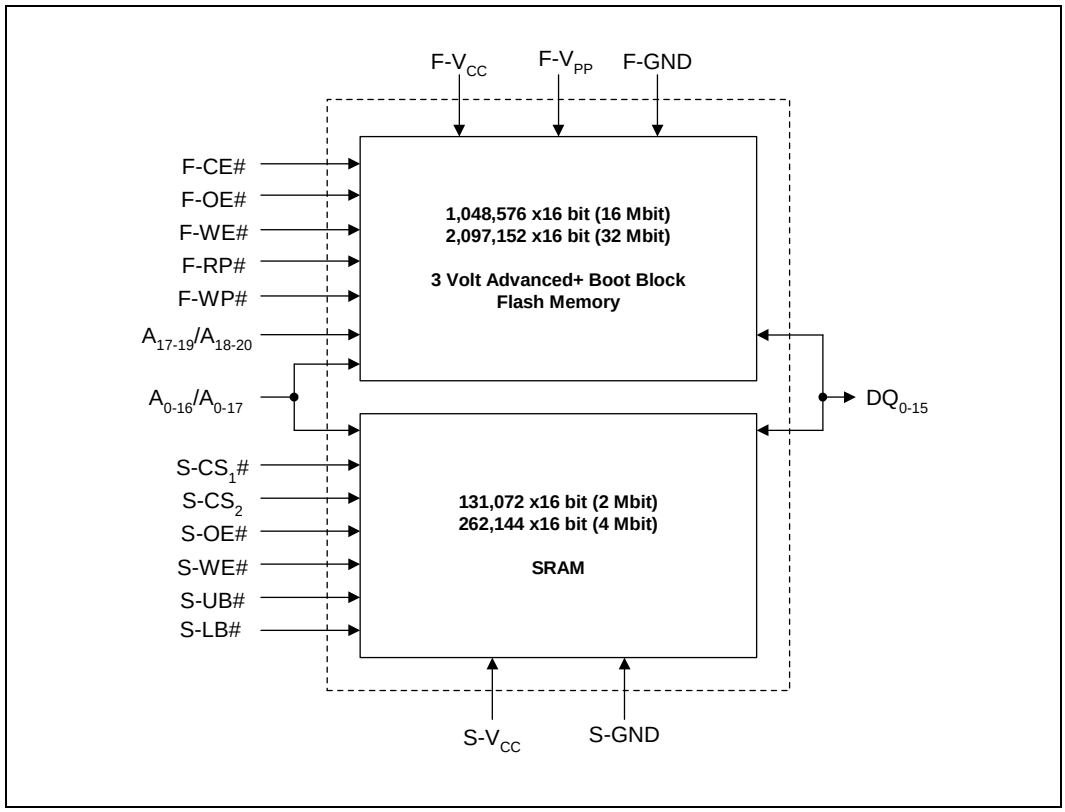


Figure 2. 3 Volt Advanced+ Stacked Chip Scale Package Block Diagram

4.1 Bus Operation

The 3 Volt Advanced+ Stacked-CSP memory devices read, program and erase in-system via the local CPU or microcontroller. All bus cycles to or from the Stacked-CSP conform to standard microcontroller bus cycles. Four control balls dictate the data flow in and out of the flash component: F-CE#, F-OE#, F-WE# and F-RP#. Four control balls handle the data flow in and out of the SRAM component: $S\text{-}CS_1\#$, $S\text{-}CS_2$, S-OE#, and S-WE# These bus operations are summarized in Tables 2 and 3.

4.1.1 READ

The SRAM has one read mode while the flash memory has four read modes: read array, read configuration, read status and read query. These flash memory read modes are accessible independent of the F-V_{PP} voltage. The appropriate read mode command must be issued to the flash memory to enter the corresponding mode. Upon initial device power-up or after exit from reset, the flash device automatically defaults to read array mode.

F-CE# and F-OE# must be driven active to obtain data from the flash component. at the outputs. $S\text{-}CS_1\#$, $S\text{-}CS_2$, and S-OE# must be driven active to obtain data from the SRAM device. For all reads operations, F-WE#, S-WE# and F-RP# must be at V_{IH}. Figure 6 illustrates a flash read cycle.

4.1.2 OUTPUT DISABLE

With F-OE# and S-OE# inactive, the Stacked-CSP outputs are disabled. Output balls are placed in a high-impedance state.

Table 2. Flash Operating Mode(1)

Mode	Note	F-RP#	F-CE#	F-OE#	F-WE#	DQ_{0-15}
Flash Read	2,3	V_{IH}	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Flash Output Disable	2	V_{IH}	V_{IL}	V_{IH}	V_{IH}	High Z
Flash Write	4	V_{IH}	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Flash Standby	2	V_{IH}	V_{IH}	X	X	High Z
Flash Reset	2,5	V_{IL}	X	X	X	High Z
SRAM Read	2	X	V_{IH}	X	X	High Z
SRAM Output Disable	2	X	V_{IH}	X	X	High Z
SRAM Write	2	X	V_{IH}	X	X	High Z

NOTES:

1. F-CE# and S-CS_1# and S-CS_2 should not be asserted at the same time. Flash device cannot be accessed while SRAM is in data retention mode.
2. X must be V_{IL}, V_{IH} for control balls and addresses.
3. See DC Characteristics for V_{PPLK}, V_{PP1}, V_{PP2}, V_{PP3}, voltages.
4. Table 5 describes valid Input Data (D_{IN}) during a flash command sequence.
5. F-RP# must be at GND ± 0.2 V to meet the maximum deep power-down current specified.

Table 3. SRAM Operating Mode(1)

Mode	Note	S-CS_1#	S-CS_2	S-OE#	S-WE#	S-UB#	S-LB#	DQ_{0-15}
Flash Read	2,3,5	V_{IH}	V_{IL}	X	X	X	X	High Z
Flash Output Disable	2,5	V_{IH}	V_{IL}	X	X	X	X	High Z
Flash Write	4	V_{IH}	V_{IL}	V_{IH}	V_{IL}	X	X	High Z
Flash Standby	2,5	V_{IH}	X	X	X	X	X	High Z
SRAM Read	2	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	D_{OUT}
SRAM Output Disable	2	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	High Z
SRAM Write	2	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	D_{IN}
SRAM Standby	2	V_{IH}	X	X	X	X	X	High Z
SRAM Standby	2	X	V_{IL}	X	X	X	X	High Z
SRAM Standby	2	X	X	X	X	V_{IH}	V_{IH}	High Z

NOTES:

1. F-CE# and S-CS_1# and S-CS_2 should not be asserted at the same time. Flash device cannot be accessed while SRAM is in data retention mode.
2. X must be V_{IL}, V_{IH} for control balls and addresses.
3. See DC Characteristics for V_{PPLK}, V_{PP1}, V_{PP2}, V_{PP3}, voltages.
4. Table 5 describes valid Input Data (D_{IN}) during a flash command sequence.
5. SRAM can be placed in standby by asserting S-CS_1# to V_{IH} or S-CS_2 to V_{IL}.

4.1.3 STANDBY

With F-CE# and S-SC_1# or S-SC_2 inactive, the Stacked-CSP enters a standby mode, which substantially reduces device power consumption. In standby, outputs are placed in a high-impedance state independent of F-OE# and S-OE#. If the flash is deselected during a program or erase operation, the flash continues to consume active power until the program or erase operation is complete.

4.1.4 RESET

The flash memory supports a reset signal, F-RP. From read mode, F-RP# at V_{IL} for time t_{PLPH} deselects the memory, places output drivers in a high-impedance state, and turns off all internal circuits. After return from reset, a time t_{PHQV} is required until the initial read access outputs are valid. A delay (t_{PHWL} or t_{PHEL}) is required after return from reset before a write can be initiated. After this wake-up interval, normal operation is restored. The flash device resets to read array mode, the status register is set to 80H, and all blocks are locked. This case is shown in Figure 8A.

If F-RP# is taken low for time t_{PLPH} during a flash program or erase operation, the operation will be aborted and the memory contents at the aborted location (for a program) or block (for an erase) are no longer valid, since the data may be partially erased or written. The abort process goes through the following sequence: When F-RP# goes low, the device shuts down the operation in progress, a process which takes time t_{PLRH} to complete. After this time t_{PLRH}, the part will either reset to read array mode (if F-RP# has gone high during t_{PLRH}, Figure 8B) or enter reset mode (if F-RP# is still logic low after t_{PLRH}, Figure 8C). In both cases, after returning from an aborted operation, the relevant time t_{PHQV} or t_{PHWL}/t_{PHEL} must be waited before a read or write operation is initiated, as discussed in the previous paragraph. However, in this case, these delays are referenced to the end of t_{PLRH} rather than when F-RP# goes high.

As with any automated device, it is important to assert F-RP# during system reset. When the system comes out of reset, processor expects to read from the flash memory. Automated flash memories provide status information when read during program or block erase operations. If a CPU reset occurs with no flash memory reset, proper CPU initialization may not occur because the flash memory may be providing status information instead of array data. Intel® Flash memories allow proper CPU initialization following a system reset through the use of the F-RP# input. In this application, F-RP# is controlled by the same RESET# signal that resets the system CPU.

4.1.5 WRITE

Writes to flash take place when both F-CE# and F-WE# are low and F-OE# is high. Writes to SRAM take place when both S-CS_1# and S-WE# are low and S-OE# and S-SC_2 are high. Commands are written to the flash memory's Command User Interface (CUI) using standard microprocessor write timings to control flash operations. The CUI does not occupy an addressable memory location within the flash component. The address and data buses are latched on the rising edge of the second F-WE# or F-CE# pulse, whichever occurs first. Figure 7 illustrates a program and erase operation. The available commands are shown in Table 5.

5.0 FLASH MEMORY MODES OF OPERATION

The flash memory has four read modes: read array, read configuration, read status, and read query. The write modes are program and erase. Three additional modes (erase suspend to program, erase suspend to read and program suspend to read) are available only during suspended operations. These modes are reached using the commands summarized in Table 5.

5.1 Read Array

When F-RP# transitions from V_{IL} (reset) to V_{IH}, the device defaults to read array mode and will respond to the read control inputs without any additional CUI commands.

In addition, the address of the desired location must be applied to the address balls. If the device is not in read array mode, as would be the case after a program or erase operation, the Read Array command (FFH) must be written to the CUI before array reads can take place.

5.2 Read Configuration

The read configuration mode outputs the manufacturer/device identifier. The device is switched to this mode by writing the read configuration command (90H). Once in this mode,

read cycles from addresses shown in Table 4 retrieve the specified information. To return to read array mode, write the Read Array command (FFH).

The Read Configuration mode outputs three types of information: the manufacturer/device identifier, the block locking status, and the protection register. The device is switched to this mode by writing the Read Configuration command (90H). Once in this mode, read cycles from addresses shown in Table 4 retrieve the specified information. To return to read array mode, write the Read Array command (FFH).

Table 4. Read Configuration Table

Item	Address	Data
Manufacturer Code (x16)	00000	0089
Device ID (See Appendix G)	00001	ID
Block Lock Configuration[2]	XX002[(1)]	LOCK
• Block Is Unlocked		DQ_0 = 0
• Block Is Locked		DQ_0 = 1
• Block Is Locked-Down		DQ_1 = 1
Protection Register Lock[3]	80	PR-LK
Protection Register (x16)	81-88	PR

NOTES:

1. "XX" specifies the block address of lock configuration being read.
2. See Section 6.4 for valid lock status outputs.
3. See Section 7.0 for protection register information.
4. Other locations within the configuration address space are reserved by Intel for future use.

5.3 Read Status Register

The status register indicates the status of device operations, and the success/failure of that operation. The Read Status Register (70H) command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the array, issue a Read Array (FFH) command.

The status register bits are output on DQ_0–DQ_7. The upper byte, DQ_8–DQ_{15}, outputs 00H during a Read Status Register command.

The contents of the status register are latched on the falling edge of F-OE# or F-CE#, whichever occurs last. This prevents possible bus errors which might occur if status register contents change while being read. F-CE# or F-OE# must be toggled with each subsequent status read, or the status register will not indicate completion of a program or erase operation.

When the WSM is active, SR.7 will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the desired operation (see Table 6).

5.3.1 CLEARING THE STATUS REGISTER

The WSM sets status bits 1 through 7 to "1," and clears bits 2, 6 and 7 to "0," but cannot clear status bits 1 or 3 through 5 to "0." Because bits 1, 3, 4 and 5 indicate various error conditions, these bits can only be cleared through the use of the Clear Status Register (50H) command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple blocks in sequence) before reading the status register to determine if an error occurred during that series. Clear the status register before beginning another command or sequence. Note that the Read Array command must be issued before data can be read from the memory array. Resetting the device also clears the status register.

5.4 Read Query

The read query mode outputs Common Flash Interface (CFI) data when the device is read. This can be accessed by writing the Read Query Command (98H). The CFI data structure contains information such as block size, density, command set and electrical specifications. Once in this mode, read cycles from addresses shown in Appendix B retrieve the specified information. To return to read array mode, write the Read Array command (FFH).

5.5 Program Mode

Programming is executed using a two-write sequence. The Program Setup command (40H) is written to the CUI followed by a second write which specifies the address and data to be programmed. The WSM will execute a sequence of internally timed events to program desired bits of the addressed location, then verify the bits are sufficiently programmed. Programming the memory results in specific bits within an address location

being changed to a “0.” If the user attempts to program “1”s, the memory cell contents do not change and no error occurs.

The status register indicates programming status: while the program sequence executes, status bit 7 is “0.” The status register can be polled by toggling either F-CE# or F-OE#. While programming, the only valid commands are Read Status Register, Program Suspend, and Program Resume.

When programming is complete, the program status bits should be checked. If the programming operation was unsuccessful, bit SR.4 of the status register is set to indicate a program failure. If SR.3 is set then F-V_{PP} was not within acceptable limits, and the WSM did not execute the program command. If SR.1 is set, a program operation was attempted on a locked block and the operation was aborted.

The status register should be cleared before attempting the next operation. Any CUI instruction can follow after programming is completed; however, to prevent inadvertent status register reads, be sure to reset the CUI to read array mode.

5.5.1 SUSPENDING AND RESUMING PROGRAM

The Program Suspend command halts an in-progress program operation so that data can be read from other locations of memory. Once the programming process starts, writing the Program Suspend command to the CUI requests that the WSM suspend the program sequence (at predetermined points in the program algorithm). The device continues to output status register data after the Program Suspend command is written. Polling status register bits SR.7 and SR.2 will determine when the program operation has been suspended (both will be set to “1”). t_{WHRH1}/t_{EHRH1} specify the program suspend latency.

A Read Array command can now be written to the CUI to read data from blocks other than that which is suspended. The only other valid commands, while program is suspended, are Read Status Register, Read Configuration, Read Query, and Program Resume. After the Program Resume command is written to the flash memory, the WSM will continue with the programming process and status register bits SR.2 and SR.7 will automatically be cleared. The device automatically outputs status register data when read (see Figure 16 in Appendix A, *Program Suspend/Resume Flowchart*) after the Program Resume command is written. F-V_{PP} must remain at the same F-V_{PP} level used for program while in program suspend mode. F-RP# must also remain at V_{IH}.

5.6 Erase Mode

To erase a block, write the Erase Set-up and Erase Confirm commands to the CUI, along with an address identifying the block to be erased. This address is latched internally when the Erase Confirm command is issued. Block erasure results in all bits within the block being set to “1.” Only one block can be erased at a time. The WSM will execute a sequence of internally timed events to program all bits within the block to “0,” erase all bits within the block to “1,” then verify that all bits within the block are sufficiently erased. While the erase executes, status bit 7 is a “0.”

When the status register indicates that erasure is complete, check the erase status bit to verify that the erase operation was successful. If the Erase operation was unsuccessful, SR.5 of the status register will be set to a “1,” indicating an erase failure. If F-V_{PP} was not within acceptable limits after the Erase Confirm command was issued, the WSM will not execute the erase sequence; instead, SR.5 of the status register is set to indicate an erase error, and SR.3 is set to a “1” to identify that F-V_{PP} supply voltage was not within acceptable limits.

After an erase operation, clear the status register (50H) before attempting the next operation. Any CUI instruction can follow after erasure is completed; however, to prevent inadvertent status register reads, it is advisable to place the flash in read array mode after the erase is complete.

5.6.1 SUSPENDING AND RESUMING ERASE

Since an erase operation requires on the order of seconds to complete, an Erase Suspend command is provided to allow erase-sequence interruption in order to read data from or program data to another block in memory. Once the erase sequence is started, writing the Erase Suspend command to the CUI suspends the erase sequence at a predetermined point in the erase algorithm. The status register will indicate if/when the erase operation has been suspended. Erase suspend latency is specified by t_{WHRH2}/t_{EHRH2}.

A Read Array/Program command can now be written to the CUI to read/program data from/to blocks other than that which is suspended. This nested Program command can subsequently be suspended to read yet another location. The only valid commands while erase is suspended are Read Status Register, Read Configuration, Read Query, Program Setup, Program Resume, Erase Resume, Lock Block, Unlock Block and Lock-Down Block. During erase suspend mode, the chip can be placed in a pseudo-standby mode by taking F-CE# to V_{IH}. This reduces active current consumption.

Erase Resume continues the erase sequence when F-CE# = V_{IL}. As with the end of a standard erase operation, the status register must be read and cleared before the next instruction is issued.

Table 5. Flash Memory Command Bus Definitions

Command	Notes	First Bus Cycle			Second Bus Cycle		
		Oper	Addr	Data	Oper	Addr	Data
Read Array	4	Write	X	FFH			
Read Configuration	2, 4	Write	X	90H	Read	IA	ID
Read Query	2, 4	Write	X	98H	Read	QA	QD
Read Status Register	4	Write	X	70H	Read	X	SRD
Clear Status Register	4	Write	X	50H			
Program	3,4	Write	X	40H/10H	Write	PA	PD
Block Erase/Confirm	4	Write	X	20H	Write	BA	D0H
Program/Erase Suspend	4	Write	X	B0H			
Program/Erase Resume	4	Write	X	D0H			
Lock Block	4	Write	X	60H	Write	BA	01H
Unlock Block	4	Write	X	60H	Write	BA	D0H
Lock-Down Block	4	Write	X	60H	Write	BA	2FH
Protection Program	4	Write	X	C0H	Write	PA	PD

X = Don't Care PA = Prog Addr BA = Block Addr IA = Identifier Addr. QA = Query Addr.
SRD = Status Reg. Data PD = Prog Data ID = Identifier Data QD = Query Data

NOTES:

1. Bus operations are defined in Table 2.
2. Following the Read Configuration or Read Query commands, read operations output device configuration or CFI query information, respectively.
3. Either 40H or 10H command is valid, but the Intel standard is 40H.
4. When writing commands, the upper data bus [DQ8–DQ15] should be either V_{IL} or V_{IH}, to minimize current draw.

Table 6. Flash Memory Register Bit Definition

WSMS	ESS	ES	PS	VPPS	PSS	BLS	R
7	6	5	4	3	2	1	0

	NOTES:
SR.7 WRITE STATE MACHINE STATUS 1 = Ready (WSMS) 0 = Busy	Check Write State Machine bit first to determine Word Program or Block Erase completion, before checking Program or Erase Status bits.
SR.6 = ERASE-SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed	When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1." ESS bit remains set to "1" until an Erase Resume command is issued.
SR.5 = ERASE STATUS (ES) 1 = Error In Block Erase 0 = Successful Block Erase	When this bit is set to "1," WSM has applied the max. number of erase pulses and is still unable to verify successful block erasure.
SR.4 = PROGRAM STATUS (PS) 1 = Error in Programming 0 = Successful Programming	When this bit is set to "1," WSM has attempted but failed to program a word/byte.
SR.3 = F-V_{PP} STATUS (VPPS) 1 = F-V_{PP} Low Detect, Operation Abort 0 = F-V_{PP} OK	The F-V_{PP} status bit does not provide continuous indication of V_{PP} level. The WSM interrogates F-V_{PP} level only after the Program or Erase command sequences have been entered, and informs the system if F-V_{PP} has not been switched on. The F-V_{PP} is also checked before the operation is verified by the WSM. The F-V_{PP} status bit is not guaranteed to report accurate feedback between V_{PPLK} and V_{PP1} min.
SR.2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed	When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to "1." PSS bit remains set to "1" until a Program Resume command is issued.
SR.1 = BLOCK LOCK STATUS 1 = Prog/Erase attempted on a locked block; Operation aborted. 0 = No operation to locked blocks	If a program or erase operation is attempted to one of the locked blocks, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode.
SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)	This bit is reserved for future use and should be masked out when polling the status register.

NOTE:

1. A Command Sequence Error is indicated when both SR.4, SR.5 and SR.7 are set.

6.0 FLASH MEMORY FLEXIBLE BLOCK LOCKING

The Intel 3 Volt Advanced+ Stacked-CSP products offer an instant, individual block locking scheme that allows any block to be locked or unlocked with no latency, enabling instant code and data protection.

This locking scheme offers two levels of protection. The first level allows software-only control of block locking (useful for data blocks that change frequently), while the second level requires hardware interaction before locking can be changed (useful for code blocks that change infrequently).

The following sections will discuss the operation of the locking system. The term “state [XYZ]” will be used to specify locking states; e.g., “state [001],” where X = value of WP#, Y = bit DQ_1 of the Block Lock status register, and Z = bit DQ_0 of the Block Lock status register. Table 8 defines all of these possible locking states.

6.1 Locking Operation

The following concisely summarizes the locking functionality.

- All blocks power-up locked, then can be unlocked or locked with the Unlock and Lock commands.
- The Lock-Down command locks a block and prevents it from being unlocked when WP# = 0.
  - — When WP# = 1, Lock-Down is overridden and commands can unlock/lock locked-down blocks.
  - — When WP# returns to 0, locked-down blocks return to Lock-Down.
  - — Lock-Down is cleared only when the device is reset or powered-down.

The locking status of each block can set to Locked, Unlocked, and Lock-Down, each of which will be described in the following sections. A comprehensive state table for the locking functions is shown in Table 8, and a flowchart for locking operations is shown in Figure 19.

6.2 Locked State

The default status of all blocks upon power-up or reset is locked (states [001] or [101]). Locked blocks are fully protected from alteration. Any program or erase operations attempted on a locked block will return an error on bit SR.1 of the status register. The status of a locked block can be changed to Unlocked or Lock-Down using the appropriate software commands. An Unlocked block can be locked by writing the Lock command sequence, 60H followed by 01H.

6.3 Unlocked State

Unlocked blocks (states [000], [100], [110]) can be programmed or erased. All unlocked blocks return to the Locked state when the device is reset or powered down. The status of an unlocked block can be changed to Locked or Locked-Down using the appropriate software commands. A Locked block can be unlocked by writing the Unlock command sequence, 60H followed by D0H.

6.4 Lock-Down State

Blocks that are Locked-Down (state [011]) are protected from program and erase operations (just like Locked blocks), but their protection status cannot be changed using software commands alone. A Locked or Unlocked block can be Locked-down by writing the Lock-Down command sequence, 60H followed by 2FH. Locked-Down blocks revert to the Locked state when the device is reset or powered down.

The Lock-Down function is dependent on the WP# input ball. When WP# = 0, blocks in Lock-Down [011] are protected from program, erase, and lock status changes. When WP# = 1, the Lock-Down function is disabled ([111]) and locked-down blocks can be individually unlocked by software command to the [110] state, where they can be erased and programmed. These blocks can then be re-locked [111] and unlocked [110] as desired while WP# remains high. When WP# goes low, blocks that were previously locked-down return to the Lock-Down state [011] regardless of any changes made while WP# was high. Device reset or power-down resets all blocks, including those in Lock-Down, to Locked state.

6.5 Reading a Block's Lock Status

The lock status of every block can be read in the configuration read mode of the device. To enter this mode, write 90H to the device. Subsequent reads at Block Address + 00002 will output the lock status of that block. The lock status is represented by the lowest two output balls, DQ_0 and DQ_1. DQ_0 indicates the Block Lock/Unlock status and is set by the Lock command and cleared by the Unlock command. It is also automatically set when entering Lock-Down. DQ_1 indicates Lock-Down status and is set by the Lock-Down command. It cannot be cleared by software, only by device reset or power-down.

Table 7. Block Lock Status

Item	Address	Data
Block Lock Configuration	XX002	LOCK
• Block Is Unlocked		$DQ_0 = 0$
• Block Is Locked		$DQ_0 = 1$
• Block Is Locked-Down		$DQ_1 = 1$

6.6 Locking Operation During Erase Suspend

Changes to block lock status can be performed during an erase suspend by using the standard locking command sequences to unlock, lock, or lock-down a block. This is useful in the case when another block needs to be updated while an erase operation is in progress.

To change block locking during an erase operation, first write the erase suspend command (B0H), then check the status register until it indicates that the erase operation has been suspended. Next write the desired lock command sequence to a block and the lock status will be changed. After completing any desired lock, read, or program operations, resume the erase operation with the Erase Resume command (D0H).

If a block is locked or locked-down during a suspended erase of the same block, the locking status bits will be changed immediately, but when the erase is resumed, the erase operation will complete.

Locking operations cannot be performed during a program suspend.

6.7 Status Register Error Checking

Using nested locking or program command sequences during erase suspend can introduce ambiguity into status register results.

Since locking changes are performed using a two cycle command sequence, e.g., 60H followed by 01H to lock a block, following the Configuration Setup command (60H) with an invalid command will produce a lock command error (SR.4 and SR.5 will be set to 1) in the status register. If a lock command error occurs during an erase suspend, SR.4 and SR.5 will be set to 1, and will remain at 1 after the erase is resumed. When erase is complete, any possible error during the erase cannot be detected via the status register because of the previous locking command error.

A similar situation happens if an error occurs during a program operation error nested within an erase suspend.

7.0 FLASH MEMORY 128-BIT PROTECTION REGISTER

The 3 Volt Advanced+ Stacked-CSP architecture includes a 128-bit protection register than can be used to increase the security of a system design. For example, the number contained in the protection register can be used to "mate" the flash component with other system components such as the CPU or ASIC, preventing device substitution.

The 128-bits of the protection register are divided into two 64-bit segments. One of the segments is programmed at the Intel factory with a unique 64-bit number, which is unchangeable. The other segment is left blank for customer designs to program as desired. Once the customer segment is programmed, it can be locked to prevent reprogramming.

Table 8. Block Locking State Transitions

Current State				Erase/Prog	Lock Command Input Result [Next State]		
WP#	DQ_1	DQ_0	Name	Allowed?	Lock	Unlock	Lock-Down
0	0	0	"Unlocked"	Yes	Goes To [001]	No Change	Goes To [011]
0	0	1	"Locked" (Default)	No	No Change	Goes To [000]	Goes To [011]
0	1	1	"Locked-Down"	No	No Change	No Change	No Change
1	0	0	"Unlocked"	Yes	Goes To [101]	No Change	Goes To [111]
1	0	1	"Locked"	No	No Change	Goes To [100]	Goes To [111]
1	1	0	Lock-Down Disabled	Yes	Goes To [111]	No Change	Goes To [111]
1	1	1	Lock-Down Disabled	No	No Change	Goes To [110]	No Change

NOTES:

1. In this table, the notation [XYZ] denotes the locking state of a block, where X = WP#, Y = DQ_1, and Z = DQ_0. The current locking state of a block is defined by the state of WP# and the two bits of the block lock status (DQ_0, DQ_1). DQ_0 indicates if a block is locked (1) or unlocked (0). DQ_1 indicates if a block has been locked-down (1) or not (0).
2. At power-up or device reset, all blocks default to Locked state [001] (if WP# = 0). Holding WP# = 0 is the recommended default.
3. The "Erase/Program Allowed?" column shows whether erase and program operations are enabled (Yes) or disabled (No) in that block's current locking state.
4. The "Lock Command Input Result [Next State]" column shows the result of writing the three locking commands (Lock, Unlock, Lock-Down) in the current locking state. For example, "Goes To [001]" would mean that writing the command to a block in the current locking state would change it to [001].

7.1 Reading the Protection Register

The protection register is read in the configuration read mode. The device is switched to this mode by writing the Read Configuration command (90H). Once in this mode, read cycles from addresses shown in Appendix E retrieve the specified information. To return to read array mode, write the Read Array command (FFH).

7.2 Programming the Protection Register

The protection register bits are programmed using the two-cycle Protection Program command. The 64-bit number is programmed 16 bits at a time for word-wide parts. First write the Protection Program Setup command, C0H. The next write to the device will latch in address and data and program the specified location. The allowable addresses are shown in Appendix E. See Figure 20 for the *Protection Register Programming Flowchart*.

Any attempt to address Protection Program commands outside the defined protection register address space will result in a status register error (program error bit SR.4 will be set to 1). Attempting to program or to a previously locked protection register segment will result in a status register error (program error bit SR.4 and lock error bit SR.1 will be set to 1).

7.3 Locking the Protection Register

The user-programmable segment of the protection register is lockable by programming Bit 1 of the PR-LOCK location to 0. Bit 0 of this location is programmed to 0 at the Intel factory to protect the unique device number. This bit is set using the Protection Program command to program “FFFD” to the PR-LOCK location. After these bits have been programmed, no further changes can be made to the values stored in the protection register. Protection Program commands to a locked section will result in a status register error (program error bit SR.4 and Lock Error bit SR.1 will be set to 1). Protection register lockout state is not reversible.

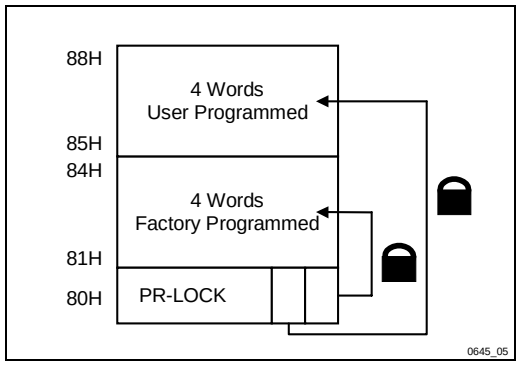


Figure 3. Protection Register Memory Map

8.0 FLASH MEMORY PROGRAM AND ERASE VOLTAGES

Intel 3 Volt Advanced+ Stacked-CSP products provide in-system programming and erase in the 1.65 V–3.3 V range. For fast production programming, it also includes a low-cost, backward-compatible 12 V programming feature.

8.1 Improved 12 Volt Production Programming

When F-V_{PP} is between 1.65 V and 3.3 V, all program and erase current is drawn through the F-V_{CC} signal. Note that if F-V_{PP} is driven by a logic signal, V_{IH} min = 1.65 V. That is, F-V_{PP} must remain above 1.65 V to perform in-system flash modifications. When F-V_{PP} is connected to a 12 V power supply, the device draws program and erase current directly from the F-V_{PP} signal. This eliminates the need for an external switching transistor to control the voltage F-V_{PP}. Figure 12 shows examples of how the flash power supplies can be configured for various usage models.

The 12 V F-V_{PP} mode enhances programming performance during the short period of time typically found in manufacturing processes; however, it is not intended for extended use. 12 V may be applied to F-V_{PP} during program and erase operations for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. F-V_{PP} may be connected to 12 V for a total of 80 hours maximum. Stressing the device beyond these limits may cause permanent damage.

8.2 F-$V_{PP} \leq V_{PPLK}$ for Complete Protection

In addition to the flexible block locking, the F-V_{PP} programming voltage can be held low for absolute hardware write protection of all blocks in the flash device. When F-V_{PP} is below V_{PPLK}, any program or erase operation will result in a error, prompting the corresponding status register bit (SR.3) to be set.

9.0 ELECTRICAL SPECIFICATIONS

NOTICE: This datasheet contains preliminary information on new products in the design phase of production. Do not finalize a design with this information. Revised information will be published when the product is available. Verify with your local Intel Sales office that you have the latest datasheet before finalizing a design.

9.1 Absolute Maximum Ratings*

Extended Operating Temperature

During Read ..... –40 °C to +85 °C

During Flash Block Erase and Program ..... –40 °C to +85 °C

Temperature Under Bias..... –40 °C to +85 °C

Storage Temperature ..... –65 °C to +125 °C

Voltage on Any Ball (except F-V_{CC}/S-V_{CC} and F-V_{PP}) with Respect to GND ..... –0.5 V to +3.3 V[1]

F-V_{PP} Voltage (for Block Erase and Program) with Respect to GND .....–0.5 V to +13.5 V[1,2,4]

F-V_{CC}/S-V_{CC} Supply Voltage with Respect to GND ..... –0.2 V to +3.3 V[1]

Output Short Circuit Current..... 100 mA[3]

** WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may effect device reliability.*

NOTES:

1. Minimum DC voltage is –0.5 V on input/output balls. During transitions, this level may undershoot to –2.0 V for periods < 20 ns. Maximum DC voltage on input/output balls is F-V_{CC}/S-V_{CC} + 0.5 V which, during transitions, may overshoot to F-V_{CC}/S-V_{CC} + 2.0 V for periods < 20 ns.
2. Maximum DC voltage on F-V_{PP} may overshoot to +14.0 V for periods < 20 ns.
3. Output shorted for no more than one second. No more than one output shorted at a time.
4. F-V_{PP} voltage is normally 1.65 V–3.3 V. Connection to supply of 11.4 V–12.6 V can only be done for 1000 cycles on the main blocks and 2500 cycles on the parameter blocks during program/erase. F-V_{PP} may be connected to 12 V for a total of 80 hours maximum. See Section 8.0 for details.

9.2 Operating Conditions

Table 9. Temperature and Voltage Operating Conditions

Symbol	Parameter	Notes	Min	Max	Units
T_A	Operating Temperature		–40	+85	°C
V_{CC1}	F-V_{CC}/S-V_{CC} Supply Voltage	1	2.7	3.3	Volts
V_{CC2}		1	3.0	3.3	
V_{PP1}	Supply Voltage	1	1.65	3.3	Volts
V_{PP2}		1, 2	11.4	12.6	Volts
Cycling	Block Erase Cycling	2	100,000		Cycles

NOTES:

1. F-V_{CC}/S-V_{CC} must share the same supply when they are in the V_{CC1} range.
2. Applying F-V_{PP} = 11.4 V–12.6 V during a program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. F-V_{PP} may be connected to 12 V for a total of 80 hours maximum. See Section 8.1 for details.

9.3 Capacitance

$T_A = 25$ °C, f = 1 MHz

Sym	Parameter	Notes	Typ	Max	Units	Conditions
C_{IN}	Input Capacitance	1	16	18	pF	$V_{IN} = 0$ V
C_{OUT}	Output Capacitance	1	20	22	pF	$V_{OUT} = 0$ V

NOTE:

1. Sampled, not 100% tested.

9.4 DC Characteristics

Sym	Parameter	Device	Note	2.7 V–3.3 V Typ	2.7 V–3.3 V Max	Unit	Test Conditions
I_{LI}	Input Load Current	Flash/SRAM	1,7		± 2	µA	F-V_{CC}/S-V_{CC} = V_{CC1} Max $V_{IN} = V_{CC1}$ Max or GND
I_{LO}	Output Leakage Current	Flash/ SRAM	1,7	0.2	± 10	µA	F-V_{CC}/S-V_{CC} = V_{CC1} Max $V_{IN} = V_{CC1}$ Max or GND
I_{CCS}	V_{CC} Standby Current	Flash	1	10	25	µA	F-V_{CC} = V_{CC1} Max F-CE# = F-RP# = V_{CC1} F-WP# = V_{CC1} or GND $V_{IN} = V_{CC1}$ Max or GND
		2-Mb SRAM	1	0.5	10	µA	S-V_{CC} = V_{CC1} Max S-CS#$_1$ = V_{CC}, S-CS_2 = V_{CC} or S-CS_2 = GND $V_{IN} = V_{CC1}$ Max or GND
		4-Mb SRAM	1	0.5	20	µA	
I_{CCD}	V_{CC} Deep Power-Down Current	Flash	1,7	7	20	µA	F-V_{CC} = V_{CC}Max $V_{IN} = V_{CC1}$ Max or GND F-RP# = GND ± 0.2 V
I_{CC}	Operating Power Supply Current (cycle time = 1 µs)	2-Mb SRAM	1	3	7	mA	I_{IO} = 0 mA, S-CS#$_1$ = V_{IL} S-CS_2 = S-WE# = V_{IH} $V_{IN} = V_{IL}$ or V_{IH}
		4-Mb SRAM	1	8	10	mA	
I_{CC2}	Operating Power Supply Current (min cycle time)	2-Mb SRAM	1	30	40	mA	Cycle time = Min, 100% duty, I_{IO} = 0 mA, S-CS#$_1$ = V_{IL}, S-CS_2 = V_{IH}, $V_{IN} = V_{IL}$ or V_{IH}
		4-Mb SRAM	1	30	45	mA	
I_{CCR}	V_{CC} Read Current	Flash	1,5, 7	9	18	mA	F-V_{CC} = V_{CC1}Max F-OE# = V_{IH}, F-CE# = V_{IL} f = 5 MHz, I_{OUT} = 0 mA $V_{IN} = V_{IL}$ or V_{IH}

9.4 DC Characteristics (continued)

Sym	Parameter	Device	Note	2.7 V–3.3 V		Unit	Test Conditions
				Typ	Max		
I_{CCW}	V_{CC} Program Current	Flash	1,4	18	55	mA	F-V_{PP} = V_{PP1} Program in Progress
				8	15	mA	F-V_{PP} = V_{PP2} (12 V) Program in Progress
I_{CCE}	V_{CC} Erase Current	Flash	1,4	16	45	mA	F-V_{PP} = V_{PP1} Erase in Progress
				8	15	mA	F-V_{PP} = V_{PP2} (12 V) Erase in Progress
I_{CCES}	V_{CC} Erase Suspend Current	Flash	1,2,4	10	25	µA	F-CE# = V_{IH}, Erase Suspend in Progress
I_{CCWS}	V_{CC} Program Suspend Current	Flash	1,2,4	10	25	µA	F-CE# = V_{IH}, Program Suspend in Progress
I_{PPD}	F-V_{PP} Deep Power-Down Current	Flash	1	0.2	5	µA	F-RP# = GND ± 0.2 V F-V_{PP} ≤ V_{CC1}
I_{PPS}	F-V_{PP} Standby Current	Flash	1	0.2	5	µA	F-V_{PP} ≤ V_{CC1}
I_{PPR}	F-V_{PP} Read Current	Flash	1	2	±15	µA	F-V_{PP} ≤ V_{CC1}
			1,4	50	200	µA	F-V_{PP} ≥ V_{CC1}
I_{PPW}	F-V_{PP} Program Current	Flash	1,4	0.05	0.1	mA	F-V_{PP} =V_{PP1} Program in Progress
				8	22	mA	F-V_{PP} = V_{PP2} (12 V) Program in Progress
I_{PPE}	F-V_{PP} Erase Current	Flash	1,4	0.05	0.1	mA	F-V_{PP} = V_{PP1} Program in Progress
				8	22	mA	F-V_{PP} = V_{PP2} (12 V) Program in Progress
I_{PPES}	F-V_{PP} Erase Suspend Current	Flash	1,4	0.2	5	µA	F-V_{PP} = V_{PP1} Erase Suspend in Progress
				50	200	µA	F-V_{PP} = V_{PP2} (12 V) Erase Suspend in Progress
I_{PPWS}	F-V_{PP} Program Suspend Current	Flash	1,4	0.2	5	µA	F-V_{PP} = V_{PP1} Program Suspend in Progress
				50	200	µA	F-V_{PP} = V_{PP2} (12 V) Program Suspend in Progress

9.4 DC Characteristics (continued)

Sym	Parameter	Device	Note	2.7 V–3.3 V		Unit	Test Conditions
				Min	Max		
V_{IL}	Input Low Voltage	Flash/ SRAM		–0.4	V_{CC} *0.22	V	
V_{IH}	Input High Voltage	Flash/ SRAM		2.2	V_{CC} +0.3	V	
V_{OL}	Output Low Voltage	Flash/ SRAM	7	–0.10	0.10	V	F-V_{CC}/S-V_{CC} = V_{CC1} Min I_{OL} = 100 µA
V_{OH}	Output High Voltage	Flash/ SRAM	7	V_{CC} – 0.1		V	F-V_{CC}/S-V_{CC} = V_{CC1} Min I_{OH} = –100 µA
V_{PPLK}	F-V_{PP} Lock-Out Voltage	Flash	3		1.0	V	Complete Write Protection
V_{PP1}	F-V_{PP} during Program / Erase	Flash	3	1.65	3.3	V	
V_{PP2}	Operations		3,6	11.4	12.6		
V_{LKO}	V_{CC} Prog/Erase Lock Voltage	Flash		1.5		V	

NOTES:

1. All currents are in RMS unless otherwise noted. Typical values at nominal F-V_{CC}/S-V_{CC}, T_A = +25 °C.
2. I_{CCES} and I_{CCWS} are specified with device de-selected. If device is read while in erase suspend, current draw is sum of I_{CCES} and I_{CCR}. If the device is read while in program suspend, current draw is the sum of I_{CCWS} and I_{CCR}.
3. Erase and Program are inhibited when F-V_{PP} < V_{PPLK} and not guaranteed outside the valid F-V_{PP} ranges of V_{PP1} and V_{PP2}.
4. Sampled, not 100% tested.
5. Automatic Power Savings (APS) reduces I_{CCR} to approximately standby levels in static operation (CMOS inputs).
6. Applying F-V_{PP} = 11.4 V–12.6 V during program/erase can only be done for a maximum of 1000 cycles on the main blocks and 2500 cycles on the parameter blocks. F-V_{PP} may be connected to 12 V for a total of 80 hours maximum. See Section 8.1 for details.
7. The test conditions F-V_{CC}/S-V_{CC} = V_{CC1} Min refer to the maximum or minimum V_{CC1} or V_{CC2} voltage listed at the top of each column.

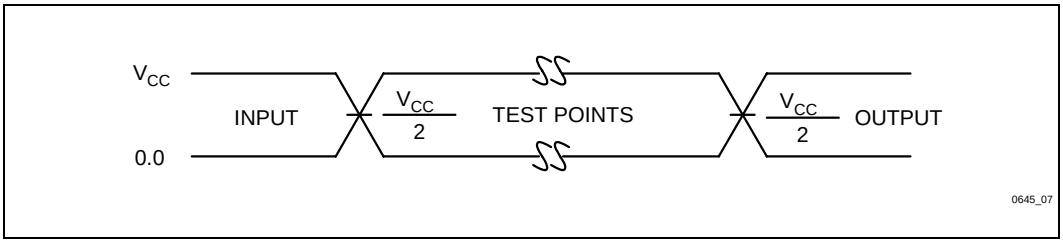


Figure 4. Input/Output Reference Waveform

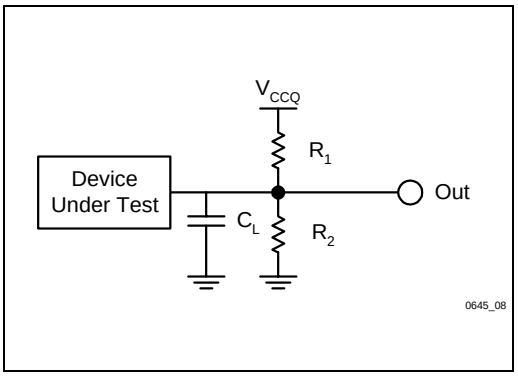


Figure 5. Test Configuration

Flash Test Configuration Component Values Table

Test Configuration	C_L (pF)	R_1 (Ω)	R_2 (Ω)
2.7 V–3.3 V Standard Test	50	25K	25K

NOTE:
C_L includes jig capacitance.

9.5 Flash AC Characteristics—Read Operations[1, 4]—Extended Temperature

			Density	16 Mbit								
			Product	–90				–110				
			Volt	3.0 V–3.3 V		2.7 V–3.3 V		3.0 V–3.3 V		2.7 V–3.3 V		
#	Sym	Parameter	Note	Min	Max	Min	Max	Min	Max	Min	Max	Unit
R1	t_{AVAV}	Read Cycle Time		80		90		100		110		ns
R2	t_{AVQV}	Address to Output Delay			80		90		100		110	ns
R3	t_{ELQV}	F-CE# to Output Delay	2		80		90		100		110	ns
R4	t_{GLQV}	F-OE# to Output Delay	2		30		30		30		30	ns
R5	t_{PHQV}	F-RP# to Output Delay			150		150		150		150	ns
R6	t_{ELQX}	F-CE# to Output in Low Z	3	0		0		0		0		ns
R7	t_{GLQX}	F-OE# to Output in Low Z	3	0		0		0		0		ns
R8	t_{EHQZ}	F-CE# to Output in High Z	3		20		20		20		20	ns
R9	t_{GHQZ}	F-OE# to Output in High Z	3		20		20		20		20	ns
R10	t_{OH}	Output Hold from Address, F-CE#, or F-OE# Change, Whichever Occurs First	3	0		0		0		0		ns

NOTES:

1. See Figure 6 *AC Waveform: Flash Read Operations*.
2. F-OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of CE# without impact on t_{ELQV}.
3. Sampled, but not 100% tested.
4. See Figure 4, *Input/Output Reference Waveform* for timing measurements and maximum allowable input slew rate.

9.5 Flash AC Characteristics—Read Operations[1, 4]—Extended Temperature, (continued)

			Density	32 Mbit								
			Product	–100[5]				–110				
			Volt	3.0 V–3.3 V		2.7 V–3.3 V		3.0 V–3.3 V		2.7 V–3.3 V		
#	Sym	Parameter	Note	Min	Max	Min	Max	Min	Max	Min	Max	Unit
R1	t_{AVAV}	Read Cycle Time		90		100		100		110		ns
R2	t_{AVQV}	Address to Output Delay			90		100		100		110	ns
R3	t_{ELQV}	F-CE# to Output Delay	2		90		100		100		110	ns
R4	t_{GLQV}	F-OE# to Output Delay	2		30		30		30		30	ns
R5	t_{PHQV}	F-RP# to Output Delay			150		150		150		150	ns
R6	t_{ELQX}	F-CE# to Output in Low Z	3	0		0		0		0		ns
R7	t_{GLQX}	F-OE# to Output in Low Z	3	0		0		0		0		ns
R8	t_{EHQZ}	F-CE# to Output in High Z	3		20		20		20		20	ns
R9	t_{GHQZ}	F-OE# to Output in High Z	3		20		20		20		20	ns
R10	t_{OH}	Output Hold from Address, F-CE#, or F-OE# Change, Whichever Occurs First	3	0		0		0		0		ns

NOTES:

1. See Figure 6 AC Waveform: Flash Read Operations.
2. F-OE# may be delayed up to t_{ELQV}–t_{GLQV} after the falling edge of F-CE# without impact on t_{ELQV}.
3. Sampled, but not 100% tested.
4. See Figure 4, Input/Output Reference Waveform for timing measurements and maximum allowable input slew rate.
5. Speed bin not initially available.

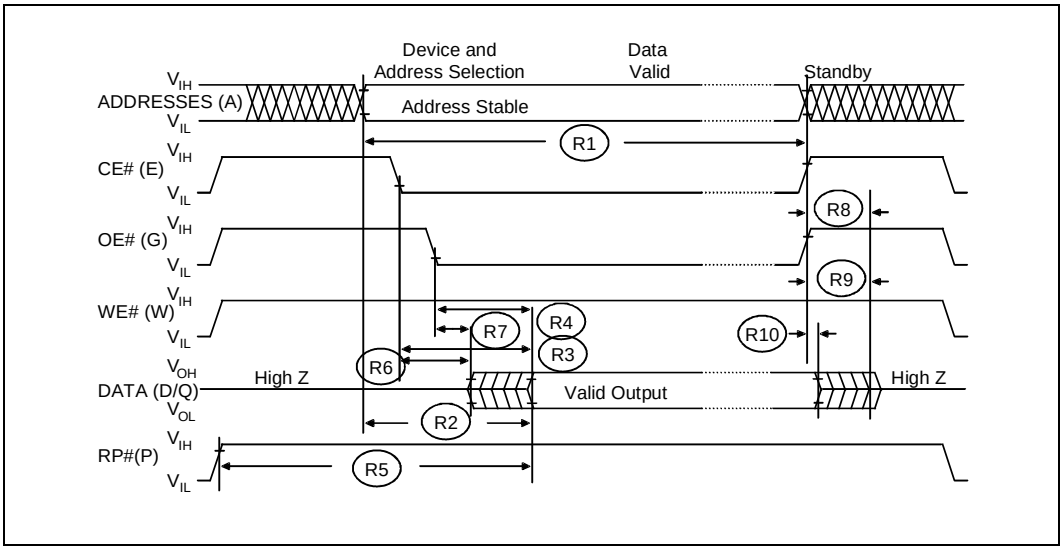


Figure 6. AC Waveform: Flash Read Operations

9.6 Flash AC Characteristics—Write Operations[1, 5, 6]—Extended Temperature

			Density	16 Mbit				32 Mbit				
			Product	–90		–110		–100		–110		
			3.0 V – 3.3 V	80		100		90		100		
			2.7 V – 3.3 V		90		110		100		110	
#	Sym	Parameter	Note	Min	Min	Min	Min	Min	Min	Min	Min	Unit
W1	t_{PHWL} / t_{PHEL}	F-RP# High Recovery to F-WE# (F-CE#) Going Low		150	150	150	150	150	150	150	150	ns
W2	t_{ELWL} t_{WLEL}	F-CE# (F-WE#) Setup to F-WE# (F-CE#) Going Low		0	0	0	0	0	0	0	0	ns
W3	t_{ELEH} t_{WLWH}	F-WE# (F-CE#) Pulse Width	4	50	60	70	70	60	70	70	70	ns
W4	t_{DVWH} t_{DVEH}	Data Setup to F-WE# (F-CE#) Going High	2	50	50	60	60	50	60	60	60	ns
W5	t_{AVWH} t_{AVEH}	Address Setup to F-WE# (F-CE#) Going High	2	50	60	70	70	60	70	70	70	ns
W6	t_{WHEH} t_{EHWH}	F-CE# (F-WE#) Hold Time from F-WE# (F-CE#) High		0	0	0	0	0	0	0	0	ns
W7	t_{WHDX} t_{EHDX}	Data Hold Time from F-WE# (F-CE#) High	2	0	0	0	0	0	0	0	0	ns
W8	t_{WHAX} t_{EHAX}	Address Hold Time from F-WE# (F-CE#) High	2	0	0	0	0	0	0	0	0	ns
W9	t_{WHWL} t_{EHEL}	F-WE# (F-CE#) Pulse Width High	4	30	30	30	30	30	30	30	30	ns
W10	t_{VPWH} t_{VPEH}	F-V_{PP} Setup to F-WE# (F-CE#) Going High	3	200	200	200	200	200	200	200	200	ns
W11	t_{QVVL}	F-V_{PP} Hold from Valid SRD	3	0	0	0	0	0	0	0	0	ns

NOTES:

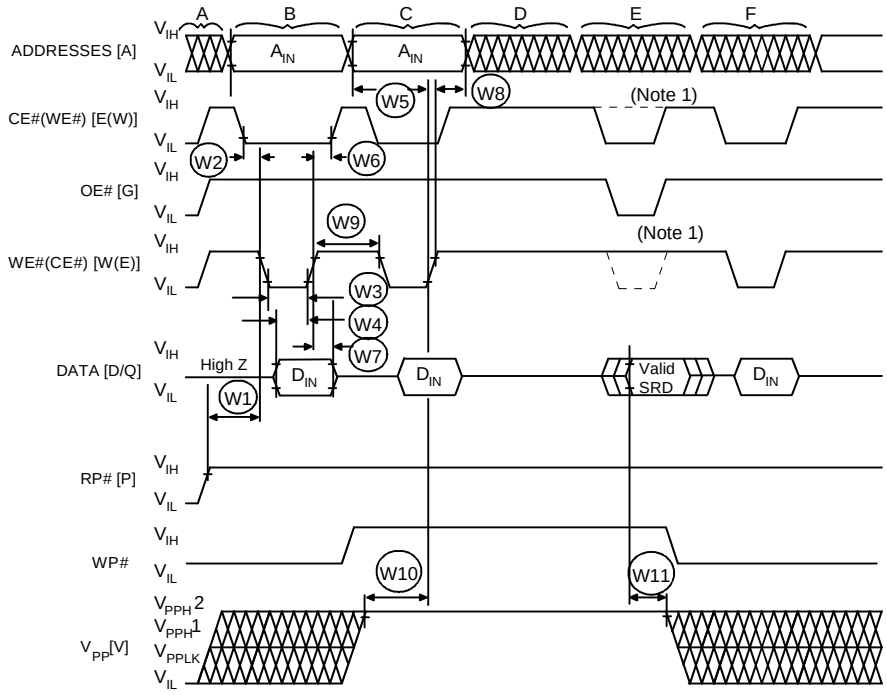
1. Write timing characteristics during erase suspend are the same as during write-only operations.
2. Refer to Table 5 for valid A_{IN} or D_{IN}.
3. Sampled, but not 100% tested.
4. Write pulse width (t_{WP}) is defined from F-CE# or F-WE# going low (whichever goes low last) to F-CE# or F-WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. Similarly, write pulse width high (t_{WPH}) is defined from F-CE# or F-WE# going high (whichever goes high first) to F-CE# or F-WE# going low (whichever goes low first). Hence, $t_{WPH} = t_{WHWL} = t_{EHEL} = t_{WHEL} = t_{EHWL}$.
5. See Figure 4, *Input/Output Reference Waveform* for timing measurements and maximum allowable input slew rate.
6. See Figure 7, *AC Waveform: Flash Program and Erase Operations.*

9.7 Flash Erase and Program Timings(1)

Symbol	Parameter	F-V_{PP} Note	1.65 V–3.3 V Typ(1)	1.65 V–3.3 V Max	11.4 V–12.6 V Typ(1)	11.4 V–12.6 V Max	Unit
t_{BWPB}	8-KB Parameter Block Program Time (Byte)	2, 3	0.16	0.48	0.08	0.24	s
	4-KW Parameter Block Program Time (Word)	2, 3	0.10	0.30	0.03	0.12	s
t_{BWMB}	64-KB Main Block Program Time (Byte)	2, 3	1.2	3.7	0.6	1.7	s
	32-KW Main Block Program Time(Word)	2, 3	0.8	2.4	0.24	1	s
t_{WHQV1} / t_{EHQV1}	Byte Program Time	2, 3	17	165	8	185	µs
	Word Program Time	2, 3	22	200	8	185	µs
t_{WHQV2} / t_{EHQV2}	8-KB Parameter Block Erase Time (Byte)	2, 3	0.5	4	0.4	4	s
	4-KW Parameter Block Erase Time (Word)	2, 3	0.5	4	0.4	4	s
t_{WHQV3} / t_{EHQV3}	64-KB Main Block Erase Time (Byte)	2, 3	1	5	0.6	5	s
	32-KW Main Block Erase Time (Word)	2, 3	1	5	0.6	5	s
t_{WHRH1} / t_{EHRH1}	Program Suspend Latency	3	5	10	5	10	µs
t_{WHRH2} / t_{EHRH2}	Erase Suspend Latency	3	5	20	5	20	µs

NOTES:

1. Typical values measured at T_A = +25 °C and nominal voltages.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.



NOTES:

1. F-CE# must be toggled low when reading Status Register Data. F-WE# must be inactive (high) when reading Status Register Data.

A. F-V_{CC} Power-Up and Standby.
B. Write Program or Erase Setup Command.
C. Write Valid Address and Data (for Program) or Erase Confirm Command.
D. Automated Program or Erase Delay.
E. Read Status Register Data (SRD): reflects completed program/erase operation.
F. Write Read Array Command.

Figure 7. AC Waveform: Flash Program and Erase Operations

9.8 Flash Reset Operations

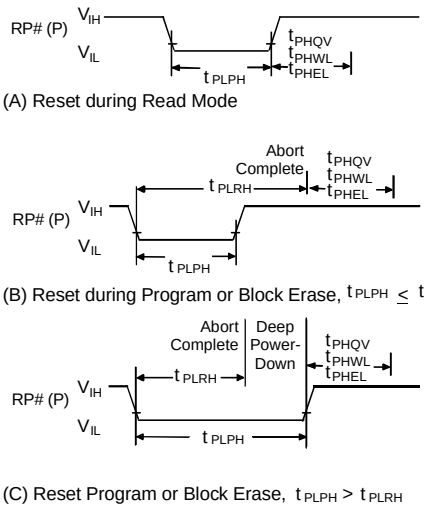


Figure 8. AC Waveform: Reset Operation

Table 10. Reset Specifications(1)

Symbol	Parameter	Notes	F-V_{CC} 2.7 V–3.3 V		Unit
			Min	Max	
t_{PLPH}	F-RP# Low to Reset during Read (If F-RP# is tied to V_{CC}, this specification is not applicable)	2,4	100		ns
t_{PLRH1}	F-RP# Low to Reset during Block Erase	3,4		22	µs
t_{PLRH2}	F-RP# Low to Reset during Program	3,4		12	µs

NOTES:

1. See Section 4.1.4 for a full description of these conditions.
2. If t_{PLPH} is < 100 ns the device may still reset but this is not guaranteed.
3. If F-RP# is asserted while a block erase or word program operation is not executing, the reset will complete within 100 ns.
4. Sampled, but not 100% tested.

9.9 SRAM AC Characteristics—Read Operations[1, 4]—Extended Temperature

#	Sym	Parameter	Density / Volt Note	2/4 Mbit / 2.7 V–3.3 V Min	2/4 Mbit / 2.7 V–3.3 V Max	Unit
R1	t_{RC}	Read Cycle Time		70	–	ns
R2	t_{AA}	Address to Output Delay		–	70	ns
R3	t_{CO1}, t_{CO2}	S-CS_1#, S-CS_2 to Output Delay		–	70	ns
R4	t_{OE}	S-OE# to Output Delay		–	35	ns
R5	t_{BA}	S-UB#, LB# to Output Delay		–	70	ns
R6	t_{LZ1}, t_{LZ2}	S-CS_1#, S-CS_2 to Output in Low Z	3	10	–	ns
R7	t_{OLZ}	S-OE# to Output in Low Z		0	–	ns
R8	t_{HZ1}, t_{HZ2}	S-CS_1#, S-CS_2 to Output in High Z	2, 3	0	25	ns
R9	t_{OHZ}	S-OE# to Output in High Z	2	0	25	ns
R10	t_{OH}	Output Hold from Address, S-CS_1#, S-CS_2, or S-OE# Change, Whichever Occurs First		0	–	ns
R11	t_{BLZ}	S-UB#, S-LB# to Output in Low Z		0	–	ns
R12	t_{BHZ}	S-UB#, S-LB# to Output in High Z		0	25	ns

NOTES:

1. See Figure 9 *AC Waveform: SRAM Read Operations*.
2. Timings of t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
3. At any given temperature and voltage condition, t_{HZ} (Max.) is less than and t_{LZ} (Max.) both for a given device and from device to device interconnection.
4. Sampled, but not 100% tested.

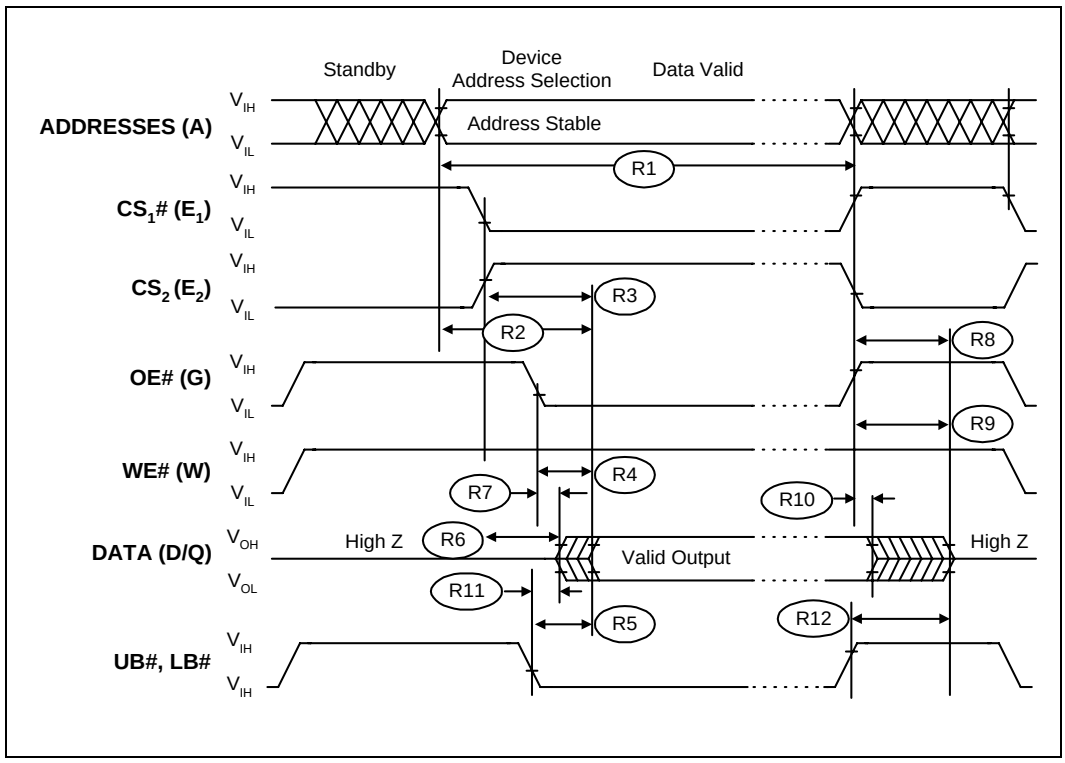


Figure 9. AC Waveform: SRAM Read Operations

9.10 SRAM AC Characteristics—Write Operations[1, 2]—Extended Temperature

#	Sym	Parameter	Density	2/4 Mbit		Unit
			Volt	2.7 V–3.3 V		
			Note	Min	Max	
W1	t_{WC}	Write Cycle Time		70	–	ns
W2	t_{AS}	Address Setup to S-WE# (S-CS_1#) and S-UB#, S-LB# Going Low	4	0	–	ns
W3	t_{WP}	S-WE# (S-CS_1#) Pulse Width	3	55	–	ns
W4	t_{DW}	Data to Write Time Overlap		30	–	ns
W5	t_{AW}	Address Setup to S-WE# (S-CS_1#) Going High		60	–	ns
W6	t_{CW}	S-CE# (S-WE#) Setup to S-WE# (S-CS_1#) Going High		60	–	ns
W7	t_{DH}	Data Hold Time from S-WE# (S-CS_1#) High		0	–	ns
W8	t_{WR}	Write Recovery	5	0	–	ns
W9	t_{BW}	S-UB#, S-LB# Setup to S-WE# (S-CS_1#) Going High		60	–	ns

NOTES:

1. See Figure 10, *AC Waveform: SRAM Write Operations*
2. A write occurs during the overlap (t_{WP}) of low S-CS_1# and low S-WE#. A write begins when S-CS_1# goes low and S-WE# goes low with asserting S-UB# or S-LB# for single byte operation or simultaneously asserting S-UB# and S-LB# for double byte operation. A write ends at the earliest transition when S-CS_1# goes high and S-WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.
3. t_{WP} is measured from S-CS_1# going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as S-CS_1# or S-WE# going high.

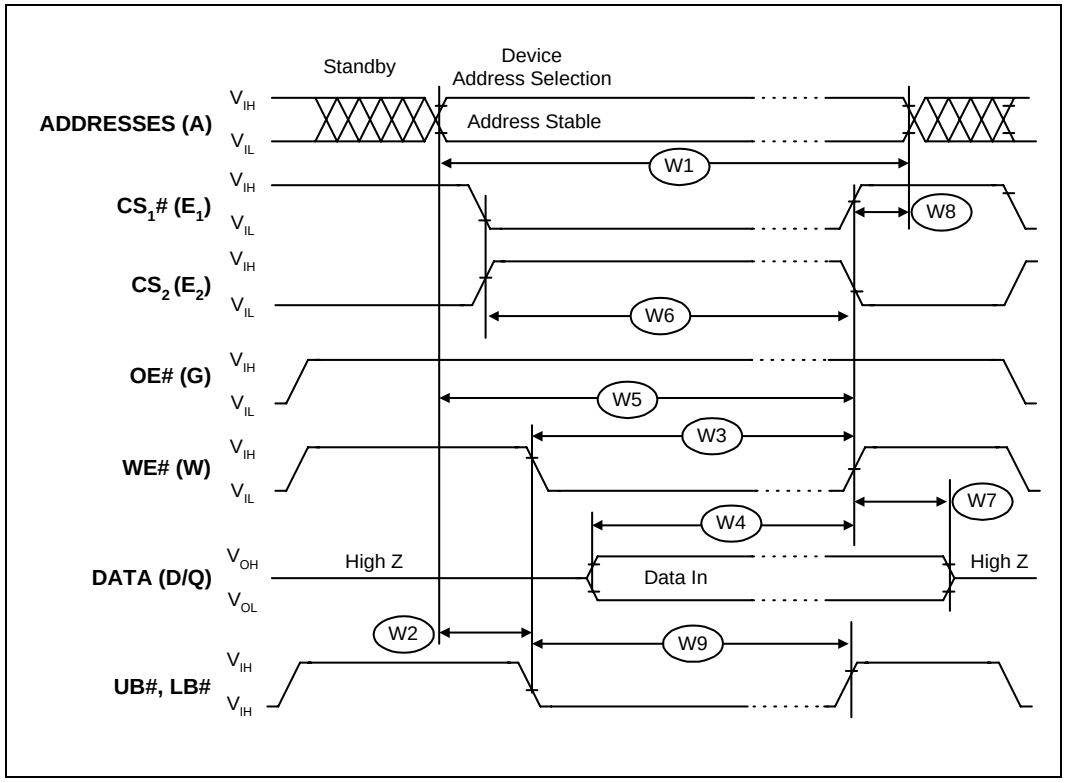


Figure 10. AC Waveform: SRAM Write Operations

9.11 SRAM Data Retention Characteristics(1) —Extended Temperature

Sym	Parameter	Note	Min	Typ	Max	Unit	Test Conditions
V_{DR}	S-V_{CC} for Data Retention	2	1.5	–	3.3	V	$CS_1\# \geq V_{CC1} - 0.2$ V
I_{DR}	Deep Retention Current	2	–	0.2	5	µA	S-V_{CC} = 1.2 V $CS_1\# \geq V_{CC1} - 0.2$ V
t_{SDR}	Data Retention Set-up Time		0	–	–	ns	See Data Retention Waveform
t_{RDR}	Recovery Time		t_{RC}	–	–	ns	

NOTES:

1. Typical values at nominal S-V_{CC}, T_A = +25 °C.
2. S-$CS_1\# \geq V_{CC1} - 0.2$ V, S-$CS_2 \geq V_{CC1} - 0.2$ V (S-CS_1# controlled) or S-$CS_2 \leq 0.2$ V (S-CS_2 controlled)

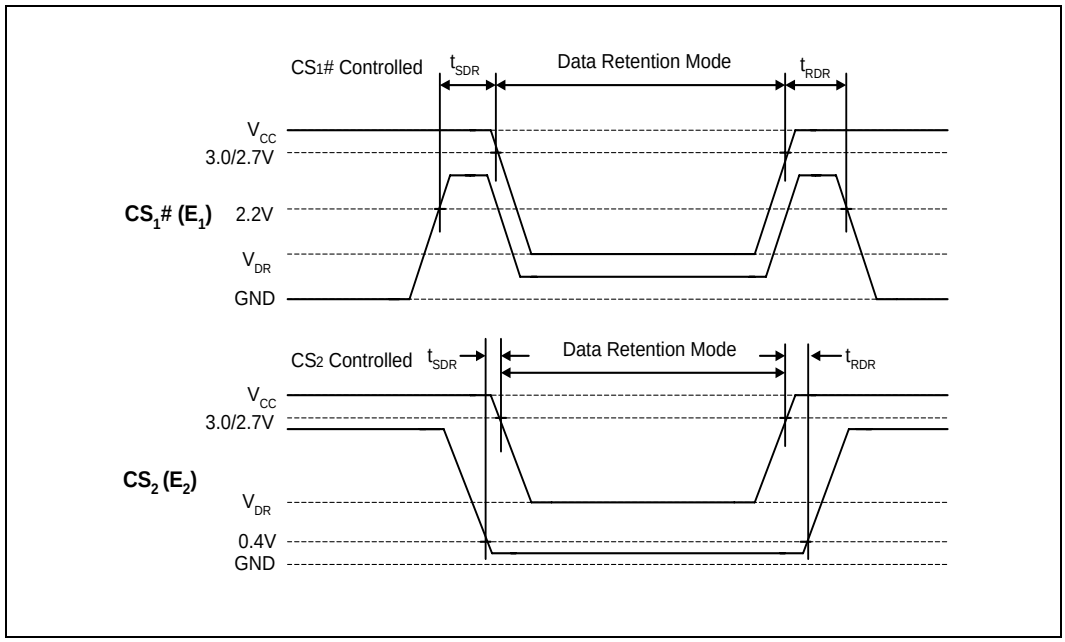


Figure 11. SRAM Data Retention Waveform

10.0 MIGRATION GUIDE INFORMATION

Typically, it is important to discuss migration compatibility between footprint between a new product and existing products. In this specific case, the Stacked CSP allows the system designer to remove two separate memory footprints for individual flash and SRAM and replace them with a single footprint, thus resulting in an overall reduction in board space required. This implies that a new printed circuit board would be used to take advantage of this feature.

Since the flash in Stacked-CSP shares the same features as the Advanced+ Boot Block Features, conversions from the Advanced Boot Block are described in *AP-658 Designing for Upgrade to the Advanced+ Boot Block Flash Memory,* order number 292216.

Please contact your local Intel representation for detailed information about specific Flash + SRAM system migrations.

11.0 SYSTEM DESIGN CONSIDERATIONS

This section contains information that would have been contained in a product design guide in earlier generations. In an effort to simplify the amount of documentation, relevant system design considerations have been combined into this document.

11.1 Background

The new Intel Advanced+ Boot Block Stacked chip scale package combines the features of the Advanced+ Boot Block flash memory architecture with a low-power SRAM to achieve an overall reduction in system board space. This enables applications to integrate security with simple software and hardware configurations, while also combining the system SRAM and flash into one common footprint. This section discusses how to take full advantage of the new 3 Volt Advanced+ Boot Block Stacked Chip Scale Package.

11.1.1 FLASH + SRAM FOOTPRINT INTEGRATION

The Stacked Chip Scale Package memory solution can be used to replace a subset of the memory subsystem within a design. Where a previous design may have used two separate footprints for SRAM and Flash, you can now replace with the industry standard I-ballout of the Stacked CSP device. This allows for an overall reduction in board space, which allows the design to integrate both the flash and the SRAM into one component.

11.1.2 ADVANCED+ BOOT BLOCK FLASH MEMORY FEATURES

Advanced+ Boot Block adds the following new features to Intel® Advanced Boot Block architecture:

- Instant, individual block locking provides software/hardware controlled, independent locking/unlocking of any block with zero latency to protect code and data.
- A 128-bit Protection Register enables system security implementations.
- Improved 12 V production programming simplifies the system configuration required to implement 12 V fast programming
- Common Flash Interface (CFI) provides component information on the chip to allow software-independent device upgrades

For more information on specific advantages of the Advanced+ Boot Block Flash Memory, please see *AP-658 Designing with the Advanced+ Boot Block Flash Memory Architecture*.

11.2 Flash Control Considerations

The flash device is protected against accidental block erasure or programming during power transitions. Power supply sequencing is not required, since the device is indifferent as to which power supply, F-V_{PP} or F-V_{CC}, powers-up first. Example Flash power supply configurations are shown in Figure 12.

11.2.1 F-RP# CONNECTED TO SYSTEM RESET

The use of F-RP# during system reset is important with automated program/erase devices since the system expects to read from the flash memory when it comes out of reset. If a CPU reset occurs without a flash memory reset, proper CPU initialization will not occur because the flash memory may be providing status information instead of array data. Intel recommends connecting F-RP# to the system CPU RESET# signal to allow proper CPU/flash initialization following system reset.

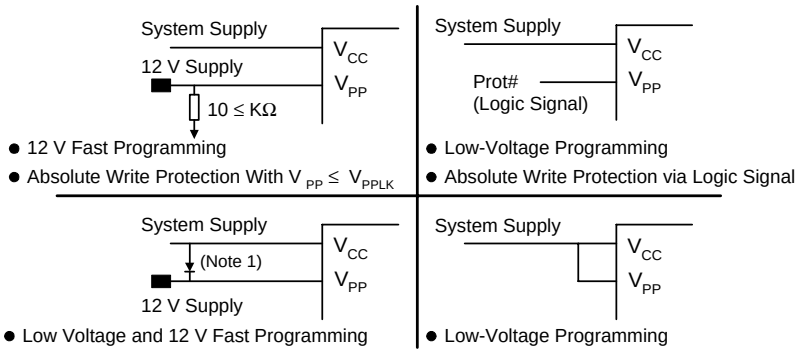
System designers must guard against spurious writes when F-V_{CC} voltages are above V_{LKO}. Since both F-WE# and F-CE# must be low for a command write, driving either signal to V_{IH} will inhibit writes to the device. The CUI architecture provides additional protection since alteration of memory contents can only occur after successful completion of the two-step command sequences. The device is also disabled until F-RP# is brought to V_{IH}, regardless of the state of its control inputs.

By holding the device in reset (F-RP# connected to system PowerGood) during power-up/down, invalid bus conditions during power-up can be masked, providing yet another level of memory protection.

11.2.2 F-V_{CC}, F-V_{PP} AND F-RP# TRANSITION

The CUI latches commands as issued by system software and is not altered by F-V_{PP} or F-CE# transitions or WSM actions. Its default state upon power-up, after exit from reset mode or after F-V_{CC} transitions above V_{LKO} (Lockout voltage), is read array mode.

After any program or block erase operation is complete (even after F-V_{PP} transitions down to V_{PPLK}), the CUI must be reset to read array mode via the Read Array command if access to the flash memory array is desired.



NOTE:

1. A resistor can be used if the F-V_{CC} supply can sink adequate current based on resistor value.

Figure 12. Example Power Supply Configurations

11.3 Noise Reduction

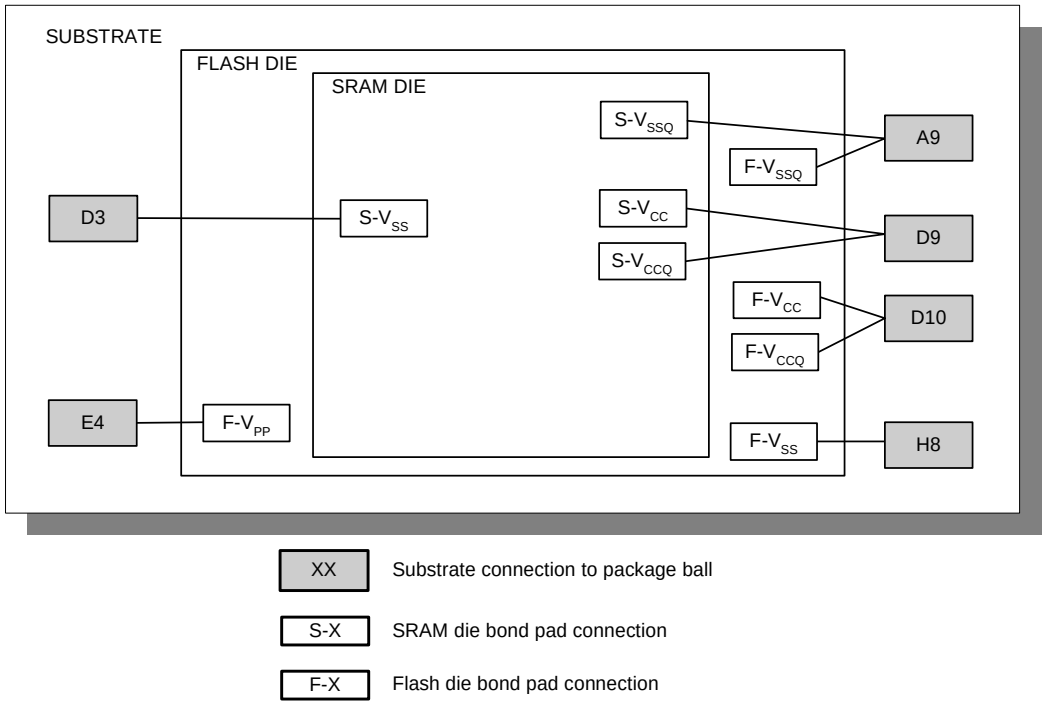
Stacked-CSP memory's power switching characteristics require careful device decoupling. System designers should consider three supply current issues for both the flash and SRAM:

1. Standby current levels (I_{CCS})
2. Read current levels (I_{CCR})
3. Transient peaks produced by falling and rising edges of F-CE#, S-CS_1#, and S-CS_2.

Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress these transient voltage peaks. Each device should have a 0.1 µF ceramic capacitor connected between each F-V_{CC}/S-V_{CC} and GND, and between its F-V_{PP} and GND. These high-frequency, inherently low-inductance capacitors should be placed as close as possible to the package leads.

Noise issues within a system can cause devices to operate erratically if it is not adequately filtered. In order to avoid any noise interaction issues within a system, it is recommended that the design contain the appropriate number of decoupling capacitors in the system. Noise issues can also be reduced if leads to the device are kept very short, in order to reduce inductance.

Decoupling capacitors between V_{cc} and V_{ss} reduce voltage spikes by supplying the extra current needed during switching. Placing these capacitors as close to the device as possible reduces line inductance. The capacitors should be low inductance capacitors; surface mount capacitors typically exhibit lower inductance.



NOTES:

1. Substrate connections refer to ballout locations shown in Figure 1.
2. 0.1µf capacitors should be used with D9, D10 and E4.

Figure 13. Typical Flash+SRAM Substrate Power and Ground Connections

Figure 13 shows that the flash V_{CC} and V_{CCQ} lines are tied together within the substrate; the diagram also shows that the SRAM V_{CC} and V_{CCQ} lines are ties together within the substrate of the package. Because of this, it is highly recommended that systems use a 0.1µf capacitor for each of the D9, D10, and E4 grid ballout locations (see Figure 1 for ballout). These capacitors are necessary to avoid undesired conditions created by excess noise.

11.4 Simultaneous Operation

The term simultaneous operation in used to describe the ability to read or write to the SRAM while also programming or erasing flash. In addition, F-CE#, S-CS_1# and S-CS should not be enabled at the same time. Simultaneous operation of the can be summarized by the following:

- Flash Program or Erase Operations during and SRAM read/write are allowed
- Simultaneous Bus Operations between the Flash and SRAM are **not** allowed (bus contention)

11.4.1 SRAM OPERATION DURING FLASH "BUSY"

This functionality provides the ability to use both the flash and the SRAM "at the same time" within a system, similar to the operation of two devices with separate footprints. This operation can be achieved by following the appropriate timing constraints within a system.

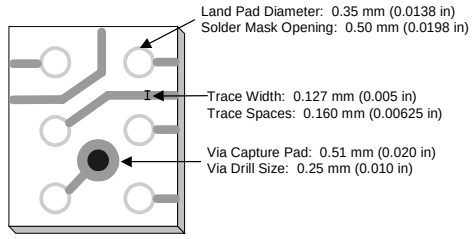
PRODUCT PREVIEW

11.4.2 SIMULTANEOUS BUS OPERATIONS

Operations that require both the SRAM and Flash to be in active mode are disallowed. An example of these cases would include simultaneous reads on both the flash and SRAM, which would result in contention for the data bus, and thus would not produce the intended result. Finally, a read of one device a write of the other similar to the conditions of direct memory access (DMA) operation are also not within the recommended operating conditions.

11.5 Printed Circuit Board Notes

The Intel Stacked CSP will save significant space on your PCB by combining two chips into one BGA style package. Intel Stacked CSP has a 0.8 mm pitch that can be routed on your Printed Circuit Board with conventional design rules. Trace widths of 0.127 mm (0.005 inches) are typical. Unused balls in the center of the package are not populated to further increase the routing options. Standard surface mount process and equipment can be used for the Intel Stacked CSP.



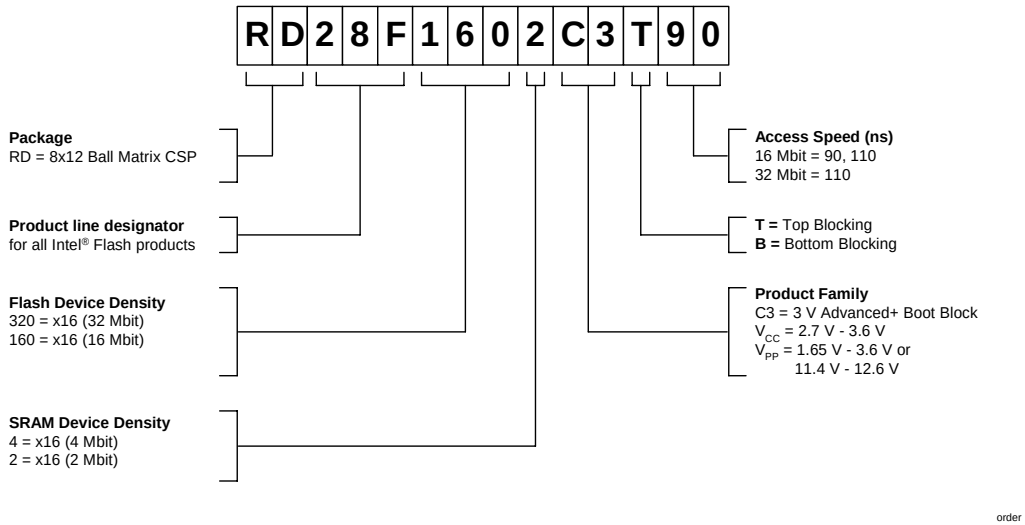
NOTE:
Top View

Figure 14. Standard PCB Design Rules Can be Used with Stacked CSP Devices

11.6 System Design Notes Summary

The new Advanced+ Boot Block Stacked CSP allows higher levels of memory component integration. Different power supply configurations can be used within the system to achieve different objectives. At least three 0.1 µf capacitors should be used to decouple the devices within a system. SRAM reads or writes during a flash program or erase are supported operations. Standard printed circuit board technology can be used.

12.0 ORDERING INFORMATION



VALID COMBINATIONS (All Extended Temperature)

RD28F1602C390 RD28F1602C3110
RD28F3204C3110

NOTE:

90 ns access speed available at production (high volume).

13.0 ADDITIONAL INFORMATION(1,2)

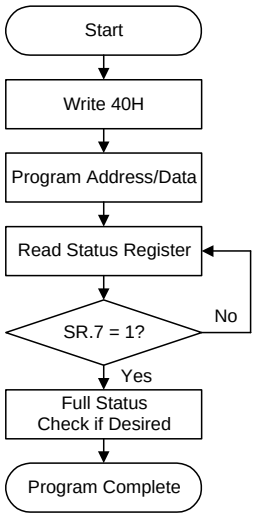
Order Number	Document/Tool
210830	*Flash Memory Databook*
292216	*AP-658 Designing for Upgrade to the Advanced+ Boot Block Flash Memory*
292215	*AP-657 Designing with the Advanced+ Boot Block Flash Memory Architecture*
Contact your Intel Representative	*Flash Data Integrator (FDI) Software Developer's Kit*
297874	*FDI Interactive: Play with Intel's Flash Data Integrator on Your PC*

NOTES:

1. Please call the Intel Literature Center at (800) 548-4725 to request Intel documentation. International customers should contact their local Intel or distribution sales office.
2. Visit Intel's World Wide Web home page at http://www.Intel.com or http://developer.intel.com for technical documentation and tools.

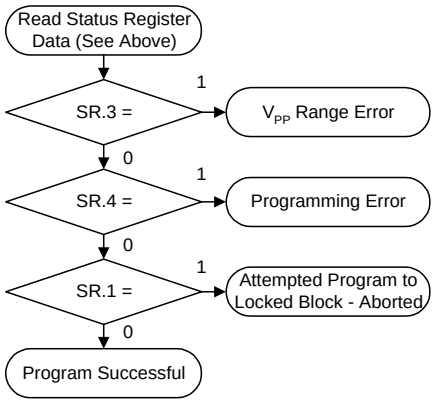
PRODUCT PREVIEW

APPENDIX A
PROGRAM/ERASE FLOWCHARTS



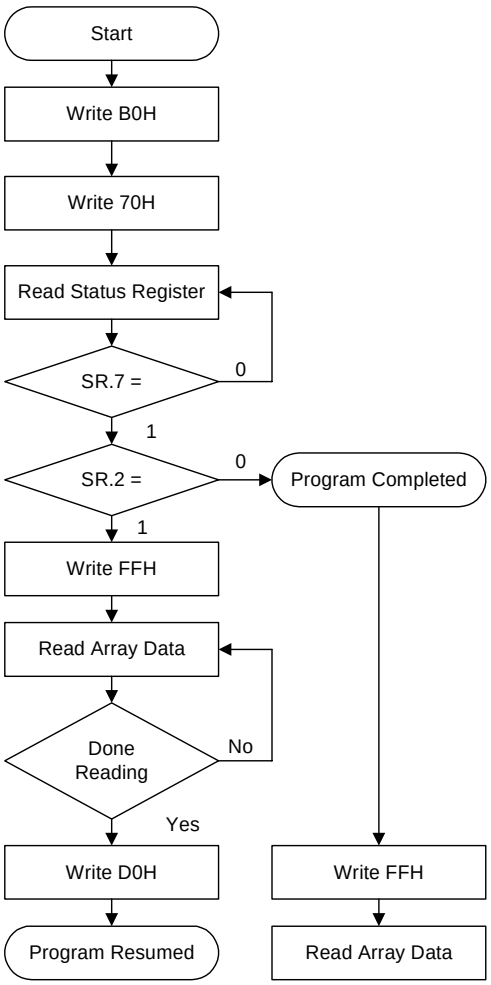
Bus Operation	Command	Comments
Write	Program Setup	Data = 40H
Write	Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Repeat for subsequent programming operations. SR Full Status Check can be done after each program or after a sequence of program operations. Write FFH after the last program operation to reset device to read array mode.		

FULL STATUS CHECK PROCEDURE



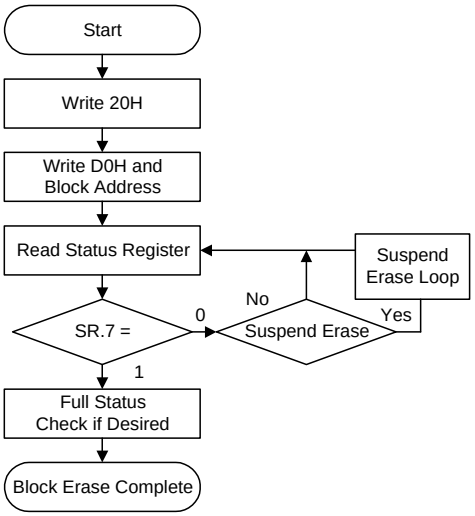
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4 1 = V_{PP} Program Error
Standby		Check SR.1 1 = Attempted Program to Locked Block - Program Aborted
SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine. SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are programmed before full status is checked. If an error is detected, clear the status register before attempting retry or other error recovery.		

Figure 15. Automated Word Programming Flowchart



Bus Operation	Command	Comments
Write	Program Suspend	Data = B0H Addr = X
Write	Read Status	Data = 70H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.2 1 = Program Suspended 0 = Program Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being programmed.
Write	Program Resume	Data = D0H Addr = X

Figure 16. Program Suspend/Resume Flowchart



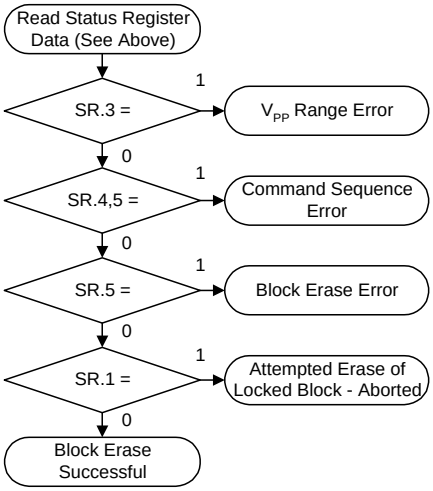
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Addr = Within Block to Be Erased
Write	Erase Confirm	Data = D0H Addr = Within Block to Be Erased
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

Repeat for subsequent block erasures.

Full Status Check can be done after each block erase or after a sequence of block erasures.

Write FFH after the last write operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



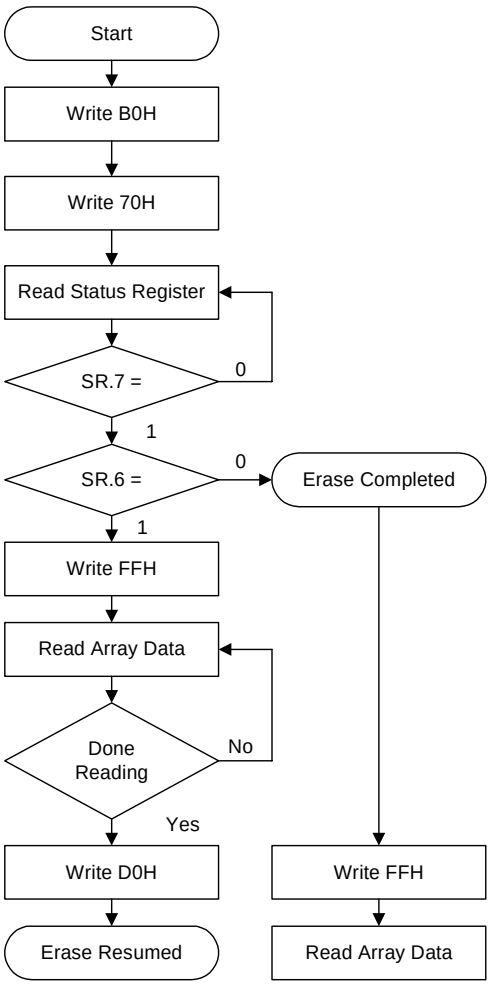
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V_{PP} Low Detect
Standby		Check SR.4,5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error
Standby		Check SR.1 1 = Attempted Erase of Locked Block - Erase Aborted

SR. 1 and 3 MUST be cleared, if set during an erase attempt, before further attempts are allowed by the Write State Machine.

SR.1, 3, 4, 5 are only cleared by the Clear Staus Register Command, in cases where multiple bytes are erased before full status is checked.

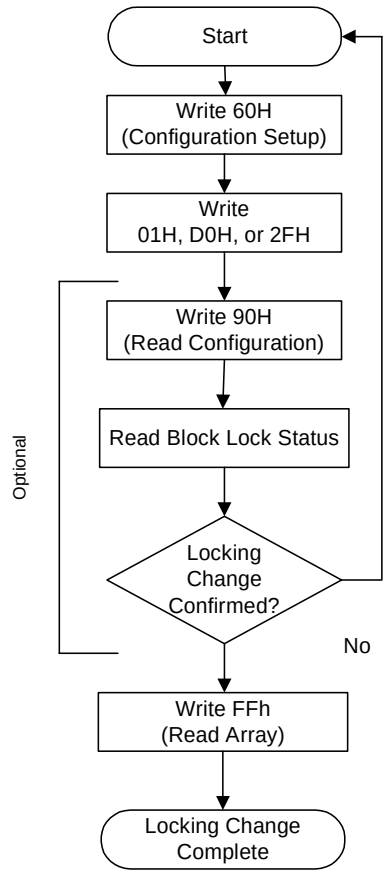
If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 17. Automated Block Erase Flowchart



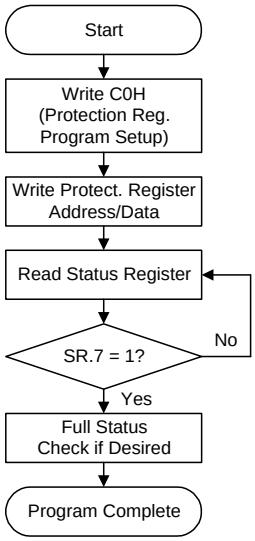
Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H Addr = X
Write	Read Status	Data = 70H Addr = X
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data Addr = X
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy
Standby		Check SR.6 1 = Erase Suspended 0 = Erase Completed
Write	Read Array	Data = FFH Addr = X
Read		Read array data from block other than the one being erased.
Write	Erase Resume	Data = D0H Addr = X

Figure 18. Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Config. Setup	Data = 60H Addr = X
Write	Lock, Unlock, or Lockdown	Data= 01H (Lock Block) D0H (Unlock Block) 2FH (Lockdown Block) Addr=Within block to lock
Write (Optional)	Read Configuration	Data = 90H Addr = X
Read (Optional)	Block Lock Status	Block Lock Status Data Addr = Second addr of block
Standby (Optional)		Confirm Locking Change on DQ_1, DQ_0. (See Block Locking State Table for valid combinations.)

Figure 19. Locking Operations Flowchart



Bus Operation	Command	Comments
Write	Protection Program Setup	Data = C0H
Write	Protection Program	Data = Data to Program Addr = Location to Program
Read		Status Register Data Toggle CE# or OE# to Update Status Register Data
Standby		Check SR.7 1 = WSM Ready 0 = WSM Busy

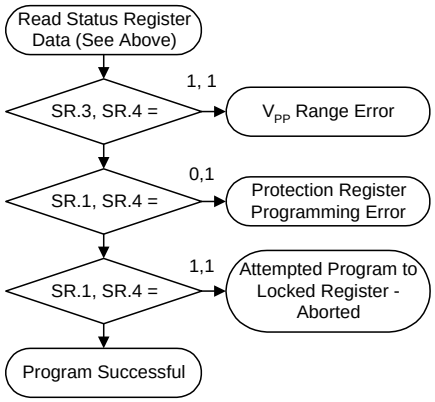
Protection Program operations can only be addressed within the protection register address space. Addresses outside the defined space will return an error.

Repeat for subsequent programming operations.

SR Full Status Check can be done after each program or after a sequence of program operations.

Write FFH after the last program operation to reset device to read array mode.

FULL STATUS CHECK PROCEDURE



Bus Operation	Command	Comments
Standby		SR.1 SR.3 SR.4 0 1 1 V_{PP} Low
Standby		0 0 1 Prot. Reg. Prog. Error
Standby		1 0 1 Register Locked: Aborted

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.1, SR.3 and SR.4 are only cleared by the Clear Staus Register Command, in cases of multiple protection register program operations before full status is checked.

If an error is detected, clear the status register before attempting retry or other error recovery.

Figure 20. Protection Register Programming Flowchart

APPENDIX B
CFI QUERY STRUCTURE

This appendix defines the data structure or “database” returned by the Common Flash Interface (CFI) Query command. System software should parse this structure to gain critical information such as block size, density, x8/x16, and electrical specifications. Once this information has been obtained, the software will know which command sets to use to enable flash writes, block erases, and otherwise control the flash component. The Query is part of an overall specification for multiple command set and control interface descriptions called Common Flash Interface, or CFI.

B.1 QUERY STRUCTURE OUTPUT

The Query “database” allows system software to gain information for controlling the flash component. This section describes the device’s CFI-compliant interface that allows the host system to access Query data.

Query data are always presented on the lowest-order data outputs (DQ_{0-7}) only. The numerical offset value is the address relative to the maximum bus width supported by the device. On this family of devices, the Query table device starting address is a 10h, which is a word address for x16 devices.

For a word-wide (x16) device, the first two bytes of the Query structure, “Q” and ”R” in ASCII, appear on the low byte at word addresses 10h and 11h. This CFI-compliant device outputs 00H data on upper bytes. Thus, the device outputs ASCII “Q” in the low byte (DQ_{0-7}) and 00h in the high byte (DQ_{8-15}).

At Query addresses containing two or more bytes of information, the least significant data byte is presented at the lower address, and the most significant data byte is presented at the higher address.

In all of the following tables, addresses and data are represented in hexadecimal notation, so the “h” suffix has been dropped. In addition, since the upper byte of word-wide devices is always “00h,” the leading “00” has been dropped from the table notation and only the lower byte value is shown. Any x16 device outputs can be assumed to have 00h on the upper byte in this mode.

Table B1. Summary of Query Structure Output As a Function of Device and Mode

Device	Hex Offset	Code	ASCII Value
Device Addresses	10:	51	“Q”
	11:	52	“R”
	12:	59	“Y”

Table B2. Example of Query Structure Output of x16 and x8 Devices

Word Addressing			Byte Addressing		
Offset	**Hex Code**	**Value**	**Offset**	**Hex Code**	**Value**
A_{15}–A_0	**D_{15}–D_0**		**A_7–A_0**	**D_7–D_0**	
0010h	0051	"Q"	10h	51	"Q"
0011h	0052	"R"	11h	52	"R"
0012h	0059	"Y"	12h	59	"Y"
0013h	P_ID_{LO}	PrVendor	13h	P_ID_{LO}	PrVendor
0014h	P_ID_{HI}	ID #	14h	P_ID_{LO}	ID #
0015h	P_{LO}	PrVendor	15h	P_ID_{HI}	ID #
0016h	P_{HI}	TblAdr	16h	...	...
0017h	A_ID_{LO}	AltVendor	17h		
0018h	A_ID_{HI}	ID #	18h		
...	...	...	...		

B.2 QUERY STRUCTURE OVERVIEW

The Query command causes the flash component to display the Common Flash Interface (CFI) Query structure or "database." The structure sub-sections and address locations are summarized below.

Table B3. Query Structure(1)

Offset	Sub-Section Name	Description
00h		Manufacturer Code
01h		Device Code
(BA+2)h(2)	Block Status Register	Block-Specific information
04-0Fh	*Reserved*	*Reserved for vendor-specific information*
10h	CFI Query Identification String	Command set ID and vendor data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
P(3)	Primary Intel-Specific Extended Query Table	Vendor-defined additional information specific to the Primary Vendor Algorithm

NOTES:

1. Refer to the Query Structure Output section and offset 28h for the detailed definition of offset address as a function of device bus width and mode.
2. BA = The beginning location of a Block Address (e.g., 08000h is the beginning location of block 1 when the block size is 32 Kword).
3. Offset 15 defines "P" which points to the Primary Intel-specific Extended Query Table.

B.3 BLOCK LOCK STATUS REGISTER

The Block Status Register indicates whether an erase operation completed successfully or whether a given block is locked or can be accessed for flash program/erase operations.

Block Erase Status (BSR.1) allows system software to determine the success of the last block erase operation. BSR.1 can be used just after power-up to verify that the V_{CC} supply was not accidentally removed during an erase operation. This bit is only reset by issuing another erase operation to the block. The Block Status Register is accessed from word address 02h within each block.

Table B4. Block Status Register

Offset	Length	Description	Add.	Value
(BA+2)h[1]	1	Block Lock Status Register	BA+2:	--00 or --01
		BSR.0 Block Lock Status 0 = Unlocked 1 = Locked	BA+2:	(bit 0): 0 or 1
		BSR.1 Block Lock-Down Status 0 = Not locked down 1 = Locked down	BA+2:	(bit 1): 0 or 1
		BSR 2–7: *Reserved for future use*	BA+2:	(bit 2–7): 0

NOTE:

1. BA = The beginning location of a Block Address (i.e., 008000h is the beginning location of block 1 in word mode.)

B.4 CFI QUERY IDENTIFICATION STRING

The Identification String provides verification that the component supports the Common Flash Interface specification. It also indicates the specification version and supported vendor-specified command set(s).

Table B5. CFI Identification

Offset	Length	Description	Add.	Hex Code	Value
10h	3	Query-unique ASCII string “QRY“	10 11: 12:	--51 --52 --59	“Q” “R” “Y”
13h	2	Primary vendor command set and control interface ID code. 16-bit ID code for vendor-specified algorithms	13: 14:	--03 --00	
15h	2	Extended Query Table primary algorithm address	15: 16:	--35 --00	
17h	2	Alternate vendor command set and control interface ID code. 0000h means no second vendor-specified algorithm exists	17: 18:	--00 --00	
19h	2	Secondary algorithm Extended Query Table address. 0000h means none exists	19: 1A:	--00 --00	

B.5 SYSTEM INTERFACE INFORMATION

Table B6. System Interface Information

Offset	Length	Description	Add.	Hex Code	Value
1Bh	1	V_{CC} logic supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1B:	--27	2.7 V
1Ch	1	V_{CC} logic supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 BCD volts	1C:	--36	3.6 V
1Dh	1	V_{PP} [programming] supply minimum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1D:	--B4	11.4 V
1Eh	1	V_{PP} [programming] supply maximum program/erase voltage bits 0–3 BCD 100 mV bits 4–7 HEX volts	1E:	--C6	12.6 V
1Fh	1	“n” such that typical single word program time-out = 2^n µs	1F:	--05	32 µs
20h	1	“n” such that typical max. buffer write time-out = 2^n µs	20:	--00	NA
21h	1	“n” such that typical block erase time-out = 2^n ms	21:	--0A	1s
22h	1	“n” such that typical full chip erase time-out = 2^n ms	22:	--00	NA
23h	1	“n” such that maximum word program time-out = 2^n times typical	23:	--04	512µs
24h	1	“n” such that maximum buffer write time-out = 2^n times typical	24:	--00	NA
25h	1	“n” such that maximum block erase time-out = 2^n times typical	25:	--03	8s
26h	1	“n” such that maximum chip erase time-out = 2^n times typical	26:	--00	NA

B.6 DEVICE GEOMETRY DEFINITION

Table B7. Device Geometry Definition

Offset	Length	Description	Code See Table Below		
27h	1	"n" such that device size = 2^n in number of bytes	27:		
28h	2	Flash device interface: x8 async x16 async x8/x16 async 28:00,29:00 28:01,29:00 28:02,29:00	28: 29:	--01 --00	x16
2Ah	2	"n" such that maximum number of bytes in write buffer = 2^n	2A: 2B:	--00 --00	0
2Ch	1	Number of erase block regions within device: 1. x = 0 means no erase blocking; the device erases in "bulk" 2. x specifies the number of device or partition regions with one or more contiguous same-size erase blocks. 3. Symmetrically blocked partitions have one blocking region 4. Partition size = (total blocks) x (individual block size)	2C:	--02	2
2Dh	4	Erase Block Region 1 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	2D: 2E: 2F: 30:		
31h	4	Erase Block Region 2 Information bits 0–15 = y, y+1 = number of identical-size erase blocks bits 16–31 = z, region erase block(s) size are z x 256 bytes	31: 32: 33: 34:		

Device Geometry Definition

Address	16 Mbit		32 Mbit	
	–B	–T	–B	–T
27:	--15	--15	--16	--16
28:	--01	--01	--01	--01
29:	--00	--00	--00	--00
2A:	--00	--00	--00	--00
2B:	--00	--00	--00	--00
2C:	--02	--02	--02	--02
2D:	--07	--1E	--07	--3E
2E:	--00	--00	--00	--00
2F:	--20	--00	--20	--00
30:	--00	--01	--00	--01
31:	--1E	--07	--3E	--07
32:	--00	--00	--00	--00
33:	--00	--20	--00	--20
34:	--01	--00	--01	--00

B.7 INTEL-SPECIFIC EXTENDED QUERY TABLE

Certain flash features and commands are optional. The Intel-Specific Extended Query table specifies this and other similar types of information.

Table B8. Primary-Vendor Specific Extended Query

Offset(1) P = 35h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+0)h	3	Primary extended query table	35:	--50	"P"
(P+1)h		Unique ASCII string "PRI"	36:	--52	"R"
(P+2)h			37:	--49	"I"
(P+3)h	1	Major version number, ASCII	38:	--31	"1"
(P+4)h	1	Minor version number, ASCII	39:	--30	"0"
(P+5)h	4	Optional feature and command support (1=yes, 0=no)	3A:	--66	
(P+6)h		*bits 9–31 are reserved; undefined bits are "0." If bit 31 is*	3B:	--00	
(P+7)h		*"1" then another 31 bit field of Optional features follows*	3C:	--00	
(P+8)h		*at the end of the bit-30 field.*	3D:	--00	
		bit 0 Chip erase supported	bit 0 = 0		No
		bit 1 Suspend erase supported	bit 1 = 1		Yes
		bit 2 Suspend program supported	bit 2 = 1		Yes
		bit 3 Legacy lock/unlock supported	bit 3 = 0		No
		bit 4 Queued erase supported	bit 4 = 0		No
		bit 5 Instant individual block locking supported	bit 5 = 1		Yes
		bit 6 Protection bits supported	bit 6 = 1		Yes
		bit 7 Page mode read supported	bit 7 = 0		No
		bit 8 Synchronous read supported	bit 8 = 0		No
(P+9)h	1	Supported functions after suspend: read Array, Status, Query Other supported operations are: *bits 1–7 reserved; undefined bits are "0"*	3E:	--01	
		bit 0 Program supported after erase suspend	bit 0 = 1		Yes
(P+A)h	2	Block status register mask	3F:	--03	
(P+B)h		*bits 2–15 are Reserved; undefined bits are "0"*	40:	--00	
		bit 0 Block Lock-Bit Status register active	bit 0 = 1		Yes
		bit 1 Block Lock-Down Bit Status active	bit 1 = 1		Yes
(P+C)h	1	V_{CC} logic supply highest performance program/erase voltage bits 0–3 BCD value in 100 mV bits 4–7 BCD value in volts	41:	--33	3.3 V
(P+D)h	1	V_{PP} optimum program/erase supply voltage bits 0–3 BCD value in 100 mV bits 4–7 HEX value in volts	42:	--C0	12.0 V

Table B9. Protection Register Information

Offset(1) P = 35h	Length	Description (Optional Flash Features and Commands)	Add.	Hex Code	Value
(P+E)h	1	Number of Protection register fields in JEDEC ID space. “00h,” indicates that 256 protection bytes are available	43:	--01	01
(P+F)h	4	Protection Field 1: Protection Description	44:	--80	80h
(P+10)h		This field describes user-available One Time Programmable (OTP) Protection register bytes. Some are pre-programmed with device-unique serial numbers. Others are user programmable. Bits 0–15 point to the Protection register Lock byte, the section’s first byte. The following bytes are factory pre-programmed and user-programmable.	45:	--00	00h
(P+11)h		bits 0–7 = Lock/bytes JEDEC-plane physical low address bits 8–15 = Lock/bytes JEDEC -plane physical high address bits 16–23 = “n” such that 2^n = factory pre-programmed bytes bits 24–31 = “n” such that 2^n = user programmable bytes	46:	--03	8 byte
(P+12)h			47:	--03	8 byte
(P+13)h		*Reserved for future use*	48:		

NOTES:

1. The variable P is a pointer which is defined at CFI offset 15h.

APPENDIX C
WORD-WIDE MEMORY MAP DIAGRAMS

16-Mbit, and 32-Mbit Word-Wide Memory Flash Addressing

Top Boot			Bottom Boot		
Size (KW)	**16M**	**32M**	**Size (KW)**	**16M**	**32M**
4	FF000-FFFFF	1FF000-1FFFFF	32		1F8000-1FFFFF
4	FE000-FEFFF	1FE000-1FEFFF	32		1F0000-1F7FFF
4	FD000-FDFFF	1FD000-1FDFFF	32		1E8000-1EFFFF
4	FC000-FCFFF	1FC000-1FCFFF	32		1E0000-1E7FFF
4	FB000-FBFFF	1FB000-1FBFFF	32		1D8000-1DFFFF
4	FA000-FAFFF	1FA000-1FAFFF	32		1D0000-1D7FFF
4	F9000-F9FFF	1F9000-1F9FFF	32		1C8000-1CFFFF
4	F8000-F8FFF	1F8000-1F8FFF	32		1C0000-1C7FFF
32	F0000-F7FFF	1F0000-1F7FFF	32		1B8000-1BFFFF
32	E8000-EFFFF	1E8000-1EFFFF	32		1B0000-1B7FFF
32	E0000-E7FFF	1E0000-1E7FFF	32		1A8000-1AFFFF
32	D8000-DFFFF	1D8000-1DFFFF	32		1A0000-1A7FFF
32	D0000-D7FFF	1D0000-1D7FFF	32		198000-19FFFF
32	C8000-CFFFF	1C8000-1CFFFF	32		190000-197FFF
32	C0000-C7FFF	1C0000-1C7FFF	32		188000-18FFFF
32	B8000-BFFFF	1B8000-1BFFFF	32		180000-187FFF
32	B0000-B7FFF	1B0000-1B7FFF	32		178000-17FFFF
32	A8000-AFFFF	1A8000-1AFFFF	32		170000-177FFF
32	A0000-A7FFF	1A0000-1A7FFF	32		168000-16FFFF
32	98000-9FFFF	198000-19FFFF	32		160000-167FFF
32	90000-97FFF	190000-197FFF	32		158000-15FFFF
32	88000-8FFFF	188000-18FFFF	32		150000-157FFF
32	80000-87FFF	180000-187FFF	32		148000-14FFFF
32	78000-7FFFF	178000-17FFFF	32		140000-147FFF
32	70000-77FFF	170000-177FFF	32		138000-13FFFF
32	68000-6FFFF	168000-16FFFF	32		130000-137FFF
32	60000-67FFF	160000-167FFF	32		128000-12FFFF
32	58000-5FFFF	158000-15FFFF	32		120000-127FFF
32	50000-57FFF	150000-157FFF	32		118000-11FFFF
32	48000-4FFFF	148000-14FFFF	32		110000-117FFF
32	40000-47FFF	140000-147FFF	32		108000-10FFFF
32	38000-3FFFF	138000-13FFFF	32		100000-107FFF
32	30000-37FFF	130000-137FFF	32	F8000-FFFFF	0F8000-0FFFFF
32	28000-2FFFF	128000-12FFFF	32	F0000-F7FFF	0F0000-0F7FFF
32	20000-27FFF	120000-127FFF	32	E8000-EFFFF	0E8000-0EFFFF
32	18000-1FFFF	118000-11FFFF	32	E0000-E7FFF	0E0000-0E7FFF
32	10000-17FFF	110000-117FFF	32	D8000-DFFFF	0D8000-0DFFFF
32	08000-0FFFF	108000-10FFFF	32	D0000-D7FFF	0D0000-0D7FFF
32	00000-07FFF	100000-107FFF	32	C8000-CFFFF	0C8000-0CFFFF
This column continues on next page			This column continues on next page		

16-Mbit, and 32-Mbit Word-Wide Memory Addressing (Continued)

Top Boot			Bottom Boot		
Size (KW)	**16M**	**32M**	**Size (KW)**	**16M**	**32M**
32		0F8000-0FFFFF	32	C0000-C7FFF	0C0000-0C7FFF
32		0F0000-0F7FFF	32	B8000-BFFFF	0B8000-0BFFFF
32		0E8000-0EFFFF	32	B0000-B7FFF	0B0000-0B7FFF
32		0E0000-0E7FFF	32	A8000-AFFFF	0A8000-0AFFFF
32		0D8000-0DFFFF	32	A0000-A7FFF	0A0000-0A7FFF
32		0D0000-0D7FFF	32	98000-9FFFF	098000-09FFFF
32		0C8000-0CFFFF	32	90000-97FFF	090000-097FFF
32		0C0000-0C7FFF	32	88000-8FFFF	088000-08FFFF
32		0B8000-0BFFFF	32	80000-87FFF	080000-087FFF
32		0B0000-0B7FFF	32	78000-7FFFF	78000-7FFFF
32		0A8000-0AFFFF	32	70000-77FFF	70000-77FFF
32		0A0000-0A7FFF	32	68000-6FFFF	68000-6FFFF
32		098000-09FFFF	32	60000-67FFF	60000-67FFF
32		090000-097FFF	32	58000-5FFFF	58000-5FFFF
32		088000-08FFFF	32	50000-57FFF	50000-57FFF
32		080000-087FFF	32	48000-4FFFF	48000-4FFFF
32		078000-07FFFF	32	40000-47FFF	40000-47FFF
32		070000-077FFF	32	38000-3FFFF	38000-3FFFF
32		068000-06FFFF	32	30000-37FFF	30000-37FFF
32		060000-067FFF	32	28000-2FFFF	28000-2FFFF
32		058000-05FFFF	32	20000-27FFF	20000-27FFF
32		050000-057FFF	32	18000-1FFFF	18000-1FFFF
32		048000-04FFFF	32	10000-17FFF	10000-17FFF
32		040000-047FFF	32	08000-0FFFF	08000-0FFFF
32		038000-03FFFF	4	07000-07FFF	07000-07FFF
32		030000-037FFF	4	06000-06FFF	06000-06FFF
32		028000-02FFFF	4	05000-05FFF	05000-05FFF
32		020000-027FFF	4	04000-04FFF	04000-04FFF
32		018000-01FFFF	4	03000-03FFF	03000-03FFF
32		010000-017FFF	4	02000-02FFF	02000-02FFF
32		008000-00FFFF	4	01000-01FFF	01000-01FFF
32		000000-007FFF	4	00000-00FFF	00000-00FFF

APPENDIX D
DEVICE ID TABLE

Read Configuration Addresses and Data

Item		Address	Data
Manufacturer Code	x16	00000	0089
Device Code			
16-Mbit x 16-T	x16	00001	88C2
16-Mbit x 16-B	x16	00001	88C3
32-Mbit x 16-T	x16	00001	88C4
32-Mbit x 16-B	x16	00001	88C5

NOTE: Other locations within the configuration address space are reserved by Intel for future use.

APPENDIX E
PROTECTION REGISTER ADDRESSING

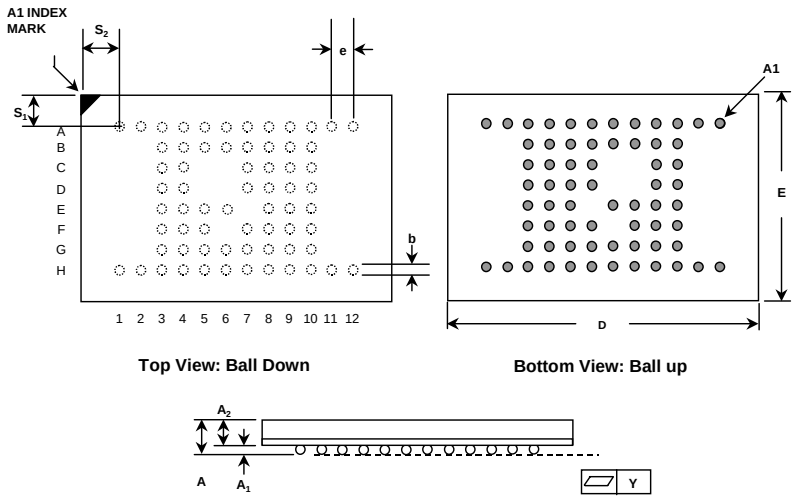
Word-Wide Protection Register Addressing

Word	Use	A7	A6	A5	A4	A3	A2	A1	A0
LOCK	Both	1	0	0	0	0	0	0	0
0	Factory	1	0	0	0	0	0	0	1
1	Factory	1	0	0	0	0	0	1	0
2	Factory	1	0	0	0	0	0	1	1
3	Factory	1	0	0	0	0	1	0	0
4	User	1	0	0	0	0	1	0	1
5	User	1	0	0	0	0	1	1	0
6	User	1	0	0	0	0	1	1	1
7	User	1	0	0	0	1	0	0	0

NOTE:

1. All address lines not specified in the above table must be 0 when accessing the Protection Register, i.e., A_{21}–A_8 = 0.

APPENDIX F
STACKED CHIP SCALE PACKAGE MECHANICAL SPECIFICATION



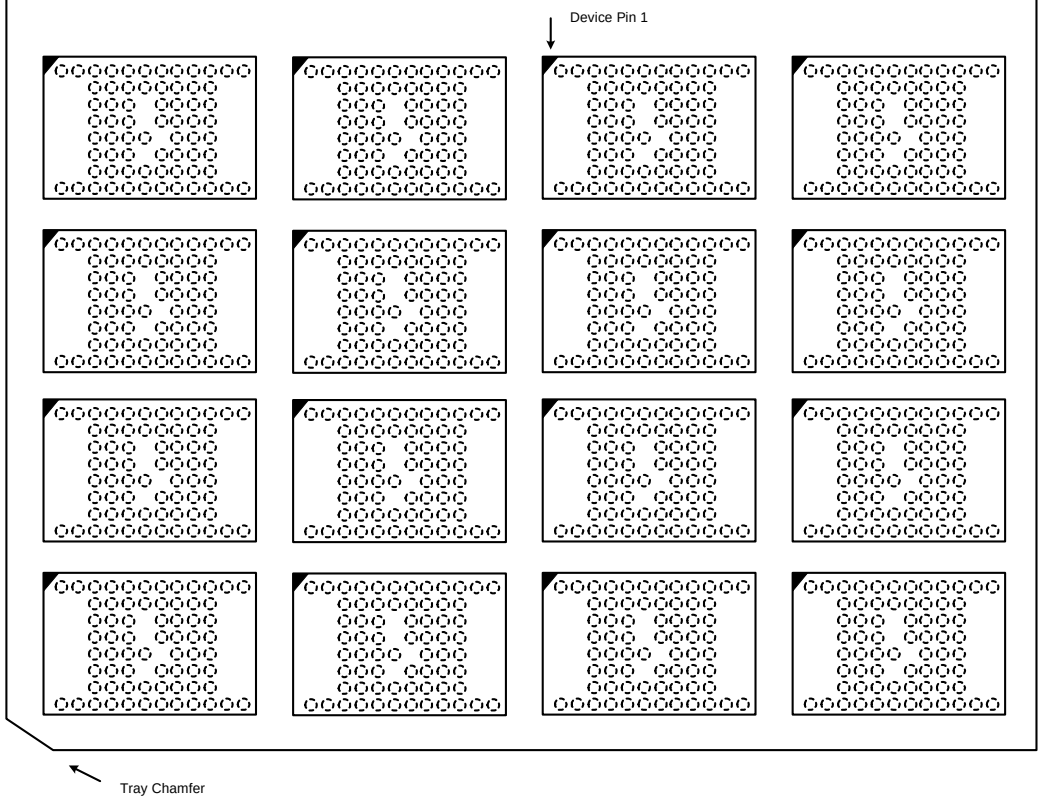
NOTE:

72- ball package consists of 8 x 12 solder ball matrix, 8 rows and 12 columns. Each row is identified by a number and the column by a letter. Each bump location, thus, is designated by row & column combination. Example, Bump C2 indicates 3rd row and the 2nd column.

Figure 21. 72-Ball Stacked-CSP: 12 x 8 Matrix

	Sym	Millimeters			Inches		
		Min	Nom	Max	Min	Nom	Max
Package Height	A	1.20	1.30	1. 40	0.047	0.051	0.055
Standoff	A1	0.30	0.35	0.40	0.012	0.014	0.016
Package Body Thickness	A2	0.92	0.97	1.02	0.036	0.038	0.040
Ball Lead Diameter	b	0.325	0.40	0.475	0.013	0.016	0.019
Package Body Length – 16 Mb/2 Mb	D	9.90	10.00	10.10	0.429	0.433	0.437
Package Body Width – 16 Mb/2 Mb	E	7.90	8.00	8.10	0.311	0.315	0.319
Package Body Length – 32 Mb/4 Mb	D	11.90	12.00	12.10	0.469	0.472	0.476
Package Body Width – 32 Mb/4 Mb	E	7.90	8.00	8.10	0.311	0.315	0.319
Pitch	e		0.80			0.031	
Seating Plane Coplanarity	Y			0.1			0.004
Corner to First Bump distance – 16 Mb/2 Mb	S1	1.10	1.20	1.30	0.0433	0.0472	0.0512
Corner to First Bump distance – 16 Mb/2 Mb	S2	0.50	0.60	0.70	0.0197	0.0236	0.0276
Corner to First Bump distance – 32 Mb/ 4Mb	S1	1.10	1.20	1.30	0.0433	0.0472	0.0512
Corner to First Bump distance – 32 Mb/ 4Mb	S2	1.50	1.60	1.70	0.0591	0.0630	0.0669

APPENDIX G
STACKED CHIP SCALE PACKAGE
MEDIA INFORMATION



NOTES:
Drawing is not to scale and is only designed to show orientation of devices.

Figure 22. Stacked CSP Device in Tray Orientation (8 x 10 mm and 8 x 12 mm)

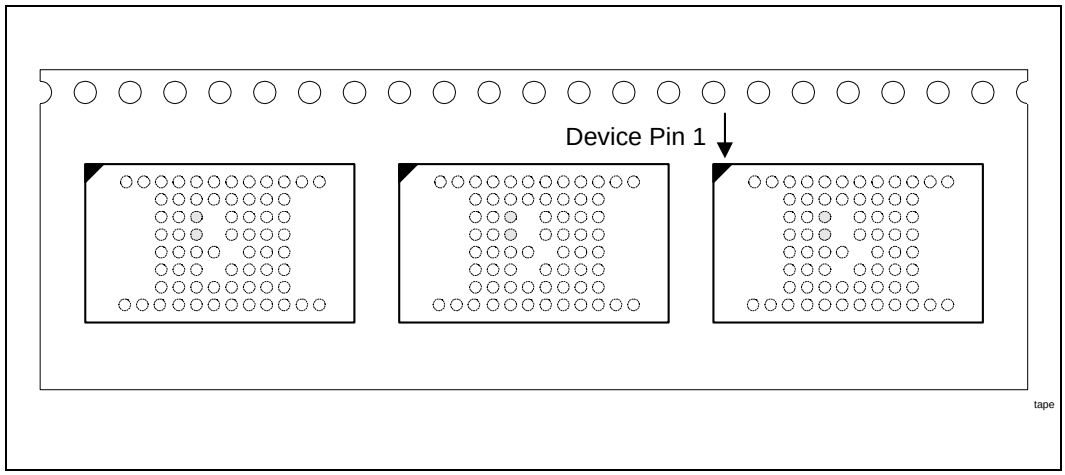


Figure 23. Stacked CSP Device in 24 mm Tape (8 x 10 mm and 8 x 12 mm)