PRELIMINARY

AMD

Am79C874

Quad Fast Ethernet Transceiver Plus (QFEX+™) for 100BASE-X

DISTINCTIVE CHARACTERISTICS

- **Compatible with IEEE 802.3u standard for 100BASE-TX and 100BASE-FX**
- **Fully integrated MLT-3 function with Baseline Wander Restoration**
- **Low latency to meet Class 2 Repeater applications**
- **Fully integrated Quad Media Independent Interface (MII)**
- **Quad Integrated Digital CMOS 100 Mbps clock recovery circuits**
- **Full Duplex capability**
- **Programmable loopback modes**
- **Programmable LED support**
- **Capable of bypassing transmit and receive state machine to support 5-bit symbol interface**
- **IEEE 1149.1-compatible JTAG support**
- **Scramble and descramble feature supported for 100BASE-TX**
- **Link Monitor and Far End Fault Indication (FEFI)**
- **Optimized for 100BASE-X repeater or switch applications**
- **Configurable repeater modes supporting port switching**
- **Carrier Integrity Monitor (CIM) support with dedicated CIM_ISOLATE counter available in repeater mode**
- **Direct interface to TX (MLT-3) or FX Physical Medium Dependent (PMD) devices**
- **Individual False Carrier Indication signal for repeater applications**
- **CMOS device features high integration and low power with a single +5 V supply in 160-pin PQFP**

GENERAL DESCRIPTION

The Am79C874 Quad Fast Ethernet Transceiver Plus (QFEX+) is a CMOS device that implements the MII, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and Physical Medium Dependent (PMD) sublayers, including the MLT-3 functions, for four 100BASE-TX ports. Therefore, the QFEX+ device interfaces directly to magnetics to support operation over two pairs of shielded twisted pair (STP) or two pairs of Category 5 unshielded twisted pair (UTP) cables. The MLT-3 functions can be disabled to support 100BASE-FX applications over two multi-mode fibers.

The QFEX+ device performs all the functions of the QFEX (Am79C870) device which include encoding the MII 4-bit data (4B/5B), decoding the received code groups (5B/4B), generating carrier sense and collision detect indications, serializing code groups for transmission, de-serializing received serial data, mapping transmit, receive, carrier sense, and collision at the MII interface, and recovering clock from the incoming data stream. In addition, the QFEX+ device includes an MLT-3 encoder/decoder, baseline wander restoration circuitry, and an adaptive equalizer per port. The QFEX+ chip offers stream cipher scrambling and descrambling capability for 100BASE-TX applications.

When transmitting, the QFEX+ chip receives 4-bit (nibble) wide data across the MII at 25 million nibbles per second. It then encodes the data, optionally scrambles the data, serializes the data, and converts the NRZI data stream to a three-level code for transmission to the network.

When receiving, the QFEX+ chip receives the three-level code and converts it back to an NRZI data stream. It then recovers the clock from the NRZI data stream, de-serializes the data stream, optionally descrambles the data stream, and decodes the code groups (5B/4B).

The QFEX+ chip has an independent MII for each of the four ports. Therefore, all four ports can simultaneously receive data from the network and output data to individual MII ports. The device can also be configured in such a way (referred to as "Shared MII mode" in this document) that the four network ports are independently mapped to either one of the MIIs (MII[0] and MII[1]). In this mode, more than one port can share a single MII.

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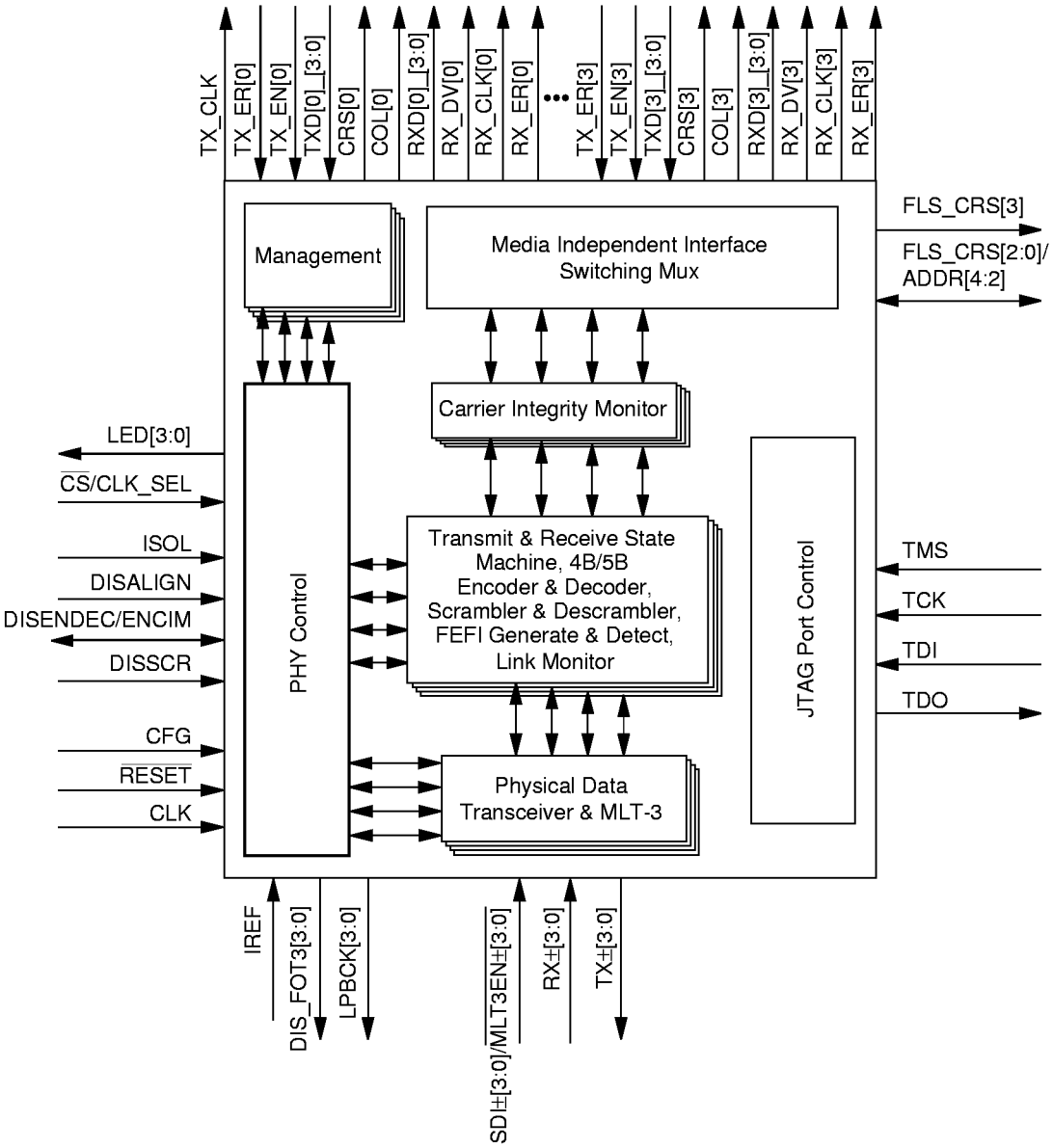
BLOCK DIAGRAM (INDEPENDENT MII MODE)



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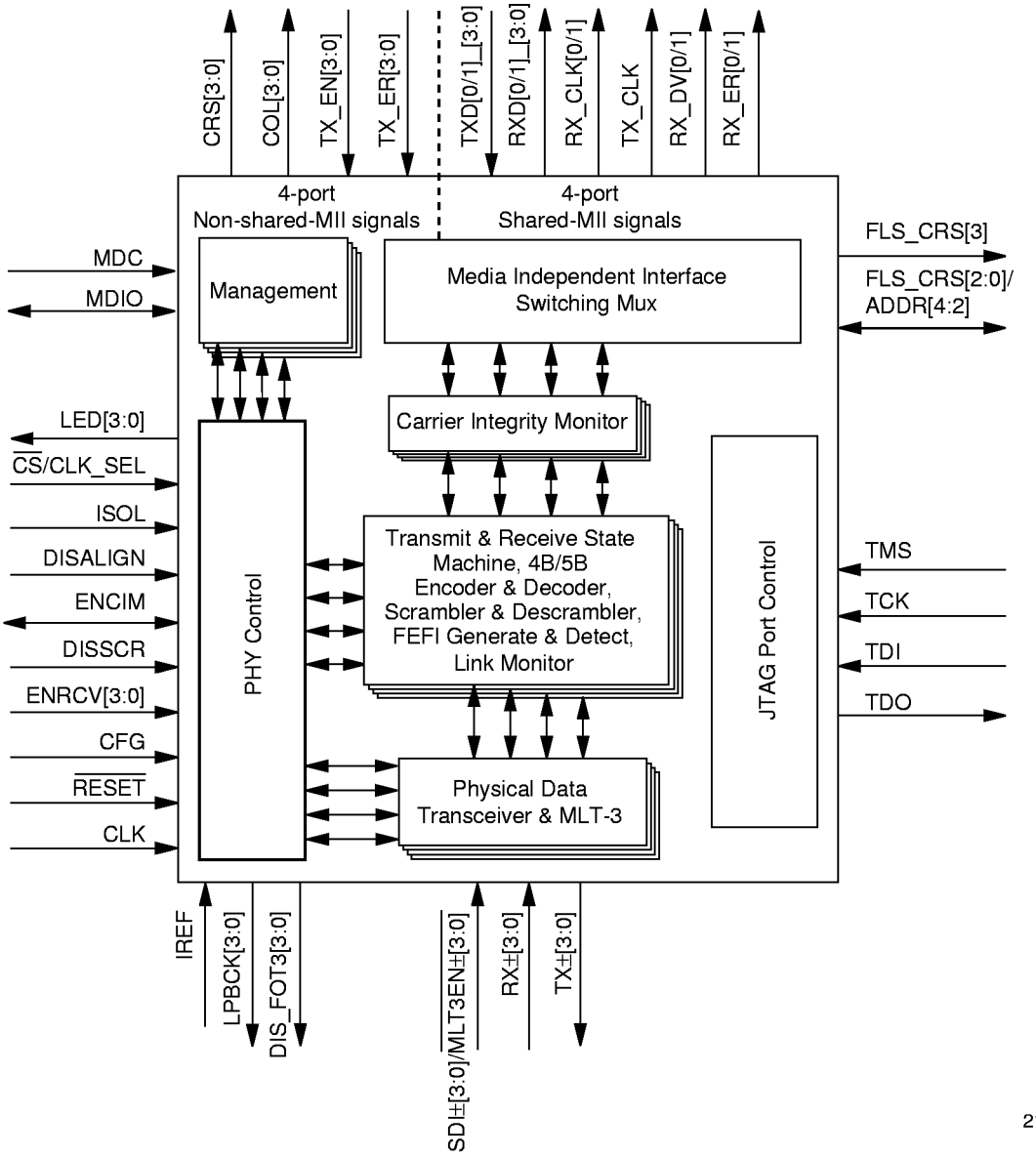
BLOCK DIAGRAM (SHARED MII MODE)



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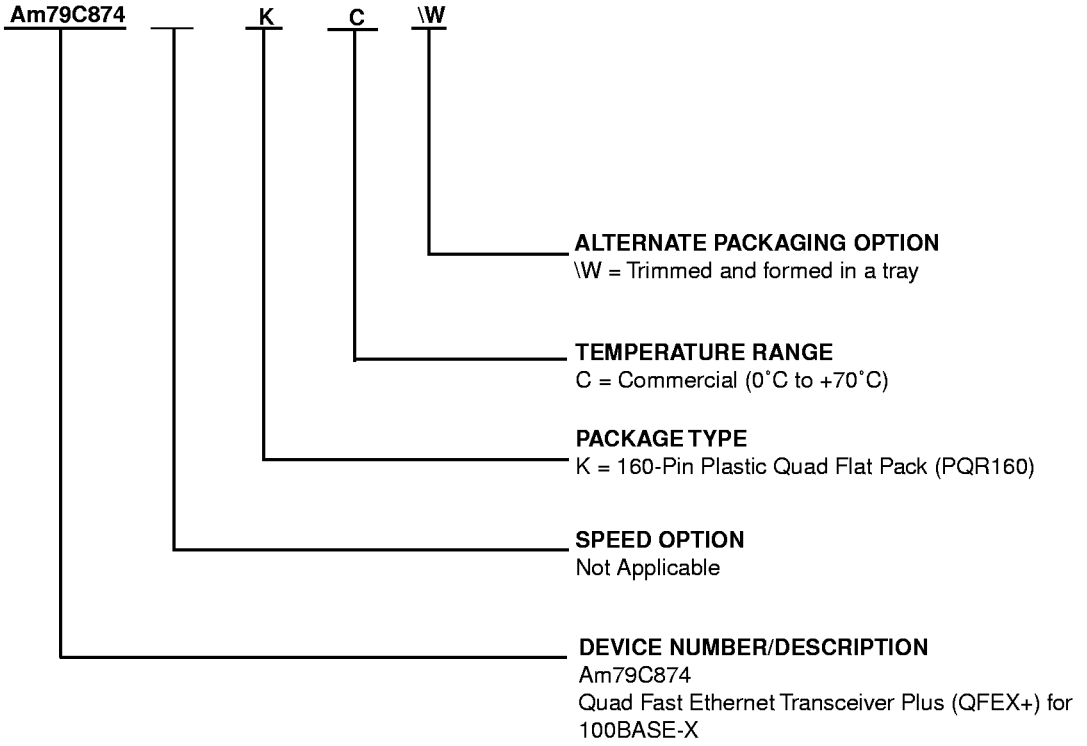
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Valid Combinations	
Am79C874	KC\W

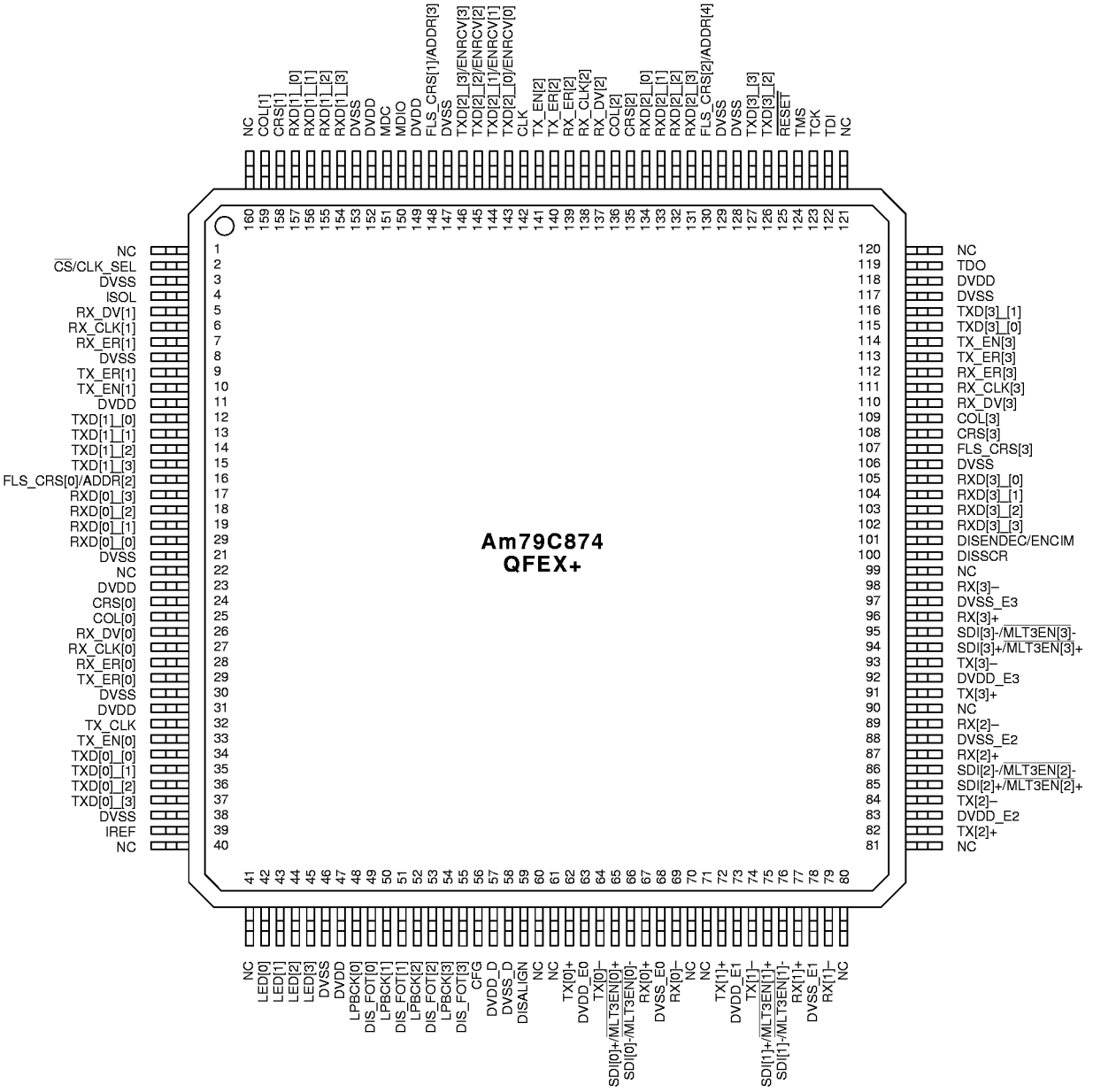
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

RELATED PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter (SIA)
Am7996	IEEE 802.3/Ethernet/Cheapernet Transceiver
Am79C90	CMOS Local Area Network Controller for Ethernet (C-LANCE)
Am79C98	Twisted Pair Ethernet Transceiver (TPEX)
Am79C100	Twisted Pair Ethernet Transceiver Plus (TPEX+)
Am79C730	Integrated Multiport Repeater 100 (IMR100™)
Am79C870	Quad Fast Ethernet Transceiver for 100BASE-X (QFEX™)
Am79C871	Quad Fast Ethernet Transceiver for 100BASE-X Repeaters (QFEXr™)
Am79C875	Quad Fast Ethernet Transceiver Plus for 100BASE-X Repeaters (QFEXr+™)
Am79C981	Integrated Multiport Repeater Plus (IMR+™)
Am79C982	basic Integrated Multiport Repeater (bIMR™)
Am79C983	Integrated Multiport Repeater 2 (IMR2™)
Am79C984A	enhanced Integrated Multiport Repeater (eIMR™)
Am79C985	enhanced Integrated Multiport Repeater Plus (eIMR+™)
Am79C987	Hardware Implemented Management Information Base (HIMIB™)
Am79C988	Quad Integrated Ethernet Transceiver (QuIET™)
Am79C900	Integrated Local Area Communications Controller (ILACC™)
Am79C940	Media Access Controller for Ethernet (MACE™)
Am79C960	PCnet™-ISA Single-Chip Ethernet Controller (for ISA bus)
Am79C961	PCnet™-ISA+ Single-Chip Ethernet Controller for ISA (with Microsoft® Plug n' Play® Support)
Am79C961A	PCnet™-ISA II Full Duplex Single-Chip Ethernet Controller for ISA
Am79C965	PCnet™-32 Single-Chip 32-Bit Ethernet Controller
Am79C970	PCnet™-PCI Single-Chip Ethernet Controller (for PCI bus)
Am79C970A	PCnet™-PCI II Full Duplex Single-Chip Ethernet Controller (for PCI bus)
Am79C971B	PCnet™-*FAST* Single-Chip Full-Duplex 10/100 Mbps Ethernet Controller for PCI Local Bus
Am79C974	PCnet™-SCSI Combination Ethernet and SCSI Controller for PCI Systems

CONNECTION DIAGRAM



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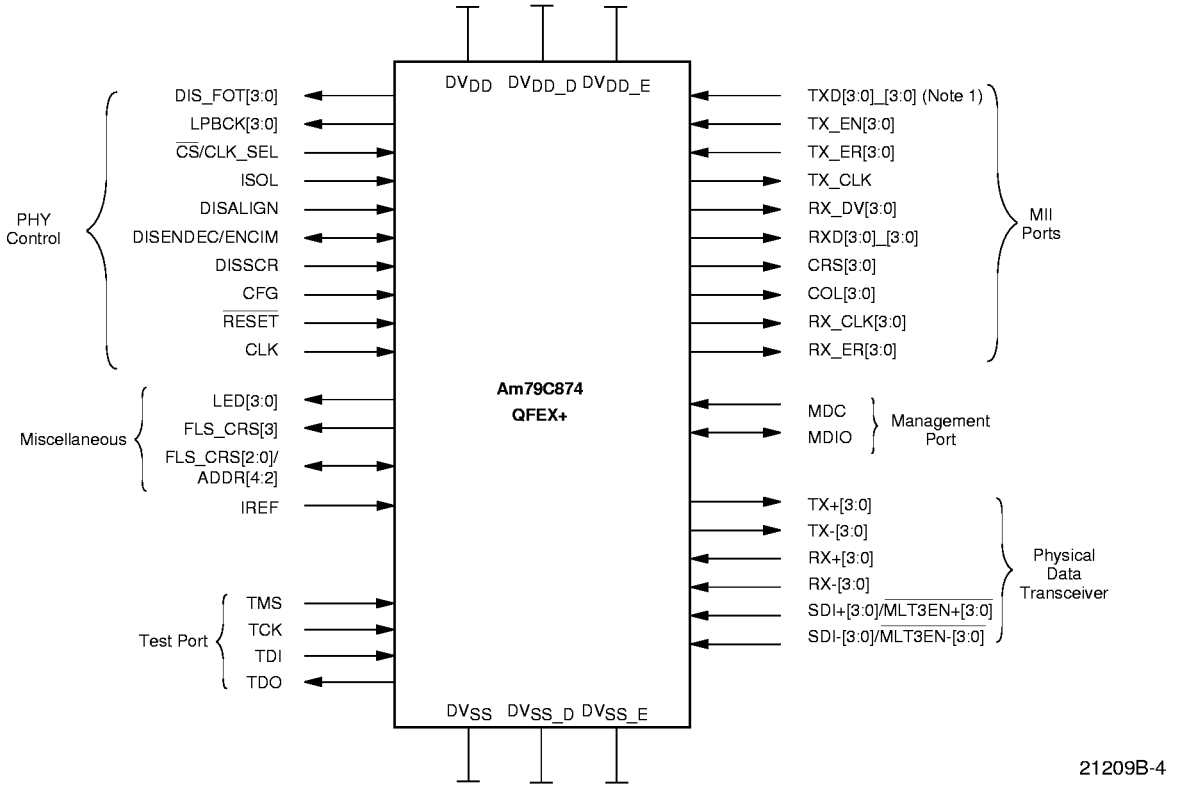
LOGIC SYMBOL



Note:
TXD[2]_[x] = ENRCV[x] when CFG = 1.

TABLE OF CONTENTS

PIN DESIGNATIONS

Listed by Pin Number

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	41	NC	81	NC	121	NC
2	$\overline{CS}$/CLK_SEL	42	LED(0)	82	TX(2)+	122	TDI
3	DVSS	43	LED(1)	83	DVDD_E2	123	TCK
4	ISOL	44	LED(2)	84	TX(2)-	124	TMS
5	RX_DV(1)	45	LED(3)	85	SDI(2)+/ $\overline{MLT3EN(2)+}$	125	$\overline{RESET}$
6	RX_CLK(1)	46	DVSS	86	SDI(2)-/ $\overline{MLT3EN(2)-}$	126	TXD(3)_[2]
7	RX_ER(1)	47	DVDD	87	RX(2)+	127	TXD(3)_[3]
8	DVSS	48	LPBCK(0)	88	DVSS_E2	128	DVSS
9	TX_ER(1)	49	DIS_FOT(0)	89	RX(2)-	129	DVSS
10	TX_EN(1)	50	LPBCK(1)	90	NC	130	FLS_CRS(2)/ ADDR(4)
11	DVDD	51	DIS_FOT(1)	91	TX(3)+	131	RXD(2)_[3]
12	TXD(1)_[0]	52	LPBCK(2)	92	DVDD_E3	132	RXD(2)_[2]
13	TXD(1)_[1]	53	DIS_FOT(2)	93	TX(3)-	133	RXD(2)_[1]
14	TXD(1)_[2]	54	LPBCK(3)	94	SDI(3)+/ $\overline{MLT3EN(3)+}$	134	RXD(2)_[0]
15	TXD(1)_[3]	55	DIS_FOT(3)	95	SDI(3)-/ $\overline{MLT3EN(3)-}$	135	CRS(2)
16	FLS_CRS(0)/ ADDR(2)	56	CFG	96	RX(3)+	136	COL(2)
17	RXD(0)_[3]	57	DVDD_D	97	DVSS_E3	137	RX_DV(2)
18	RXD(0)_[2]	58	DVSS_D	98	RX(3)-	138	RX_CLK(2)
19	RXD(0)_[1]	59	DISALIGN	99	NC	139	RX_ER(2)
20	RXD(0)_[0]	60	NC	100	DISSCR	140	TX_ER(2)
21	DVSS	61	NC	101	DISENDEC/ ENCIM	141	TX_EN(2)
22	NC	62	TX(0)+	102	RXD(3)_[3]	142	CLK
23	DVDD	63	DVDD_E0	103	RXD(3)_[2]	143	TXD(2)_[0]/ ENRCV(0)
24	CRS(0)	64	TX(0)-	104	RXD(3)_[1]	144	TXD(2)_[1]/ ENRCV(1)
25	COL(0)	65	SDI(0)+/ $\overline{MLT3EN(0)+}$	105	RXD(3)_[0]	145	TXD(2)_[2]/ ENRCV(2)
26	RX_DV(0)	66	SDI(0)-/ $\overline{MLT3EN(0)-}$	106	DVSS	146	TXD(2)_[3]/ ENRCV(3)
27	RX_CLK(0)	67	RX(0)+	107	FLS_CRS(3)	147	DVSS
28	RX_ER(0)	68	DVSS_E0	108	CRS(3)	148	FLS_CRS(1)/ ADDR(3)
29	TX_ER(0)	69	RX(0)-	109	COL(3)	149	DVDD
30	DVSS	70	NC	110	RX_DV(3)	150	MDIO
31	DVDD	71	NC	111	RX_CLK(3)	151	MDC
32	TX_CLK	72	TX(1)+	112	RX_ER(3)	152	DVDD
33	TX_EN(0)	73	DVDD_E1	113	TX_ER(3)	153	DVSS
34	TXD(0)_[0]	74	TX(1)-	114	TX_EN(3)	154	RXD(1)_[3]
35	TXD(0)_[1]	75	SDI(1)+/ $\overline{MLT3EN(1)+}$	115	TXD(3)_[0]	155	RXD(1)_[2]
36	TXD(0)_[2]	76	SDI(1)-/ $\overline{MLT3EN(1)-}$	116	TXD(3)_[1]	156	RXD(1)_[1]
37	TXD(0)_[3]	77	RX(1)+	117	DVSS	157	RXD(1)_[0]

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
38	DVSS	78	DVSS_E1	118	DVDD	158	CRS(1)
39	IREF	79	RX(1)-	119	TDO	159	COL(1)
40	NC	80	NC	120	NC	160	NC

Note:
NC= no connect.

PIN DESCRIPTION

Network Interfaces

The QFEX+ device provides four 100BASE-X ports.

TX[3:0]+, TX[3:0]-
Serial Transmit Data
MLT-3/PECL Output

These pins are the 100BASE-X port differential drivers, one pair per port. For 100BASE-FX, these transmit outputs carry differential PECL-level NRZI data for direct connection to an external fiber optic transceiver. They can be forced to logical 0 (TX+ low, TX- high) by programming the TX_DISABLE bit (bit 3 of the PHY Control/Status Register, Register 17). For 100BASE-TX, these pins carry MLT-3 data and are connected to the primary side of the magnetics module.

RX[3:0]+, RX[3:0]-
Serial Receive Data
MLT-3/PECL Input

These pins are the 100BASE-X port differential receiver pairs, one pair for each port. They receive MLT-3 data and are connected to the receive side of the magnetics module in 100BASE-TX operation. They receive PECL NRZI data from an external fiber optic transceiver in 100BASE-FX application.

DIS_FOT[3:0]
Disable Fiber Optic Transceiver
Output

This output provides a means for the user to control the external fiber optic module. It is used to force the external fiber optic transceiver to output the fiber dark condition. This pin reflects the status of the DIS_FOT bits (bit 5 of PHY Control/Status Register, Register 17) of the corresponding ports.

LPBCK[3:0]
Loopback
Output

This output provides a means for the user to control the PMD transceivers. Each port has a dedicated pin to connect to its transceiver, and it is used to force the PMD device to loopback the transmit data. This pin reflects the status of the Loopback bit (bit 14 of MII Control Register, Register 0) of the corresponding port.

SDI[3:0]+/$\overline{\text{MLT3EN[3:0]}}$+, SDI[3:0]-/$\overline{\text{MLT3EN[3:0]}}$-
Signal Detect/MLT3 Select
PECL Input

These pins control the selection, on a per port basis, between PECL and MLT-3 data for the TX± and RX± pins. For 100BASE-TX, both of these pins should be tied to ground. This enables transmission and reception of MLT-3 signals at the TX± and RX± pins. For 100BASE-FX, these pins are biased at PECL levels. They are connected to the SDI± pins from the optical transceiver modules to indicate whether the received signal is above the required threshold. There is one SDI pair per port.

Table 1. SDI[3:0]± Settings for Transceiver Operation

SDI[x]+	SDI[x]-	Port Mode
DV_{SS}	DV_{SS}	MLT-3 Mode
PECL Bias	PECL Bias	PECL Mode

Note:
PECL Bias is V_{CC} - 2V.

Media Independent Interface

TX_CLK
Transmit Clock
Output

TX_CLK (Transmit Clock) is a continuous clock that provides the timing reference for TX_EN[3:0], TXD[3:0], and TX_ER[3:0] signals from the Reconciliation sublayer to the PHY. TX_CLK is sourced by the QFEX+ device. The four ports of the QFEX+ device share the same TX_CLK.

RX_CLK[3:0]
Receive Clock
Output

RX_CLK (Receive Clock) is a clock that provides the timing reference for RX_DV, RXD[3:0], and RX_ER signals from the PHY to the Reconciliation sublayer. RX_CLK is sourced by the QFEX+ device. The four ports of the QFEX+ device have independent RX_CLK pins providing continuous clock sources for received data.

RX_CLK is a 25-MHz clock recovered from the received serial data stream, and it is not a 50-percent duty cycle clock. Refer to the timing specification section.

In Shared MII mode, (the CFG pin set HIGH at reset), the RX_CLK[3:2] signal will always be in a high impedance state. The RX_CLK[1:0] functionality is under the control of the MII_SELECT bit (bit 0 of the Configuration Register, Register 22) and the ENRCV[3:0] pins. The MII_SELECT bit determines whether the receive clock for a network port is mapped to RX_CLK[0] or RX_CLK[1]. The assertion of the control signal ENRCV[3:0] decides which QFEX+ port supplies the RX_CLK output. At any given time, only one port can put its receive clock out on RX_CLK[0] or RX_CLK[1]. Thus, when two ports are mapped to the same MII, both of their ENRCV signals cannot be asserted at the same time. If no ports are mapped to MII[0] or MII[1] have ENRCV asserted, then the corresponding RX_CLK pin for the MII will be in high impedance state. Therefore, it is recommended that RX_CLK[1:0] should

be pulled LOW through a 20-kΩ or larger resistor in Shared MII mode.

2 provides the RX_CLK[3:0] pin functionality.

Table 2. RX_CLK[3:0] Pin Functionality

Pin	MII_SELECT Bit	CFG Pin	Functionality Description
RX_CLK[3:0]	X	0	Receive Clock at the MII from port[0], port[1], port[2] and port[3].
RX_CLK[0]	0	1	Receive Clock at the MII from any one of the four ports that are mapped to MII[0]. ENRCV[3:0] decides which port's receive clock is presented at the MII[0].
RX_CLK[1]	1	1	Receive Clock at the MII from any one of the four ports that are mapped to MII[1]. ENRCV[3:0] decides which port's receive clock is presented at the MII[1].
RX_CLK[3:2]	X	1	High Impedance State.

TX_EN[3:0]
Transmit Enable
Input

TX_EN indicates that the Reconciliation sublayer is presenting nibbles on the MII port for transmission. The four ports of the QFEX+ device have independent TX_EN pins, and each signal determines whether the corresponding port transmits the data on TXD[3:0].

TXD[3:0]_[3:0]
Transmit Data
Input

TXD[3:0] is a set of four data signals driven by the Reconciliation sublayer. The four ports of the QFEX+ device have an independent set of TXD pins, i.e., TXD[X]_[3:0], where X = 0, 1, 2, or 3.

In Symbol mode, TXD[ ]_[3:0] become the inputs for the lower bits of the symbol data, SYMBOL_IN[3:0], for each port. The following shows how the 5-bit symbol signals are mapped on the MII signals:

SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]},

SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}.

In Shared MII mode, any one of the four ports can accept data from TXD[0]_[3:0] or TXD[1]_[3:0], based on the MII_SELECT bit (bit 0 of the Configuration Register, Register 22). The individual TX_EN signals decide to which port the data stream is transmitted. TXD[2]_[3:0] pins are used as ENRCV[3:0] in Shared MII mode. 3 provides TXD[3:0]_[3:0] pin functionality.

Table 3. TXD[3:0]_[3:0] Pin Functionality

Pin	MII_SELECT Bit	CFG Pin	Functionality Description
TXD[3:0]_[3:0]	X	0	Transmit Data at the MII for port[0], port[1], port[2], and port[3].
TXD[0]_[3:0]	0	1	Transmit Data at the MII for any of the four ports that are mapped to MII[0]. TX_EN[3:0] decides which port will transmit the data from the TXD[0][3:0] signal interface.
TXD[1]_[3:0]	1	1	Transmit Data at the MII for any of the four ports that are mapped to MII[1]. TX_EN[3:0] decides which ports will transmit the data from the TXD[1][3:0] signal interface.
TXD[2]_[3:0]	X	1	Used as ENRCV[3:0].
TXD[3]_[3:0]	X	1	Ignored by the QFEX+ device.

Note:
If no ports are mapped to either MII[0] or MII[1], then the corresponding TXD[3:0] pin will be ignored by QFEX+ device.

TX_ER[3:0]
Transmit Coding Error
Input

TX_ER, when asserted for one or more TX_CLK periods while TX_EN is active, causes the QFEX+ device to transmit a non-data, invalid code-group. The four ports of the QFEX+ device have independent TX_ER pins.

In Symbol mode, TX_ER becomes the input for the fifth bit of the symbol data, SYMBOL_IN[4], for each port.

The following shows how the 5-bit symbol signals are mapped on the MII signals:

SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]},

SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}.

RX_DV[3:0]
Receive Data Valid
Output

RX_DV signal indicates which port of the QFEX+ device is presenting recovered and decoded 4-bit data on RXD[3:0]. The four ports of the QFEX+ device have independent RX_DV pins in Independent MII mode.

In Shared MII mode, the RX_DV[1:0] functionality is under the control of the MII_SELECT bit (bit 0 of the Configuration Register, Register 22) and the ENRCV[3:0] pins. The MII_SELECT bit determines which MII port (RX_DV[1] or RX_DV[0]) the receive data valid signal is mapped to. The assertion of the control signal ENRCV[3:0] decides which port drives RX_DV[0] or RX_DV[1]. If two ports are mapped to the same MII, both of their ENRCV signals cannot be asserted at the same time. If no ports that are mapped to MII[0] or MII[1] have ENRCV asserted, then the corresponding RX_DV pin for the MII will be in high impedance state. Therefore, it is recommended that RX_DV[1:0] should be pulled LOW through a 20 kΩ or larger resistor.

The RX_DV[3:2] signal interface will always be in the high impedance state and should not be used in Shared MII mode.

Table 4. RX_DV[3:0] Pin Configuration

Pin	MII_SELECT Bit	CFG Pin	Functionality Description
RX_DV [3:0]	X	0	Receive Data Valid at the MII from port[0], port[1], port[2] and port[3].
RX_DV [0]	0	1	Receive Data Valid at the MII from any one of the four ports that are mapped to MII[0]. ENRCV[3:0] decides which port will drive RX_DV[0] at the MII.
RX_DV [1]	1	1	Receive Data Valid at the MII from any one of the four ports that are mapped to MII[1]. ENRCV[3:0] decides which port will drive RX_DV[1] at the MII.
RX_DV [3:2]	X	1	High Impedance State.

RXD[3:0]_[3:0]
Receive Data
Output

RXD is a set of four data signals driven by the device to transfer recovered data to the Reconciliation sublayer. The four ports of the QFEX+ device have an independent set of RXD pins, i.e., RXD[X]_[3:0], where x = 0, 1, 2, or 3.

When the disable data alignment or disable 4B/5B encoder/decoder feature is used, RXD[ ]_[3:0] become the outputs for the lower bits of the symbol data, SYMBOL_OUT[3:0], for each port.

The following shows how the 5-bit symbol signals are mapped on the MII signals:

SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]},

SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}.

Table 5. RXD[3:0]_[3:0] Pin Configuration

Pin	MII_SELECT Bit	CFG Pin	Functionality Description
RXD[3:0]_[3:0]	X	0	Receive Data at the MII from port[0], port[1], port[2] and port[3].
RXD[0]_[3:0]	0	1	Receive Data from the port whose MII_SELECT bit is set to 0. ENRCV[3:0] decides which port will present data to RXD[0][3:0] at the MII.
RXD[1]_[3:0]	1	1	Receive Data from the port whose MII_SELECT bit is set to 1. ENRCV[3:0] decides which port will present data to RXD[1][3:0] at the MII.
RXD[3:2]_[3:0]	X	1	High Impedance State

In Shared MII mode, the RXD[1:0]_[3:0] pins are under the control of the MII_SELECT bit 0 of the Configuration Register, Register 22) and the ENRCV[3:0] pins.

The MII_SELECT bit decides which MII port (RXD[0][3:0] or RXD[1][3:0]) the receive data stream will be presented to. The assertion of the control signal ENRCV[3:0] decides which port of the QFEX+ drives these outputs. At any given time, only one port can drive the RXD[0][3:0] or the RXD[1][3:0] signals. Therefore, if two ports are mapped to the same MII, both of their ENRCV signals cannot be asserted at the same time. If no ENRCV[3:0] signals are asserted, the RXD[1:0][3:0] signals will be in the high impedance state.

RXD outputs are also used with RX_DV and RX_ER to indicate a False Carrier Condition (see pin description for FLS_CRS[3:0]).

The RXD[3:2]_[3:0] signals will always be in the high impedance state and should not be used in Shared MII mode.

RX_ER[3:0]
Receive Error
Output

RX_ER is driven by the QFEX+ device for one or more RX_CLK periods to indicate to the Reconciliation sublayer that an error (usually an invalid symbol) was detected in the frame presently being transferred. The four ports of the QFEX+ device have independent RX_ER pins.

When the disable data alignment or disable 4B/5B encoder/decoder feature is used, RX_ER becomes the output for the 5th bit of the symbol data, SYMBOL_OUT[4], for each port.

The following shows how the 5-bit symbol signals are mapped on the MII signals:

SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]},

SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}.

In Shared MII mode, the RX_ER[1:0] functionality is under the control of the MII_SELECT bit (bit 0 of the Configuration Register, Register 22) and the ENRCV[3:0] pins. The MII_SELECT bit determines which MII port (RX_ER[1] or RX_ER[0]) the signal is mapped to. The assertion of the control signal ENRCV[3:0] decides which port of the QFEX+ drives the RX_ER[0] or RX_ER[1] output. If two ports are mapped to the same MII, both of their ENRCV signals cannot be asserted at the same time. If no ports that are mapped to MII[0] or MII[1] has ENRCV asserted, then the corresponding RX_ER pin for the MII will be in high impedance state. Therefore, it is recommended that RX_ER[1:0] should be pulled LOW through a 20 kΩ or larger resistor.

RX_ER is also used with RXD and RX_DV to indicate a False Carrier Condition (see pin description for FLS_CRS[3:0]).

The RX_ER[3:2] signal interface will always be in the high-impedance state and should not be used in Shared MII mode.

Table 6. RX_ER[3:0] Pin Configuration

Pin	MII_SELECT Bit	CFG Pin	Functionality Description
RX_ER[3:0]	X	0	Receive Error at the MII from port[0], port[1], port[2] and port[3].
RX_ER[0]	0	1	Receive Error from the port whose MII_SELECT bit is set to 0. ENRCV[3:0] decides which port will drive RX_ER[0] at the MII
RX_ER[1]	1	1	Receive Error from the port whose MII_SELECT bit is set to 1. ENRCV[3:0] decides which port will drive RX_ER[1] at the MII
RX_ER[3:2]	X	1	High Impedance State

CRS[3:0]
Carrier Sense
Output

The CRS signal is asserted by the QFEX+ device when either the transmit or receive medium is non-idle. If the QFEX+ device is configured to Shared MII mode, the CRS signal is asserted only when receive activity is detected. However, if the TX_CRS_EN bit (bit 2 in PHY Control and Status Register, REG 17) is also set, the CRS signal will be asserted while transmitting or receiving. Note that the TX_CRS_EN bit is ignored when the device is configured to have independent MIIs. The four ports of the QFEX+ device have independent CRS pins.

COL[3:0]
Collision Detected
Output

COL is asserted by the QFEX+ device when activity is detected on the transmit and receive path of the corresponding port. The four ports of the QFEX+ device have independent COL pins. When configured to operate in full-duplex mode (by setting bit 8 of the MII Management

Control Register, Register 0), the COL pin will be logic LOW unless the port is in the collision test state.

MDC
Management Data Clock
Input

MDC is an input to the QFEX+ device and it is the timing reference for transfer of information on the MDIO signal. The four ports of the QFEX+ device share the same MDC pin. The MDC can operate at frequencies up to 12.5 MHz.

MDIO
Management Data Input/Output
Input/Output

MDIO is a bidirectional signal between the QFEX+ device and the management entity. It is used to transfer control and status information between the QFEX+ device and the station management entity. The four ports of the QFEX+ device share the same MDIO pin.

Configuration, Status, and Control Interface

CFG
Configuration
Input

This pin is used to configure the operation mode of the device. It must be tied HIGH or LOW for proper operation. *The status of this pin is latched during the rising edge of the $\overline{RESET}$. After reset, any status change on this pin will not affect the operation mode of the device.* If the CFG pin is HIGH at the rising edge of the $\overline{RESET}$, the device will operate in Shared MII mode; if it is LOW, the device is in Independent MII mode.

ENRCV[3:0]
Enable Receive
Input/Output

The ENRCV[3:0] pins are only available in Shared MII mode since these inputs are multiplexed with TXD[2]_[3:0] in QFEX+ device. ENRCV is an input enable signal to the QFEX+ device for the receive signals RXD[1:0]_[3:0], RX_DV[1:0], RX_ER[1:0], and RX_CLK[1:0]. The four ports of the QFEX+ device have independent enable signals. An active HIGH on this pin will result in the corresponding port's receive signals being presented at MII[0] or MII[1], depending on which MII this port is mapped to.

Note: *Only one ENRCV pin can be active for an MII. If multiple ENRCV pins are asserted and the corresponding ports are mapped to the same MII, the QFEX+ device operation is undefined. If no ENRCV[3:0] signals are asserted, RXD[3:0], RX_DV, RX_ER, and RX_CLK signal interface will be in the high impedance state.*

Table 7. ENRCV[3:0]/TXD[2]_[3:0] Pin Functionality

Pin	CFG Pin	Functionality Description
TXD[2]_[3:0]	0	Configured as independent MII and are TXD[2]_[3:0] inputs.
TXD[2]_[3:0]	1	Configured to share the MII and are ENRCV[3:0] inputs.

DISALIGN
Disable Alignment
Input

When the QFEX+ device is configured to Shared MII mode, the alignment of the receive data stream cannot be disabled. This pin disables the alignment of the data stream in the PCS layer of the 100BASE-X standard. When asserted this pin will disable the alignment for all four ports of the QFEX+ device. The software bit SDISALIGN in the PHY Control/Status register (Register 13, bit 13) should be used to disable the alignment of the data stream on a per port basis. The disabling of alignment is only supported by the QFEX+ device when the CFG pin is sampled logic LOW upon power-up or reset.

The following shows how the 5-bit symbol signals are mapped on the MII signals:

SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]},

SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}.

8 outlines the behavior of the QFEX+ device.

When DISALIGN is enabled, the QFEX+ device will not insert the /J/K/ code-group sequence, and the data stream will not be encoded. In order for a port to transmit the symbol data, its TX_EN signal needs to be asserted, otherwise, IDLE symbols will be sent.

Table 8. DISALIGN Pin and SDISALIGN Bit Functions

DISALIGN Pin	SDISALIGN Bit	Alignment of Data Stream Function
1	x	Disable alignment of the receive data stream for all ports.
0	1	Disable alignment of the receive data stream for the corresponding port.
0	0	Enable alignment of the receive data stream.

DISSCR
Disable Scrambler/Descrambler
Input

When asserted, the DISSCR pin will disable the scrambler/descrambler for all ports of the QFEX+ device. The software bit SDISSCR in the PHY Control/Status register, Register 17, should be used to disable the scrambler/descrambler on a per port basis. 9 outlines the scrambler/descrambler function of the QFEX+ device.

Table 9. DISSCR Pin and SDISSCR Bit Functions

DISSCR Pin	SDISSCR Bit	Scrambler/Descrambler Function
1	x	Disable Scrambler/ Descrambler for all ports
0	1	Disable Scrambler/ Descrambler for the corresponding port
0	0	Enable Scrambler/Descrambler

Note:
The status of this pin is latched during the rising edge of RESET. After reset, any transitions on this pin will not change the behavior of the QFEX+ device with respect to disabling the scrambler/descrambler.

DISENDEC/ENCIM
Disable 4B/5B Coding/Enable CIM
Input/Output

This pin serves different purposes in Independent MII mode or in Shared MII mode.

In Independent MII mode (the CFG is sampled LOW at reset), the status of this pin at the rising edge of the RESET pin determines whether the 4B/5B encoding and 5B/4B decoding are disabled. When HIGH, the 4B/5B encoding/decoding for all four ports of the QFEX+ device is disabled; otherwise, it is enabled. The software bit SDISENC in the PHY Control/Status register (Register 17, bit 15) should be used to disable the 4B/5B encoding/decoding on a per port basis. 10 outlines the differences.

Table 10. DISENDEC Pin and SDISENC Bit Function

DISENDEC Pin	SDISENC Bit	Encoder/Decoder Function
1	x	Disable Encoder/Decoder for all ports
0	1	Disable Encoder/Decoder for the corresponding port
0	0	Enable Encoder/Decoder

When encoding/decoding of the data stream is disabled, the QFEX+ device will map the 5-bit code group to RX_ER and RXD[3:0] at the MII, and accept the 5-bit code-group at the MII from TX_ER and TXD[3:0]. TX_EN must be asserted for a port to transmit the 5-bit data.

When encoding/decoding of data stream is disabled, all the 5-bit symbols recovered from the serial data stream will be presented to the MII without any conversion, but the received 5-bit symbols presented on RX_ER and RXD[3:0] are framed to each symbol boundary, i.e., one whole symbol per cycle (note that this is not true with the Disable Alignment feature).

The following shows how the 5-bit symbol signals are mapped on the MII signals:

SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]},

SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}.

In Shared MII mode, the encoding/decoding of the data stream cannot be disabled. This pin is used to enable the Carrier Integrity Monitor (CIM) function in the QFEX+ device. If this pin is HIGH, the internal CIM is enabled. Refer to the Carrier Integrity Monitor section for the description of the CIM function.

Note that when it is used as DISENDEC, the status of this pin is latched during the rising edge of RESET and, hence, any transitions on this pin after that will not change the behavior of the QFEX+ device. However, when used as ENCIM in Shared MII mode, its status is not latched at reset. So, whenever its status is changed, it turns the CIM on or off.

RESET
Reset
Input

This pin is an active LOW signal. When asserted, it resets the internal registers to their default values and resets all the internal state machines. The reset operation can be asynchronous to the CLK and must be asserted for a minimum of 30 clock cycles or 1.2 µs.

CS/CLK_SEL
Chip Select/Clock Select
Input

This pin has two functions. As CLK_SEL, at the rising edge of RESET, the status of this pin determines whether TX_CLK or CLK is used as the reference for all TXD, TX_ER, and TX_EN signals. If the pin is HIGH at the rising edge of the RESET, all the timing parameters for TXD[3:0], TX_ER[3:0], and TX_EN[3:0] signals use the CLK input signal as the reference; if LOW, the TX_CLK output signal is the reference.

As CS, after RESET goes high, this pin is used to select the transceiver device in assigning the address for each PHY through the management interface. This is done by writing the 5-bit PHY address to the lowest five bits of PHY Management Extension Register, Register 19, for the port, while asserting the CS (active low) of the device. Note that management Register 19, which contains the PHY address, can only be written to when

this pin is asserted. Refer to the *Register Administration for 100BASE-X PHY Device* section for details.

FLS_CRS[3:0]
False Carrier Sense
Input/Output

FLS_CRS is asserted when the QFEX+ device detects a bad carrier without having seen a proper /J/K/ symbol pair. The four ports of the QFEX+ device have independent FLS_CRS pins.

The False Carrier Sense condition is also indicated by presenting 1110 on the RXD[3:0] with the RX_ER asserted and the RX_DV de-asserted.

The FLS_CRS[2:0] functionality is multiplexed with Address Assignment functionality on the same input/output pins. The status of the FLS_CRS[2:0]/ADDR[4:2] pin is latched at the rising edge of $\overline{\text{RESET}}$. The latched data is then programmed into bits 4-2 of the PHY Management Extension Register (Register 19). After reset, the functionality of these pins is for False Carrier Sense indication. These pins should be pulled HIGH or LOW through a 20-kΩ or larger resistor for assigning PHY addresses.

ISOL
Isolate
Input

This pin is used to tristate the MII port. When this pin is asserted, the PHY isolates its data paths from the MII and does not respond to TXD[3:0], TX_EN[3:0], and TX_ER[3:0] inputs. When isolated, it presents high impedance on its TX_CLK, RX_CLK, RX_DV, RX_ER, RXD[3:0], COL[3:0], and CRS[3:0] outputs. Each port will also respond to the corresponding ISOLATE bit in the MII Management Control bit 10, Register 0. 11 outlines the behavior of the QFEX+ device when this pin or the register bit is set.

Table 11. ISOL Pin and Isolate Bit Functions

ISOL pin	Isolate bit	MII Isolation Function
1	1	MII Isolated
0	1	MII Enabled
1	0	MII Enabled
0	0	MII Enabled

The logic to enable the MII is a logical AND between the ISOL pin (note, active high) and the Control Register bit. When the PHY powers up, the ISOL pin should be set HIGH and will be driven LOW when the repeater is ready.

Note: *MII isolation status is reflected in the QFEX+ PHY Control/Status Register bit 0, Register 17.*

ADDR[4:2]
Address Assignment
Input/Output

The ADDR[4:2] pins are used to assign PHY addresses to the QFEX+ device. The lower two bits of the five-bit address are fixed within the QFEX+ device. ADDR[4] is the most significant bit of the five-bit address. The lower two bits are pre-assigned to be 00, 01,10, and 11 for the four ports. The ADDR[4] bit is the first address bit received by the QFEX+ device in the management frame. The ADDR[4:2] bits are latched on the rising edge of $\overline{\text{RESET}}$. The latched data is then programmed into bits 4-2 of the PHY Management Extension Register (Register 19).

The Address Assignment functionality is multiplexed with FLS_CRS[2:0] functionality on the same input/output pin. After reset, the functionality of these pins are used for False Carrier Sense indication. These pins should be pulled HIGH or LOW through 20-kΩ or larger resistors for assigning PHY addresses.

Test Access Port

TMS
Test Mode Select
Input

This pin is a serial input bit stream used to define the specific boundary scan test to be executed. TMS has an internal pull up.

TCK
Test Clock
Input

This pin is the clock input for the boundary scan test mode operation. TCK can operate at frequencies up to 12.5 MHz. TCK has an internal pull up.

TDO
Test Data Output
Output

This pin is the test data output path from the QFEX+ device.

TDI
Test Data Input
Input

This pin is the test data input path to the QFEX+ device. TDI has an internal pull up.

LED Port

LED[3:0]
LED Port
Output

Each LED output from the QFEX+ device is capable of sinking the necessary 12 mA of current to drive an LED directly. There is one LED pin for each of the four ports of the QFEX+ device.

Clock Interface

CLK
TTL/CMOS Clock Input
Input

This input is used for the 25-MHz reference clock. This clock is used to generate the TX_CLK at the MII interface.

Power Supply

DVDD
+5 V Power
Input

There are four DVDD pins on the QFEX+ device. They supply power to the TTL I/O buffers and all the logic blocks of the device except the Physical Data Transceiver (PDX). They must all be connected to a 5 V ±5% source.

DVDD_D
+5 V Power
Input

The DVDD_D pin is the power supply for the PDX block and must be connected to a +5 V ±5% source. It is critical that the signal supplied to this pin is clean to ensure proper performance of the device.

DVDD_E0, DVDD_E1, DVDD_E2, DVDD_E3
+5 V Power
Input

The DVDD_E input pins are the power supply for the PECL and MLT-3 I/O buffers of the four network ports. They must be connected to a +5 V ±5% source. It is critical that the signal supplied to this pin is clean to ensure proper performance of the device.

IREF
Internal Current Reference
Input

This pin serves as an internal current reference for QFEX+ device. This pin must be connected to the same plane as the DVDD_D pin through a 13 kΩ (±1%) resistor.

DVSS
Ground
Input

There are 12 DVSS pins on the QFEX+ device. They are the ground pins for TTL I/O and all the logic blocks of the device except for the PDX block, and they must all be connected to a common external ground reference.

DVSS_D
Ground
Input

The DVSS_D pin is the ground for the PDX block. The signal on this pin needs to be clean to ensure proper performance of the device.

DVSS_E0, DVSS_E1, DVSS_E2, DVSS_E3
Ground
Input

The DVSS_E pins are the ground source for the PECL and MLT-3 I/O buffers of the four network ports. It is critical that the signal supplied to this pin is clean to ensure proper performance of the device.

FUNCTIONAL DESCRIPTION

Overview

The QFEX+ device provides the Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA), and the Physical Medium Dependent (PMD) functionality for 100BASE-X. The QFEX+ device communicates with a Repeater, Switch, or MAC device through the Media Independent Interface (MII).

The QFEX+ device consists of the following functional blocks:

- Media Independent Interface
- Carrier Integrity Monitor
- 100BASE-X block including:
- Transmit and Receive State Machines
- 4B/5B Encoder and Decoder
- Stream Cipher Scrambler and Descrambler
- Link Monitor State Machine
- Far End Fault Indication (FEFI) State Machine
- Physical Data Transceiver (PDX)
- MLT-3 encoder/decoder with adaptive equalization
- IEEE 1149.1-compatible JTAG Controller
- PHY Control and Management

Media Independent Interface

The Media Independent Interface (MII) provides the interconnection between the QFEX+ device and the 100BASE-T Media Access Controller (MAC) or repeater device. The MII is also responsible for the communication between the QFEX+ device and the station management entity (STA). The interface is compatible with the Clause 22 of the IEEE 802.3 standard specification. The QFEX+ device provides flexible MII configurations. It can be configured to Independent MII mode or to Shared MII mode for repeater applications.

Independent MII Mode

When CFG pin is sampled logic LOW during the rising edge of $\overline{\text{RESET}}$, the device is configured with an independent MII for each of the four ports of QFEX+ device. All four ports have their own set of MII signals except TX_CLK. There is only one TX_CLK signal supplying all the ports and one PHY management interface. In this mode, the QFEX+ device operates as four independent PHYs. The functionality of the MII pins complies with the IEEE 802.3 standard.

Shared MII mode

In an Ethernet repeater, packets received from one port are repeated out to all other ports; if more than one port receives activity at the same time, a collision occurs and Jam sequence is transmitted out to all ports. The shared MII is designed to take advantage of this feature of repeaters.

The QFEX+ device has the following MII signals shared among the four ports.

TXD[0/1]_[3:0]	Transmit Data (4-bit)
RXD[0/1]_[3:0]	Receive Data (4-bit)
TX_CLK	Transmit Clock
RX_DV[0/1]	Receive Data Valid
RX_ER[0/1]	Receiver Error
RX_CLK[0/1]	Receive Clock
MDC	Management Data Clock
MDIO	Management Input/Output

The following MII signals are independent for each of the ports:

CRS	Carrier Sense
COL	Collision
TX_EN	Transmit Enable
TX_ER	Transmit Error

The COL and CRS signals are asynchronous and independent for each port. Each TX_EN signal is used to enable transmission of data on one port. The port which is receiving data will not transmit data at the same time unless there is other port activity which will initiate a collision condition. The other ports will repeat the data being received. Since the TXD signals are shared for all ports, the repeater device connected to the MII port is responsible for asserting the appropriate TX_EN[3:0] signals to enable the appropriate port. Each port also has its own TX_ER signal. There is one TX_CLK signal for all four ports since they all will be transmitting the same data out of the PHY.

The receive signals (RXD[3:0], RX_DV, RX_CLK, RX_ER) of the four ports are multiplexed together internally to share one set of MII outputs. This internal MUX is controlled by the ENRCV[3:0] signals. Each ENRCV pin enables the corresponding port receive signals to be used for transferring data to the MII. Only one of the four ENRCV[3:0] pins can be active at any given time. If no ENRCV[3:0] signal is asserted, the RXD[3:0], RX_DV, RX_CLK, and RX_ER signal interface will be in high-impedance state. The repeater device is responsible for driving the ENRCV[3:0] pins.

False Carrier

If False Carrier (bad SSD) is detected on a port, the False Carrier Indication will be presented to the MII for a minimum four RX_CLK cycles. False Carrier Indication is communicated by the following state on the MII signals: RXD[3:0] = 1110, RX_ER = 1, and RX_DV = 0. This is to guarantee that the repeater relies on this code

rather than the FLS_CRS pins to determine the False Carrier Condition. The repeater will be notified of the condition if it asserts the offending port's ENRCV signal within two RX_CLK cycles of the assertion of the CRS.

Carrier Integrity Monitor

The QFEX+ device implements the Carrier Integrity Monitor (CIM) function for repeater applications. The ENCIM input is used to enable or disable the CIM function. If the QFEX+ device is used with a repeater device that supports the CIM function, the internal CIM feature of the QFEX+ device should be disabled. Otherwise, it should be enabled if the CIM function is needed. The following describes how this function is implemented in the QFEX+ device.

There are four CIM state machines in the device, one per port. Each state machine performs the functionality as specified by the 100BASE-X carrier integrity state diagram in the IEEE standard. It monitors the carrier received from the PMD of the port and is responsible for generating the **force_jam** and **isolate** primitives for this port as necessary. When the **force_jam** and **isolate** primitives are both false, the CIM does not interfere with the operation of the port.

CIM Isolation Counter

The CIM Isolation Counter is an 8-bit read-only register (Register 23). Each time the device enters the isolation state, the counter is incremented.

Following a read operation, it is reset back to zero. After reaching the maximum count and a read has not occurred, the counter freezes this value until a read occurs.

100BASE-X MAU

Within the QFEX+ device this block is replicated for each port. The MII signals (that are not shared) within this section of the specification should be taken in context with the port being referred. The 100BASE-X Medium Access Unit (MAU) consists of the following sub-blocks:

- Transmit Process
- Receive Process
- 4B/5B Encoder
- Stream Cipher Scrambler
- 5B/4B Decoder
- Stream Cipher Descrambler
- Serializer/Deserializer and Clock Recovery
- Link Monitor
- Far End Fault Generation and Detection & Code-Group Generator
- MLT-3 encoder/decoder with Adaptive Equalization
- Baseline Restoration

Transmit Process

The transmit process generates code-groups based on TXD[3:0], TX_EN, TX_ER signals on the MII. These code-groups are transmitted by the PDX block. This process is also responsible for frame encapsulation into a Physical Layer Stream, generating the collision signal based on whether a carrier is received simultaneously with transmission and generating the Carrier Sense (CRS) and Collision (COL) signals at the MII. The transmit process is implemented in compliance with the transmit state diagram as defined in Clause 24 of the IEEE 802.3u specification. Figure 1 shows the transmit process.

In Shared MII mode, the CRS signal is asserted only when receive activity is detected. If CRS signal assertion is required during transmit or receive activity when the device is configured to share the MII, then TX_CRS_EN bit (bit 2 in the PHY Control and Status Register, Register 17) must be set. The TX_CRS_EN bit is ignored when the device is configured to Independent MII mode.

Receive Process

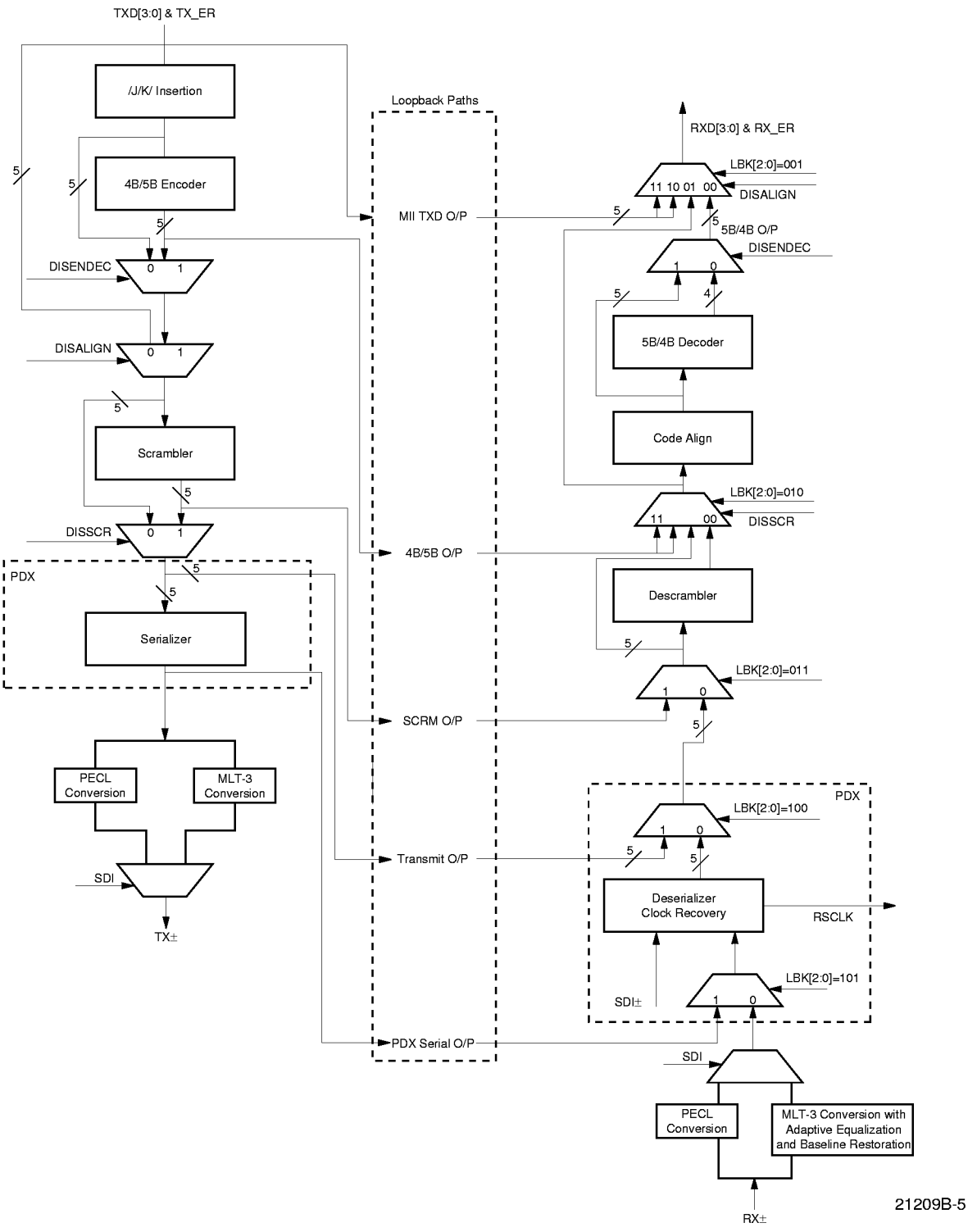
The receive process passes to the MII a sequence of data nibbles derived from the incoming code-groups. Each code-group is comprised of five code-bits. This process detects channel activity and then aligns the incoming code bits in code-group boundaries for subsequent data decoding. The receive process is responsible for code-group alignment and also generates the Carrier Sense (CRS) signal at the MII. The receive process is implemented in compliance with the receive state diagram as defined in Clause 24 of the IEEE 802.3u specification. The False Carrier Indication as specified in the standard is also generated by this block, and communicated to the Reconciliation layer through RXD and RX_ER as well as individual FLS_CRS pins. 1 shows the receive process.

Internal Loopback Paths

As shown in 1, the QFEX+ device provides the following five internal loopback paths for system testing purposes. The different loopback options can be programmed via the LBK[2:0] bits in the PHY Control/Status Register (Register 17) and are indicated below:

- From MII TX_ER, TXD[3:0] to RX_ER, RXD[3:0]
- From the 4B/5B encoder output to the 5B/4B decoder input (after code alignment)
- From the scrambler output to the descrambler input
- From the 5-bit data output to 5-bit data input inside the PDX block
- From PDX serial output to PDX serial input.

For the corresponding LBK settings, refer to the description for the PHY Control/Status Register.



Note:
The 5-bit mode bypasses Encoder/Decoder and Scrambler/Descrambler logic.

Figure 1. Transmit and Receive Data Paths

Encoder

The encoder converts the 4-bit nibble from the MII into five-bit code-groups, using a 4B/5B block coding scheme. The encoder operates on the 4-bit data nibble independent of the code-group boundary. The 100BASE-X physical protocol data unit is called a *stream*. The encoding method used provides the following:

- Adequate codes (32) to provide for all data code-groups (16) plus necessary control code-groups.
- Appropriate coding efficiency (4 data bits per 5 code-bits; 80%) to implement a 100-Mbps physical layer interface on a 125-Mbps physical channel.
- Sufficient transition density to facilitate clock recovery (when not scrambled).

The code-group mapping is defined in 11.

Table 11. Encoder Code-Group Mapping:

MII (TXD[3:0])	Name	PCS Code-Group	Interpretation
0 0 0 0	0	1 1 1 1 0	Data 0
0 0 0 1	1	0 1 0 0 1	Data 1
0 0 1 0	2	1 0 1 0 0	Data 2
0 0 1 1	3	1 0 1 0 1	Data 3
0 1 0 0	4	0 1 0 1 0	Data 4
0 1 0 1	5	0 1 0 1 1	Data 5
0 1 10	6	0 1 1 1 0	Data 6
0 1 1 1	7	0 1 1 1 1	Data 7
1 0 0 0	8	1 0 0 1 0	Data 8
1 0 0 1	9	1 0 0 1 1	Data 9
1 0 1 0	A	1 0 1 1 0	Data A
1 0 1 1	B	1 0 1 1 1	Data B
1 1 0 0	C	1 1 0 1 0	Data C
1 1 0 1	D	1 1 0 1 1	Data D
1 1 1 0	E	1 1 1 0 0	Data E
1 1 1 1	F	1 1 1 0 1	Data F
Undefined	I	1 1 1 1 1	IDLE; used as inter-Stream fill code
0 1 0 1	J	1 1 0 0 0	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
0 1 0 1	K	1 0 0 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
Undefined	T	0 1 1 0 1	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
Undefined	R	0 0 1 1 1	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
Undefined	H	0 0 1 0 0	Transmit Error; used to force signaling errors
Undefined	V	0 0 0 0 0	Invalid Code
Undefined	V	0 0 0 0 1	Invalid Code
Undefined	V	0 0 0 1 0	Invalid Code
Undefined	V	0 0 0 1 1	Invalid Code
Undefined	V	0 0 1 0 1	Invalid Code
Undefined	V	0 0 1 1 0	Invalid Code
Undefined	V	0 1 0 0 0	Invalid Code
Undefined	V	0 1 1 0 0	Invalid Code
Undefined	V	1 0 0 0 0	Invalid Code
Undefined	V	1 1 0 0 1	Invalid Code

Decoder

The decoder performs the 5B/4B decoding of the received code-groups. The five bits of data are decoded into four bits of nibble data. The decoded nibble is then forwarded to the PCS Control block to be sent across the MII to the Repeater, switch, or MAC device. The code-group decoding is shown in 12.

Table 12. Decoder Code-Group Mapping:

PCS Code-Group	Name	MII (RXD[3:0])	Interpretation
1 1 1 1 0	0	0 0 0 0	Data 0
0 1 0 0 1	1	0 0 0 1	Data 1
1 0 1 0 0	2	0 0 1 0	Data 2
1 0 1 0 1	3	0 0 1 1	Data 3
0 1 0 1 0	4	0 1 0 0	Data 4
0 1 0 1 1	5	0 1 0 1	Data 5
0 1 1 1 0	6	0 1 10	Data 6
0 1 1 1 1	7	0 1 1 1	Data 7
1 0 0 1 0	8	1 0 0 0	Data 8
1 0 0 1 1	9	1 0 0 1	Data 9
1 0 1 1 0	A	1 0 1 0	Data A
1 0 1 1 1	B	1 0 1 1	Data B
1 1 0 1 0	C	1 1 0 0	Data C
1 1 0 1 1	D	1 1 0 1	Data D
1 1 1 0 0	E	1 1 1 0	Data E
1 1 1 0 1	F	1 1 1 1	Data F
1 1 1 1 1	I	Undefined	IDLE; used as Inter-Stream fill code
1 1 0 0 0	J	0 1 0 1	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
1 0 0 0 1	K	0 1 0 1	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
0 1 1 0 1	T	Undefined	End-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0 0 1 1 1	R	Undefined	End-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
0 0 1 0 0	H	Undefined	Transmit Error; used to force signaling errors
0 0 0 0 0	V	Undefined	Invalid Code
0 0 0 0 1	V	Undefined	Invalid Code
0 0 0 1 0	V	Undefined	Invalid Code
0 0 0 1 1	V	Undefined	Invalid Code
0 0 1 0 1	V	Undefined	Invalid Code
0 0 1 1 0	V	Undefined	Invalid Code
0 1 0 0 0	V	Undefined	Invalid Code
0 1 1 0 0	V	Undefined	Invalid Code
1 0 0 0 0	V	Undefined	Invalid Code
1 1 0 0 1	V	Undefined	Invalid Code

Scrambler/Descrambler

The 4B/5B encoded data has repetitive patterns which result in peaks in the RF spectrum large enough to keep the system from being approved by regulatory agencies such as the FCC. The peaks in the radiated signal are reduced significantly by scrambling the transmitted signal. Scramblers add the output of a random generator to the data signal so that the resulting signal has fewer repetitive data patterns.

The scrambled data stream is descrambled at the receiver by adding it to the output of another random generator. The receiver's random generator has the same function as the transmitter's random generator. The fact that the random generators are the same and anything exclusive ORed with itself is zero, the output of the descrambler is the original data stream.

Scrambler operation is dictated by the 100BASE-X and TP_PMD standards.

Serializer/Deserializer and Clock Recovery

The Physical Data Transceiver (PDX) is a CMOS all digital core that is used in the QFEX+ device. It employs new circuit techniques to achieve clock and data recovery.

Traditionally, Phase-Locked-Loops (PLLs) are used for the purpose of clock recovery in data communication areas. There are both analog and digital versions of the PLL components such as phase detector, filter, and charge pump. A traditional PLL always contains a voltage-controlled oscillator (VCO) to regenerate a clock which is synchronized in frequency to and aligned in phase with the received data.

The PDX employs techniques that are significantly different from traditional PLLs. Not only are the control functions completely digital, the VCO function is also replaced by a proprietary delay time ruler technique. The result is a highly integratable core which can be manufactured in a standard digital CMOS process.

To transmit, the PDX accepts 4B/5B encoded data symbols from the scrambler. The 5-bit symbol is clocked into the PDX by the rising edge of CLK, serialized, converted to NRZI format and shifted to the outputs or further converted to MLT-3 format. The TX± pair carries PECL-compatible differential NRZI data to the fiber optic transmitter or carries the MLT3 data directly to the magnetics module.

The PDX uses CLK as the frequency and phase reference to generate the serial link data rate. The external clock source must be continuous. All of the internal logic of the PDX runs on an internal clock that is derived from the external reference source. The PDX's clock multiplier is referenced to the rising edges of CLK only.

In order to generate the serial output wave forms conforming to the specifications, the external reference clock must meet 100BASE-X frequency and stability requirements. Under normal conditions, the frequency of CLK must be within the 100BASE-X specified ±100 ppm of the received data for the PDX to operate optimally.

Note: *The 100 ppm is the tolerance of the crystal-controlled source.*

Receiving from the physical medium through the PMD device, the PDX accepts encoded PECL NRZI or MLT-3 signal levels at the RX± inputs. If MLT-3 data is received, it is converted back to NRZI format. The receiver circuit recovers data from the input stream by regenerating clocking information embedded in the serial stream. The recovered clock is called RSCLK (an internal signal). The PDX then clocks the unframed symbol (5 bits) to the descrambler interface on the falling edge of RSCLK.

The PDX receiver uses advanced circuit techniques to extract encoded clock information from the serial input stream and recovers the data. Its operating frequency is established by the reference at CLK. The PDX is capable of recovering data correctly within ±1000 ppm of the 25-MHz CLK signal (which exceeds the frequency range defined by the 100BASE-X specification). The 100BASE-X 4B/5B encoding scheme ensures run-length limitation and adequate transition density of the encoded data stream, while TP-PMD achieves this on a statistical basis through data scrambling. The PDX clock recovery circuit is designed to tolerate a worst-case run-length of 60-bits in order to function correctly with both fiber-optic and twisted-pair PMDs.

The PDX receiver has input jitter tolerance characteristics that meet or exceed the recommendations of Physical Layer Medium Dependent (PMD) 100BASE-X document. Typically, at 125 MBaud (8 ns/bit), the peak-to-peak Duty-Cycle Distortion (DCD) tolerance is 1.4 ns, the peak-to-peak Data Dependent Jitter (DDJ) tolerance is 2.2 ns, and the peak-to-peak Random Jitter (RJ) tolerance is 2.27 ns. The total combined peak-to-peak jitter tolerance is typically 5 ns with a bit error rate (BER) better than 2.5 E-10.

Link Monitor

The Link Monitor process is responsible for determining whether the underlying receive channel is providing reliable data. This process takes advantage of the continuous indication of signal detect by the PMD (PDX & MLT-3). The process sets the link_status to FAIL whenever signal_status is OFF. The link is reliable whenever the signal_status has been continuously ON for about 650 µs. The implementation is in compliance with Clause 24 of the IEEE 802.3 u specification.

The current link status of this port is displayed In the MII Management Status Register (Register 1, bit 2).

Far End Fault Generation and Detection

Far End Fault Generation and Detection is implemented in the QFEX+ device for 100BASE-TX over STP and 100BASE-FX. This block generates a special Far End Fault indication to its far end peer. This indication is generated only when an error condition is detected on the receive channel. When Far End Fault Indication is detected from the far end peer, this block will cause the link monitor to transition the link_status to FAIL. This action in-turn will cause IDLE code-group bits to be automatically transmitted. This is necessary to re-establish communication when the link is repaired. The implementation is in compliance with the Clause 24 of IEEE 802.3u specification.

Far End Fault Indication can be initialized using the PHY Control/Status Register (Register 17, bit 10).

MLT-3 and Adaptive Equalization

This block is responsible for converting the NRZI data stream from the PDX block to a currently sourced MLT-3 encoded data stream. The effect of MLT-3 is the reduction of energy on the media (TX or FX cable) in the critical frequency range of 20 MHz to 100MHz. The receive section of this block is responsible for equalizing and amplifying the received data stream and link detection. The adaptive equalizer compensates for the amplitude and phase distortion due to the cable.

The implementation of this block is in compliance with ANSI X3712 TP-PMD/312, Revision 2.1 that defines a 125-Mbps, full-duplex signalling for twisted pair wiring.

The TX± drivers convert the NRZI serial output to MLT-3 format. The RX± receivers convert the received MLT-3 signals to NRZI. When the TX ports of the QFEX+ device are connected as in 3, the transmit and receive signals will be compliant with IEEE 802.3u Section 25. The required signals (MLT-3) are described in detail in ANSI X3.263:1995 TP-PMD Revision 2.2 (1995).

MLT-3 is a tri-level signal. All transitions are between 0 V and +1 V or 0 V and -1 V. A transition has a logical value of 1 and a lack of a transition has a logical value of 0. The benefit of MLT-3 is that it reduces the maximum frequency over the data line. The bit rate of TX data is 125 Mbps. The maximum frequency (using NRZI) is half of 62.5 MHz. MLT-3 reduces maximum frequency to 31.25 MHz.

A data signal stream following MLT-3 rules is illustrated in 2. The data stream is 101010.

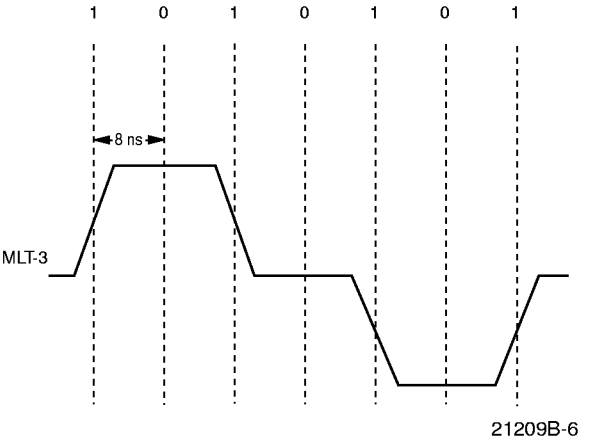


Figure 2. MLT-3 Waveform

MLT-3 connections to the QFEX+ device are shown in 3.

Baseline Restoration

The QFEX+ device includes Baseline Restoration logic for received data.

Baseline restoration corrects a phenomenon called baseline wander. This is essentially a DC shift of a data transmission over copper wire out of normal reference signal levels (e.g., data wanders away from the reference baseline). This shift happens over the time due to data patterns and AC frequencies always present on the line and in transformers. Baseline wander can result in bit errors on a port, which can result in the port being isolated.

Status LED

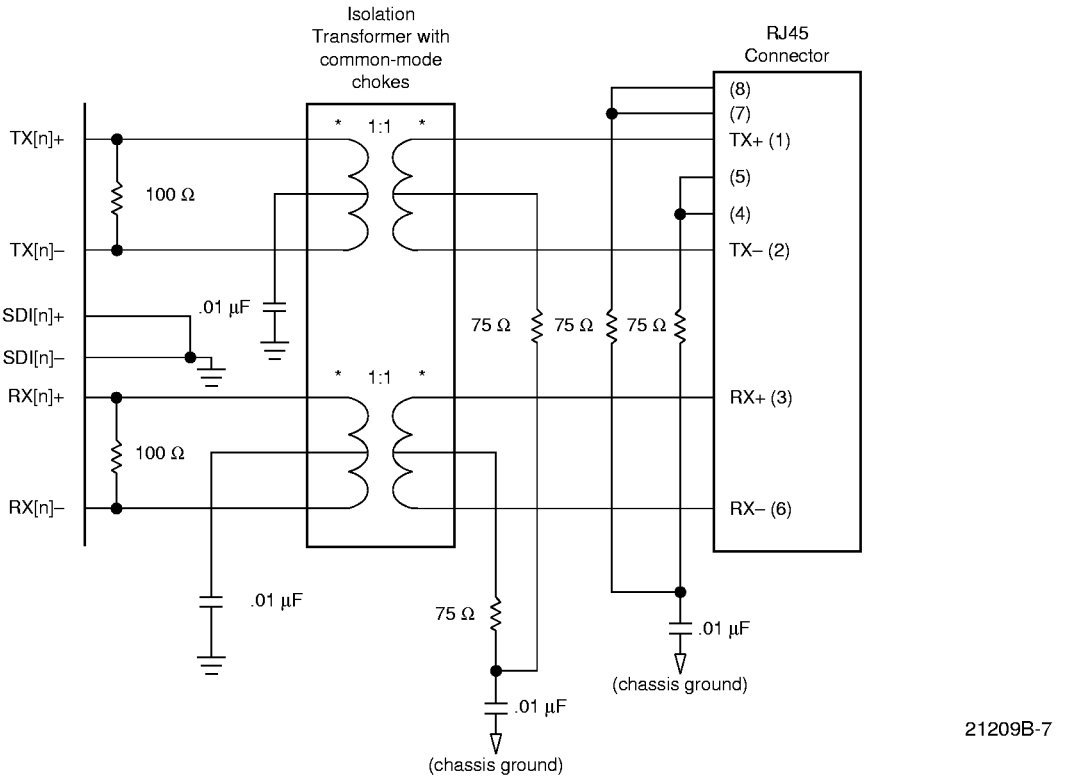
The QFEX+ device can support one LED per port. LED outputs LED[3:0] allow for direct connection of an LED and its supporting pull-up device.

LEDs can be programmed through an LED register to indicate one or more of the following network status or activities: Collision Status, Link Status, Receive Status, Transmit Status, and Signal_Detect. The LED is an open-drain pin (active low). The output can be stretched to allow the human eye to recognize even short events that last only several microseconds. After reset, the LED output is configured as shown in 13.

Table 13. LED Default Configuration

LED Output	Indication	Driver Mode	Pulse Stretch
LED	Link Status	Open Drain - Active Low	Enabled

Each of the status signals is ANDed with its enable signal, and these signals are all ORed together to form a combined status signal. An LED output signal runs to a pulse stretcher, which provides stretched LED output for duration of 42 ms to 63 ms. The pulse stretcher can be disabled by programming the DIS_PS (bit 9 of Register 17).



Notes:

1. *The isolation transformers include common-mode chokes.*
2. *Consult magnetics vendors for appropriate termination schemes.*

Figure 3. TX± and RX± Termination for MLT-3

Reset Operation

The QFEX+ device can be reset in two different ways:

— Hardware Reset, using $\overline{\text{RESET}}$ pin (pin 82)

— Soft Reset, using bit 15 of the MII Control Register (Register 0)

Hardware Reset Function

A complete device reset for all ports can be performed by triggering the $\overline{\text{RESET}}$ pin (pin 82) or following a power-up for at least 1.2 µs or 30 clocks minimum. **This must be done after power-up (DVDD must be constant for 12 clock cycles) and after a clock signal is available.**

All QFEX+ registers are reset to default values. Refer to the individual MII registers for default values.

Note: *The clock recovery section undergoes an internal calibration procedure after hardware reset. Until this has been completed, the QFEX+ device cannot transmit properly.* ***The combined reset and calibration procedure will take approximately 130 clocks.***

The rising edge of $\overline{\text{RESET}}$ latches the configuration of the hardware (external) pins as shown in 14.

Soft Reset Function

The MII Control Register (Register 0) incorporates the soft reset function (bit 15) on a per port basis. It is a read/write register and is self-clearing. Writing a 1 to this bit causes a soft reset or a hardware reset. When read, the register returns a 1 if the soft reset is still being performed; otherwise, it is cleared to 0. *Note that the register can be polled to verify that the soft reset has terminated.* Under normal operating conditions, soft reset will be finished in 18 clock cycles.

Soft reset only resets the QFEX+ device registers to default values (some register bits retain their previous values). Refer to the individual registers for values after a soft reset. The soft reset function does not latch the external configuration of the hardware pins described in 14. It also does not reset the PDX block nor the management interface.

Soft reset is required when changing the value of the SDISSCR (scrambling/descrambling) bit. After soft reset, the register will retain the previous value written.

Table 14. External Pins Latched at Reset

Pin	Pin No.	Action at Reset
CFG	56	If tied high, QFEX+ is in Shared MII mode; else it is in independent MII mode.
DISALIGN	59	If tied high, alignment is off. ***Note:*** SDISALIGN (Reg. 17, bit 13) defaults to 0, or retains any previous value at reset. See Table 7 for DISALIGN and SDISALIGN functions.
DISSCR	100	If tied high, scrambler/ descrambler is off. ***Note:*** SDISSCR (Reg. 17, bit 14) defaults to 0, or retains any previous value at reset. See Table 8 for DISSCR and SDISSCR functions.
DISENDEC/ ENCIM	101	If tied HIGH and CFG=0, 4B/5B encoding/decoding is off. If tied HIGH and CFG=1 (Shared MII mode), CIM is enabled. (CIM state can be changed after reset.)
$\overline{CS}$/ CLK_SEL	2	If tied high, CLK is selected as reference; otherwise, TX_CLK is used as reference.
FLS_CRS[2]/ ADDR[4] FLS_CRS[1]/ ADDR[3] FLS_CRS[0]/ ADDR[2]	130 148 16	Latches bits 4-2 of PHY address into Register 19.

Symbol Interface (PDT/PDR mode)

The QFEX+ device also offers support for a 5-bit symbol interface. The 5-bit symbol interface can be used when no MII interface is available or with other 5-bit interface devices.

In symbol mode, each channel converts the 5-bit code group input into a serial 125 Mbaud NRZI data stream to transmit, also called Physical Data Transmitter mode (PDT). The reverse happens upon receiving in Physical Data Receive (PDR) mode. The PDR mode recovers the 125 MHz clock from the incoming data stream. Since the 5-bit interface passes data from the PHY device unencoded (no 4B/5B process encoding), it expects the layer above it to make sense of the data and to perform any conversion necessary on the data. Thus, PDT/PDR mode only implements clock recovery and serialization/deserialization of data, not a complete PHY function as per the 100BASE-X standard. Of course, PDT/PDR mode is useful in many applications not requiring strict 100BASE-X compatibility.

AMD offers individual PDT/PDR devices for single-port applications. The QFEX+ device can be configured to work as four PDT/PDR pairs, that is, as four 5-bit symbol interfaces.

The QFEX+ device maps the 5-bit symbol interface on the MII signals as follows:

— SYMBOL_IN[4:0] = {TX_ER, TXD[3:0]}

— SYMBOL_OUT[4:0] = {RX_ER, RXD[3:0]}

To configure the QFEX+ device to a four-port PDT/PDR mode, a symbol interface must be configured. **Symbol mode does not use any 4B/5B encoding or alignment, and scrambling must be turned off (DISSCR = 1). TX_EN of all ports must be pulled HIGH. A hardware reset must be issued.**

Table 15. Symbol Mode Operations

DISENDEC Pin	DISALIGN Pin	Function
0	0	Data is aligned and 4B/5B encoded.
0	1	Data is not aligned; **no** 4B/ 5B encoding performed.
1	0	Data is not 4B/5B encoded, but is aligned.
1	1	DISENDEC is ignored. Defaults to DISALIGN enabled: data is not aligned, **no** 4B/5B encoding performed.

Each port can be individually configured to PDT/PDR mode using the SDISSCR, SDISALIGN, and SDISENC bits. A software reset is required to convert that port to symbol mode.

IEEE 1149.1 Compatible JTAG Controller

An IEEE 1149.1-compatible boundary scan Test Access Port is provided for board-level continuity test and diagnostics. All input, output, and input/output pins are tested.

The following is a brief summary of the IEEE 1149.1 compatible test functions implemented in the QFEX+ device. For additional details, consult the IEEE Standard Test Access Port and Boundary-Scan Architecture document (IEEE Standard 1149.1-1990).

The boundary scan test circuit requires four pins (TCK, TMS, TDI and TDO). defined as the Test Access Port (TAP). It includes a finite state machine (FSM), an instruction register, a data register array, and a power on reset circuit. At power up, the FSM goes to reset state. Internal pull-up resistors are provided for the TCK, TDI and TMS pins.

The TAP engine is a 16-state FSM, driven by the Test Clock (TCK), and the Test Mode Select (TMS) pins. An independent power on reset circuit is provided to ensure that the FSM is in the TEST_LOGIC_RESET state at power up.

In addition to the minimum IEEE 1149.1 instruction requirements (EXTEST, SAMPLE and BYPASS), three additional instructions (IDCODE, TRI_ST, and SET_I/O) are provided to further ease board-level testing. All unused instruction codes are reserved.

Instructions Supported

This section describes the public and private instruction that are supported in this implementation. The instruction register is a 4-bit register. The least significant bit of the instruction is the bit nearest the TDO input. The encoding of the instructions is as follows in 16.

Table 16. IEEE 1149.1 Supported Instruction Summary

INST Name	Description	Selected data REG	Mode	INSTCODE
EXTEST	External Test	BSR	TEST	0000
IDCODE	Id Code Inspection	ID REG	NORMAL	0001
SAMPLE	Sample Boundary	BSR	NORMAL	0010
TRI_ST	Force Tristate	BYPASS	NORMAL	0011
SET_I/0	Control Boundary To I/0	BYPASS	TEST	0100
BYPASS	Bypass Scan	BYPASS	NORMAL	1111

EXTEST Instruction

The decoding logic provides signals to control the data flow in the DATA registers according to the current instruction. Each Boundary Scan Register (BSR) cell also has two stages. A flip-flop and a latch are used in the Serial Shift Stage and the Parallel Output Stage, respectively.

There are four possible operational modes in the BSR cell:

— CAPTURE

— SHIFT

— UPDATE

— SYSTEM FUNCTION

The EXTEST instruction is used to test board level interconnect and for testing of circuitry external to the QFEX+ device. This instruction selects the Boundary Scan Register (BSR) for scanning between TDI and TDO when in the Shift-DR controller state. During execution:

1. The QFEX+ outputs are driven from the Parallel Data Register.
2. The QFEX+ internal outputs are sampled into the BSR.
3. The QFEX+ inputs are sampled into the BSR.
4. The QFEX+ internal inputs are driven from the Parallel Data Register.

IDCODE Instruction

The IDCODE instruction is provided for access to the manufacturer's identity, the part number, and the version of the QFEX+ device. This instruction selects the 32-bit identification register for scanning between TDI and TDO in the Shift-DR controller state. The IDCODE instruction is forced into the instruction registers parallel output latches during the Test-Logic-Reset controller state. The 32 bits of the identification register are broken down as shown in 17.

Table 17. Identification Register Bits

Bits	Description
IDREG[31 - 28]	Version (4 bits). The version number for the QFEX+ device is 0h.
IDREG[27-12]	Part Number (16 bits). The part number for QFEX+ device is 8740h.
IDREG[11-1]	Manufacturer ID (11 bits). The manufacturer ID code for AMD is 00000000001 in accordance with JEDEC Publication 106-A.
IDREG[0]	Always a logic 1.

SAMPLE Instruction

The SAMPLE/PRELOAD instruction is used to observe the normal operation of the QFEX+ device without affecting system operation. It is also used to load values into the Parallel Data Register prior to the selection of another instruction. This instruction selects the BSR for scanning between TDI and TDO during the Shift_DR controller state. During execution:

1. The QFEX+ outputs are driven by the QFEX+ device.
2. The QFEX+ internal outputs are sampled into the BSR.
3. The QFEX+ inputs are sampled into the BSR.
4. The QFEX+ internal inputs are driven from the QFEX+ inputs.

TRI_ST Instruction

The TRI_ST instruction is provided for easy tristate of all QFEX+ outputs. This instruction selects the bypass register for scanning between TDI and TDO during the Shift-DR controller state.

SET_I/O Instruction

The SET_I/O instruction is used to bypass the QFEXr/QFEX+ BSR; data from TDI is passed to TDO directly. At the same time, the data previously stored in the BSRs are passed to their respective outputs. The main purpose of this instruction is to isolate the TDI from the scan chain. The difference between this instruction and the BYPASS instruction is that the latter does not pass BSR values to their respective outputs.

BYPASS Instruction

The BYPASS instruction is used to bypass the QFEX+ BSR and shorten access times to other devices on a board. This instruction selects the bypass register for scanning between the TDI and TDO during the Shift-DR controller state. The QFEX+ device is not otherwise affected by this instruction.

Boundary Scan Cells

In boundary scan, most of the chip input and output latches are linked together to form a scan chain. The main purpose of this is for board level testing. The boundary scan ring order is listed in the 18.

Table 18. Boundary Scan Ring Order

BSR Cell No.	Pin No.	Pin Type	Description
1	126	INPUT	TxD[3]_[2]
2	127	INPUT	TxD[3]_[3]
3,4	130	INOUT	FLS_CRS[2] / ADDR[4]
5	131	OUTPUT	RxD[2]_[3]
6	132	OUTPUT	RxD[2]_[2]
7	133	OUTPUT	RxD[2]_[1]
8	134	OUTPUT	RxD[2]_[0]
9	-----	-----	OE CONTROL (1 TO ENABLE)
10	135	OUTPUT	CRS[2]
11	136	OUTPUT	COL[2]
12	-----	-----	OE CONTROL (1 TO ENABLE)
13	137	OUTPUT	RX_DV[2]
14	138	OUTPUT	RX_CLK[2]
15	139	OUTPUT	RX_ER[2]
16	140	INPUT	TX_ER[2]
17	141	INPUT	TX_EN[2]
18	142	INPUT	CLK
19	143	INPUT	TxD[2]_[0] / ENRCV[0]
20	144	INPUT	TxD[2]_[1] / ENRCV[1]
21	145	INPUT	TxD[2]_[2] / ENRCV[2]
22	146	INPUT	TxD[2]_[3] / ENRCV[3]
23	-----	-----	OE CONTROL (1 TO ENABLE)
24,25	148	INOUT	FLS_CRS[1] / ADDR[3]
26	-----	-----	OE CONTROL (1 TO ENABLE)
27,28	150	INOUT	MDIO
29	151	INPUT	MDC
30	-----	-----	OE CONTROL (1 TO ENABLE)
31	154	OUTPUT	RxD[1]_[3]
32	155	OUTPUT	RxD[1]_[2]
33	156	OUTPUT	RxD[1]_[1]

BSR Cell No.	Pin No.	Pin Type	Description
34	157	OUTPUT	RxD[1]_[0]
35	-----	-----	OE CONTROL (1 TO ENABLE)
36	158	OUTPUT	CRS[1]
37	159	OUTPUT	COL[1]
38	2	INPUT	CS# / CLK_SEL
39	4	INPUT	ISOL
40	5	OUTPUT	RX_DV[1]
41	6	OUTPUT	RX_CLK[1]
42	7	OUTPUT	RX_ER[1]
43	9	INPUT	TX_ER[1]
44	10	INPUT	TX_EN[1]
45	12	INPUT	TxD[1]_[0]
46	13	INPUT	TxD[1]_[1]
47	14	INPUT	TxD[1]_[2]
48	15	INPUT	TxD[1]_[3]
49,50	16	INOUT	FLS_CRS[0] / ADDR[2]
51	17	OUTPUT	RxD[0]_[3]
52	18	OUTPUT	RxD[0]_[2]
53	19	OUTPUT	RxD[0]_[1]
54	20	OUTPUT	RxD[0]_[0]
55	24	OUTPUT	CRS[0]
56	25	OUTPUT	COL[0]
57	-----	-----	OE CONTROL (1 TO ENABLE)
58	26	OUTPUT	RX_DV[0]
59	27	OUTPUT	RX_CLK [0]
60	28	OUTPUT	RX_ER[0]
61	-----	-----	OE CONTROL (1 TO ENABLE)
62	29	INPUT	TX_ER[0]
63,64	32	OUTPUT	TX_CLK
65	-----	-----	OE CONTROL (1 TO ENABLE)
66	33	INPUT	TX_EN[0]
67	34	INPUT	TxD[0]_[0]
68	35	INPUT	TxD[0]_[1]
69	36	INPUT	TxD[0]_[2]

BSR Cell No.	Pin No.	Pin Type	Description
70	37	INPUT	TxD[0]_[3]
71	42	OUTPUT	LED[0]
72	43	OUTPUT	LED[1]
73	44	OUTPUT	LED[2]
74	45	OUTPUT	LED[3]
75	48	OUTPUT	LPBCK[0]
76	49	OUTPUT	DISFOT[0]
77	50	OUTPUT	LPBCK[1]
78	51	OUTPUT	DISFOT[1]
79	52	OUTPUT	LPBCK[2]
80	53	OUTPUT	DISFOT[2]
81	54	OUTPUT	LPBCK[3]
82	55	OUTPUT	DISFOT[3]
83	56	INPUT	CFG
84	59	INPUT	DISALIGN
85	100	INPUT	DISSCR
86	-----	-----	OE CONTROL (1 TO ENABLE)
87,88	101	INOUT	DISENDEC / ENCIM
89	102	OUTPUT	RxD[3]_[3]
90	103	OUTPUT	RxD[3]_[2]
91	104	OUTPUT	RxD[3]_[1]
92	105	OUTPUT	RxD[3]_[0]
93	107	OUTPUT	FLS_CRS[3]
94	-----	-----	OE CONTROL (1 TO ENABLE)
95	108	OUTPUT	CRS[3]
96	109	OUTPUT	COL[3]
97	-----	-----	OE CONTROL (1 TO ENABLE)
98	110	OUTPUT	RX_DV[3]
99	111	OUTPUT	RX_CLK[3]
100	112	OUTPUT	RX_ER[3]
101	113	INPUT	TX_ER[3]
102	114	INPUT	TX_EN[3]
103	115	INPUT	TxD[3]_[0]
104	116	INPUT	TxD[3]_[1]

Note:
BSR cells not in table are not used. However, because they are in the scan chain they exist, but any results from the cells should be ignored.

PHY Control and Management Block (PCM Block)

Register Administration for 100BASE-X PHY Device

The management interface specified in Clause 22 of the IEEE 802.3u standard provides for a simple two wire, serial interface to connect a management entity and a managed PHY for the purpose of controlling the PHY and gathering status information. The two lines are Management Data Input/Output (MDIO), and Management Data Clock (MDC). A station management entity which is attached to multiple PHY entities must have prior knowledge of the appropriate PHY address for each PHY entity. The ADDR[4:2] pins are used to assign addresses to each PHY within the QFEX+ device. The lower two bits of the five-bit address is fixed within the QFEX+ device. ADDR[4] is the most significant bit of the five-bit address. The lower two bits are pre-assigned to be 00, 01,10,11 for the four ports. The ADDR[4] bit is the first bit received by the QFEX+ device in the management frame. The ADDR[4:2] bits are latched on the rising edge of $\overline{\text{RESET}}$. The address is then programmed into the PHY Management Extension Register (Register 19).

The QFEX+ device also provides a methodology for the station management entity to dynamically assign PHY addresses to the multiple PHY entities using the management frames.

Description of the Methodology

The management interface physically transports management information across the MII. The information is encapsulated in a frame format as specified in Clause 22 of IEEE 802.3u draft standard and is shown in 19.

Table 19. Clause 22 Frame Format

	PRE	ST	OP	PHYAD	REGADD	TA	DATA	IDLE
READ	1..1	01	10	AAAAA	RRRRR	Z0	D.....D	Z
WRITE	1..1	01	01	AAAAA	RRRRR	10	D.....D	Z

The PHYAD field, which is five bits wide, allows 32 unique PHY addresses. The managed PHY layer device that is connected to a station management entity via the MII interface has to respond to transactions addressed to the PHY's address. A station management entity attached to multiple PHYs, such as in a managed 802.3 Repeater or Ethernet switch, is required to have prior knowledge of the appropriate PHY address.

PHY Address Assignment Through the MDIO

The QFEX+ device provides an alternative way to assign addresses to each port using the management interface. The $\overline{\text{CS}}$ pin is used to facilitate this operation. The management entity transmits a management frame with the address to be assigned to the PHY in the DATA field of the frame while asserting the $\overline{\text{CS}}$ pin. The structure of the management frame is defined in 20. 4 shows the PHY Management read and write operations.

Bits 6 and 5 in the DATA field select the appropriate port within the QFEX+ device. The selected port will then program its PHY ADDRESS bits in the PHY Management Extension Register (Register 19) with the data in the DATA field (bits 4:0) and will respond to the management frames with that address in the PHYAD field transmitted by the management entity.

Note: *In order to program all four PHY ports, each PHY port requires an independent address when using this alternate method.*

Bad Management Frame Handling

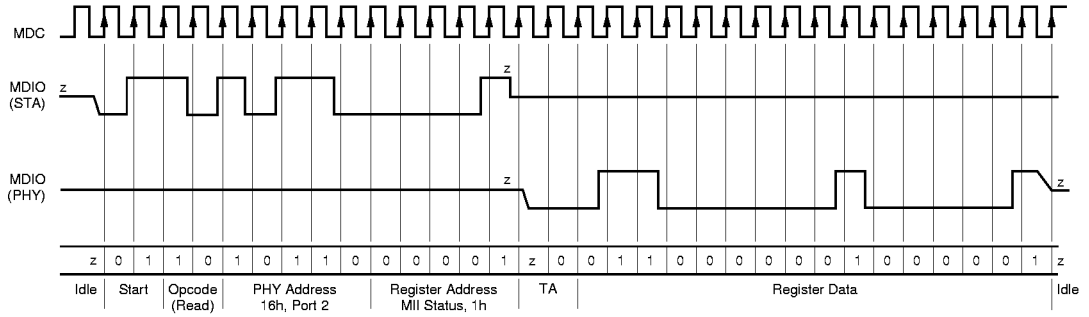
The management block of the device can recognize management frames without preambles (preamble suppression). However, if it receives a bad management frame, it will go into a Bad Management Frame state. It will stay in this state and will not respond to any management frame without preambles until a frame with a full 32-bit preamble is received, then it will return to normal operation.

Table 20. Management Frame Structure

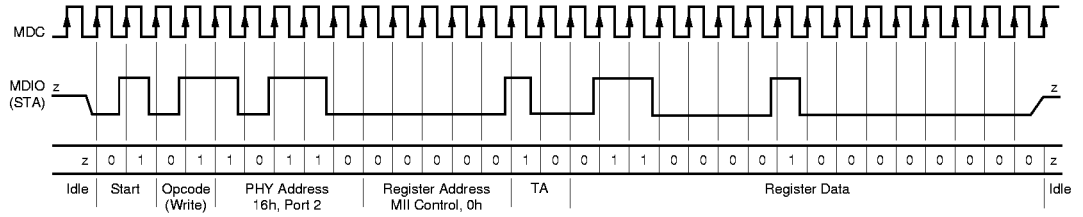
	PRE	ST	OP	PHYAD	REGADD	TA	DATA	IDLE
READ	1..1	01	10	00000	RRRRR	Z0	XXXXXXXXXPPAAAAA	Z
WRITE	1..1	01	01	00000	RRRRR	10	XXXXXXXXXPPAAAAA	Z

A bad management frame is a frame that does not comply with the IEEE standard specification. It can be one with less than 32-bit preamble, with illegal OP field, etc. However, a frame with more than 32 preamble bits is considered to be a good frame.

When a bad management frame is received, the Management Frame Format bit (bit 5 of the Management Extension Register, Register 19) of every port will be set. This bit will be cleared after it is read.



a. Read Operation



b. Write Operation

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Figure 4. PHY Management Read and Write Operations

MII Management Registers

The QFEX+ device supports ten physical registers per port. Therefore, there are 40 registers in each QFEX+ device.

A specific PHY register is identified in a management frame by its 5-bit PHY address and 5-bit register address. The PHY addresses can be assigned by the user in two ways:

1. By setting the ADDR[4:2] pin at reset (see ADDR[4:2] pin description section) and
2. By writing a 5-bit value to the lowest five bits of Register 19 through the management port while asserting the $\overline{CS}$ pin. Refer to the *Register Administration for 100BASE-X PHY Device* section for details.

Each PHY supports the MII basic register set and extended register set. Both sets of registers are accessible through the MII Management Interface. As specified in the IEEE standard, the basic register set consists of the Control Register (Register 0) and the Status Register (Register 1). The extended register set consists of Registers 2 to 31.

21 lists all the registers implemented in the device. All the reserved registers should not be written to, and reading them will return a zero value.

MII Management Control Register (Register 0)

The MII Management Control Register (22) contains both R/W and RO bits. This register is in per port basis, and all the bits are compliant with the IEEE standard specification.

Note: *Since auto-negotiation is not implemented in the device, bits 9 and 12 are read-only.*

Table 21. QFEX+ MII Management Register Set

Register Address	Register Name	Basic/Extended
0	MII Control	B
1	MII Status	B
2-3	PHY Identifier	E
4-16	Reserved	E
17	PHY Control/Status	E
18	Descrambler Resynch. Timer	E
19	PHY Management Extension	E
20	Reserved	E
21	LED	E
22	Configuration	E
23	CIM_Isolate Counter	E
24-31	Reserved	E

Table 22. MII Management Control Register (Register 0)

Reg	Bits	Name	Description	Read/Write (Note 1)	Default Value	Soft Reset
0	15	Soft Reset (Note 2)	When write: 1 = PHY software reset, 0 = normal operation. When read: 1 = reset in process, 0 = reset done.	R/W, SC	0	0
0	14	Loopback	1 =asserts the external LPBCK, 0 = deasserts the external LPBCK	R/W	0	0
0	13	Speed Selection	1 = 100 Mb/s, 0 = 10 Mbps	RO	1	1
0	12	Auto-Negotiation Enable	1 = enable Auto-Negotiation, 0 = disable Auto-Negotiation	RO	0	0
0	11	Power Down	1 = power down, 0 = normal operation	R/W	0	0
0	10	Isolate	1 = electrically isolate PHY from MII, 0 = normal operation	R/W	1	1
0	9	Restart Auto-Negotiation	1 = restart Auto-Negotiation, 0 = normal operation	RO	0	0
0	8	Duplex Mode	1 = full duplex, 0 = half duplex	R/W	0	Retains previous value
0	7	Collision Test	1 = enable COL signal test, 0 = disable COL signal test	R/W	0	0
0	6-0	Reserved	Write as 0, ignore on read	R/W	0	0

Notes:

1. *R/W = Read/Write, SC = Self Clearing, RO = Read only.*
2. *Refer to the Reset Section for details on Soft Reset.*

MII Management Status Register (Register 1)

The MII Management Status Register identifies the physical and auto-negotiation capabilities of the local PHY. This register is read only; a write will have no effect. There is one of these registers per network port.

Table 23. MII Management Status Register (Register 1)

Reg	Bits	Name	Description	Read/Write (Note 1)	Default Value
1	15	100BASE-T4	1 = 100BASE-T4 able, 0 = not 100BASE-T4 able	RO	0
1	14	100BASE-X Full Duplex	1 = 100BASE-X full duplex able, 0 = not 100BASE-X full duplex able	RO	1
1	13	100BASE-X Half Duplex	1 = 100BASE-X half duplex able, 0 = not 100BASE-X half duplex able	RO	1
1	12	10 Mbps Full Duplex	1 = 10 Mb/s full duplex able, 0 = not 10 Mb/s full duplex able	RO	0
1	11	10 Mbps Half Duplex	1 = 10 Mb/s full duplex able, 0 = not 10 Mb/x full duplex able	RO	0
1	10-7	Reserved	Ignore when read	RO	0
1	6	MF Preamble Suppression	1 = PHY can accept management (mgmt) frames with or without preamble, 0 = PHY can only accept mgmt frames with preamble	RO	1
1	5	Auto-Negotiation Complete	1 = Auto-Negotiation completed, 0 = Auto-Negotiation not completed	RO	0
1 (Note 1)	4	Remote Fault	1 = remote fault detected, 0 = no remote fault detected	RO, LH	0
1	3	Auto-Negotiation Ability	1 = PHY able to auto-negotiate, 0 = PHY not able to auto-negotiate	RO	0
1 (Note 1)	2	Link Status	1 = link is up, 0 = link is down	RO, LL	0
1	1	Jabber Detect	1 = jabber condition detected, 0 = no jabber condition detected	RO	0
1	0	Extended Capability	1 = extended register capabilities, 0 = basic register set capabilities only	RO	1

Note:
LH = Latching High, LL = Latching Low.

PHY Identifier (Registers 2 and 3)

Registers 2 and 3 contain a unique PHY identifier, consisting of 22 bits of the organizationally unique IEEE Identifier, a 6-bit manufacturer's model number, and a 4-bit manufacturer's revision number. The most significant bit of the PHY identifier is bit 15 of register 2; the least significant bit of the PHY identifier is bit 0 of register 3. Register 2, bit 15 corresponds to bit 3 of the IEEE Identifier and register 2, bit 0 corresponds to bit 18 of the IEEE Identifier. Register 3, bit 15 corresponds to bit 19 of the IEEE Identifier and register 3, bit 10 corresponds to bit 24 of the IEEE Identifier. Register 3, bits 9-4 contain the manufacturer's model number and bits 3-0 contain the manufacturer's revision number. These registers are shown in Tables 14 and 15.

Table 24. PHY Identifier (Register 2)

Reg	Bits	Name	Description	Read/ Write	Default Value	Soft Reset
2	15-0	PHY_ID[31-16]	IEEE Address (bits 3-18); Register 2, bit 15 is MS bit of PHY Identifier	RO	0000000000000000 (0000 Hex)	Retains original Value

Table 25. PHY Identifier (Register 3)

Reg	Bits	Name	Description	Read/Write	Default Value	Soft Reset
3	15-10	PHY_ID[15-10]	IEEE Address (bits 19-24)	RO	011010 (1A Hex)	Retains original value
3	9-4	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	RO	111100 (3C Hex)	Retains original value
3	3-0	PHY_ID[3-0]	Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier	RO	0000	Retains original value

Reserved Registers (Registers 4-16, 20, and 24-31)

The QFEX+ device contains reserved registers at addresses 4-16, 20, and 24-31. These registers should be ignored when read and should not be written at any time.

PHY Control/Status Register (Register 17)

PHY Control/Status Register (shown in 26) has address 17. There are four of these registers in this device, one for each network port. This register is used to control the configuration of the QFEX+ device and to provide status information to the management entity. When configuring the QFEX+ device to disable (scrambling/descrambling), a software reset after a write operation to the appropriate bits in this register is mandatory for proper configuration. The bit assignments are listed in 26.

Note: *LBK[2:0] cases transmit data to the network (e.g., the TX± outputs are switching and transmit any loopback data).*

Table 26. PHY Control/Status Register (Register 17)

Reg	Bits	Name	Description	Read/Write	Default Value	Soft Reset
17	15	SDISENC	1 = disable 4b/5b encoding/decoding (use TX_ER and RX_ER for additional data bit 5); 0 = enable 4b/5b encoding/decoding	R/W	0	Retains Previous Value
17	14	SDISSCR	1 = disable scrambler/descrambler; 0 = enable scrambler/descrambler	R/W	0	Retains Previous Value
17	13:11	SDISALIGN	1 = pass unaligned data to the MII; 0 = enable alignment block	R/W	0	Retains Previous Value
17	10	EN_FEFI	1 = enable FEFI when not in auto-negotiation; 0 = disable FEFI when not in auto-negotiation	R/W	0	0
17	9	DIS_PS	1 = disable Pulse Stretch option of LED output; 0 = enable Pulse Stretch option of LED output	R/W	0	0
17	8:6	LBK[2-0]	000 = normal operation 001 = MII loopback (TXD[3:0], TX_ER to RXD[3:0], RX_ER) 010 = loopback from 4B/5B ENC. output to 5B/4B DEC. input 011 = loopback from scrambler output to descrambler input 100 = loopback through top of PDX 101 = loopback through bottom of PDX (transmit to network) 110 = reserved 111 = reserved	R/W	000	000
17	5	DIS_FOT	1 = Causes the external pin DIS_FOT to be asserted; 0 = Causes the external pin DIS_FOT to be de-asserted	R/W	0	0
17	4	Reserved	Write as 0; ignore on read.	R/W	0	0
17	3	TX_DISABLE	1 = Causes the TX+ to logical “0”; TX- to logical 1. 0 = Default mode. Transmits valid data.	R/W	0	0
17	2	TX_CRS_EN	1 = Causes the CRS to be asserted when transmit or receive medium is non-idle. 0 = Causes the CRS to be asserted when receive medium is non-idle	R/W	0	0
17	1	CIM_ISOLATE	1 = the port has been isolated by the CIM; 0 = not isolated by the CIM.	RO (Note 1)	0	0
17	0	MII Isolated	1 = MII is isolated; 0 = MII is enabled (Note 2)	RO	0/1 (Note 3)	0

Notes:

1. *Cleared when read.*
2. *If both the ISOL pin of the chip and the Isolate bit in Register 0 are 1, this bit will be set.*
3. *This value depends on the status of the ISOL pin.*

Descrambler Resynchronization Timer Register (Register 18)

Descrambler Resynchronization Timer Register (shown in 27) allows the user to program the time it takes for the descrambler to start the resynchronization process. This is to ensure that the Descrambler resynchronizes itself to the next IDLE symbol stream after it receives a packet of excessive length. This register should be programmed as described in the 27. The programmed timer value should always be greater than the length of the maximum size packet in normal operation.

There are four of these registers in this device, one for each network port.

Table 27. Descrambler Resynchronization Timer (Register 18)

Reg	Bits	Name	Description	Read/ Write	Default Value	Soft Reset
18	15-0	Descrambler Resynch Timer	Each bit indicates 4 clocks, or 160 ns. The count decrements from a default value of 1 ms or an initial value loaded by the user. This counter provides a maximum timer value of 10.5 ms.	R/W	000110000 1101010 (Note 1)	0001100 0011010 10 (Note 1)

Note:
The corresponding time to this setting is 1ms.

PHY Management Extension Register (Register 19)

Refer to the *PHY Address Assignment through the MDIO* section at the beginning of this section. 28 contains the PHY Management Extension Register (Register 19) bits.

Table 28. PHY Management Extension Register (Register 19)

Reg	Bits	Name	Description	Read/Write	Default Value	Soft Reset
19	15:6	Reserved	Write as 0, ignore on read.	RO	0	0
19	5	Mgmt Frame Format	1 = last management frame was invalid (opcode error, etc.); 0 = last management frame was valid.	RO	0	0
19	4-0	PHY Address	PHY Address for MII Accesses, can only be modified by asserting $\overline{CS}$.	R/W	AAAXX (Note 1)	Retains Previous Value

Note:
AAA reflects the status of the FLS_CRS[2:0]/ADDR[4:2] pins upon power-up or hardware RESET; XX = 00 for port 0, 01 for port 1, 10 for port 2, 11 for port 3.

LED Register (Register 21)

The LED Register allows the user to set the LED display option, and it also indicates the status of the LED output as described in 29. There are four LED registers, one per port.

Table 29. LED Register (Register 21)

Reg	Bits	Name	Description	Read/Write	Default Value	Soft Reset
21	15	LEDOUT	This bit indicates the current (non-stretched) value of the LED output pin. The value is determined by the settings of the individual enable bits of this register.	RO	0	0
21	14-5	Reserved	Write as 0; ignore on read	RO	0	0
21	4	SIG_DET_EN	1 = Pass SIGNAL DETECT to the LED output; 0 = Do not pass SIGNAL DETECT to the LED output	R/W	0	0
21	3	XMT_EN	1 = Pass Transmit Status to LED output; 0 = Do not pass Transmit Status to LED output	R/W	0	0
21	2	RCV_EN	1 = Pass Receive Status to LED output; 0 = Do not pass Receive Status to LED output	R/W	0	0
21	1	COL_EN	1 = Pass Collision Status to LED output; 0 = Do not pass Collision Status to LED output	R/W	0	0
21	0	LNK_EN	1 = Pass Link Status to LED output; O = Do not pass Link Status to LED output	R/W	1	1

Configuration Register (Register 22)

The Configuration Register (shown in 30) should only be used in Shared MII mode. It is used by the repeater device to program whether MII[0] or MII[1] is the network port it is mapped to. If this port is mapped to MII[0], the packets going in TXD[0]_[3:0] will be transmitted out of this network port, and the packets received from this network port will come out of RXD[0]_[3:0], RX_CLK[0], RX_ER[0] and RX_DV[0]. Similarly, if this port is mapped to MII[1], the packets coming in TXD[1]_[3:0] will be transmitted out of this network port, and the packets received from this network port will come out of RXD[1]_[3:0], RX_CLK[1], RX_ER[1] and RX_DV[1].

Table 30. Configuration Register (Register 22)

Reg	Bits	Name	Description	Read/Write	Default Value	Soft Reset
22	15-1	Reserved	Write as 0; ignore on read	RO	0	0
22	0	MII_SELECT	1 = Port is mapped to MII[1]; 0 = Port is mapped to MII[0]	R/W	0	Retains Previous Value

CIM Isolate Counter (Register 23)

The CIM Isolation Counter is an 8-bit read-only register (Register 23). Each time the device enters the isolation state, the counter is incremented. 31 contains the CIM Isolate Counter (Register 23) bits.

Table 31. CIM Isolate Counter (Register 23)

Reg	Bits	Name	Description	Read/Write	Default Value	Soft Reset
23	7-0	CIM_Isolate Counter	Following a read operation, it is reset back to zero. After reaching the maximum count and a read has not occurred, the counter freezes this value until a read occurs.	RO	0	0

ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature Under Bias . . . . . 0°C to +70°C

Supply Voltage to all D_{VSS} inputs . . . . –0.3 V to +6.0 V

DC Voltage applied to any Pin Referenced to D_{VSS} . . . . . –0.5 V to D_{VDD} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Temperature (TA) . . . . . .0°C to +70°C

Supply Voltages (all D_{VDD}) . . . . . +4.75 V to +5.25 V

Operating ranges define those limits between which functionality of the device is guaranteed.

DC CHARACTERISTICS

Digital I/O

Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Unit
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage		2.0		V
I_{IL}	Input Low Current (Note 1)	D_{VDD}=Maximum, V_{IN} = 0.0 V		–200	µA
I_{IH}	Input High Current (Note 1)	D_{VDD}=Maximum, V_{IN} = 2.7 V		–100	µA
V_{OH}	Output High Voltage (Note 3)	$I_{OH} = -I_{OL}/2$	2.4		V
V_{OL}	Output Low Voltage	I_{OL}=Maximum		0.4	V
I_{OL}	Output Low Current (Note 4)			12.0	mA
I_{OL}	Output Low Current (Note 5)			4.0	mA
I_{OL}	Output Low Current (Note 6)			8.0	mA
I_{OH}	Output High Current (Note 3)			$-I_{OL}/2$	mA
I_{OZ}	Output Leakage Current (Note 2)	0.4 V < V_{OUT} < D_{VDD}	-10	10	µA
I_{IX}	Input Leakage Current (Note 7)	0.0 V < V_{IN} < D_{VDD}	-10	10	µA

Notes:

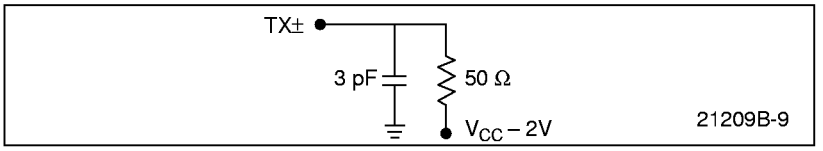
1. *Applies to TMS, TCK, TDI.*
2. *I_{OZ} applies to all three-state output pins and bidirectional pins.*
3. *V_{OH}/I_{OH} does not apply to LED[3:0].*
4. *An I_{OL} value of 12 mA applies to LED[3:0].*
5. *An I_{OL} values of 4.0 mA applies to all signals except those listed in LED[3:0], MDIO, RXD[3:0], RX_CLK, RX_ER, RX_DV, and TX_CLK.*
6. *An I_{OL} value of 8.0 mA applies to MDIO, RXD[3:0], RX_CLK, RX_ER, RX_DV and TX_CLK.*
7. *I_{IX} applies to all non-PECL input-only pins except TMS, TCK, TDI.*

Analog I/O - PECL Mode

Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Unit
V	Input Voltage Range (Note 1)		D_{VDD}-2.0	D_{VDD}	V
V_{OH}	Output High Voltage	PECL Load (Notes 2, 3)	D_{VDD}-1.025	D_{VDD}-0.60	V
V_{OL}	Output Low Voltage	PECL Load (Notes 2, 3)	D_{VDD}-1.81	D_{VDD}-1.62	V
V_{DIFF}	Input Differential Voltage (Note 1)	D_{VDD}=Maximum	0.40	1.1	V

Notes:

1. *Applies to PECL inputs only RX+, RX-, SDI+, SDI-.*
2. *Tested for D_{VDD}=Minimum, shown limits are specified over entire D_{VDD} operating range.*
3. *Applies to PECL outputs TX+,TX- only. Measured with the load shown below:*



Notes:

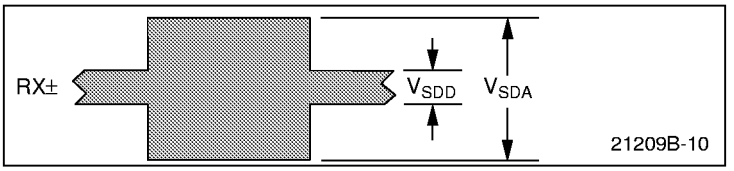
1. *C = 3 pF includes scope probe, wiring, and stray capacitances without device in test fixture.*
2. *AMD uses Automatic Test Equipment (A.T.E.) load configurations and forcing functions. This figure is for reference only.*

Analog I/O - MLT-3 Mode

Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Unit
V_{TXD}	Differential Output Peak Voltage (Note 1)	D_{VDD} = Maximum	950	1050	mV
V_{SDA}	Input Differential Assert Threshold (Note 2)	D_{VDD} = Maximum		750	mV
V_{SDD}	Input Differential Deassert Threshold (Note 2)	D_{VDD} = Maximum	200		mV
I_{IX}	Input Leakage Current	0 V < V_{IN} < D_{VDD}	-10	10	µA

Notes:

1. *V_{TXD} is measured with a 100-Ω termination and a standard Ethernet transformer with a UTP-test load (100Ω) across the secondary winding.*
2. *Receiver Differential Input is shown in the following figure:*



Power Supply Current

Symbol	Parameter Description	Test Conditions	Minimum	Maximum	Unit
I_{CC}	Power Supply Current	V_{DD} = Maximum MLT-3 Mode	–	420	mA
		V_{DD} = Maximum PECL Mode	–	TBD	mA

SWITCHING CHARACTERISTICS

Clocks

No.	Symbol	Parameter Description (Note 1)	Min	Max	Unit
1	t_{PER}	CLK Period	39.996	40.004	ns
2	t_{PWH}	CLK High Pulse Width	18	22	ns
3	t_{PWL}	CLK Low Pulse Width	18	22	ns
4	t_{PER}	TX_CLK Period	39.996	40.004	ns
5	t_{PWH}	TX_CLK High Pulse Width (Note 3)	18	22	ns
6	t_{PWL}	TX_CLK Low Pulse Width (Note 3)	18	22	ns
8	t_{PER}	MDC Period (Note 2)	80		ns
9	t_{PWH}	MDC High Pulse Width	35		ns
10	t_{PWL}	MDC Low Pulse Width	35		ns
11	t_{PER}	RX_CLK Period	40	40	ns
12	t_{PWH}	RX_CLK High Pulse Width (Note 3)	14	18	ns
13	t_{PWL}	RX_CLK Low Pulse Width (Note 3)	22	26	ns

Notes:

1. *There is no parameter 7.*
2. *Max frequency is 12.5 MHz, tested at up to 100 pF load.*
3. *Not included in production test.*

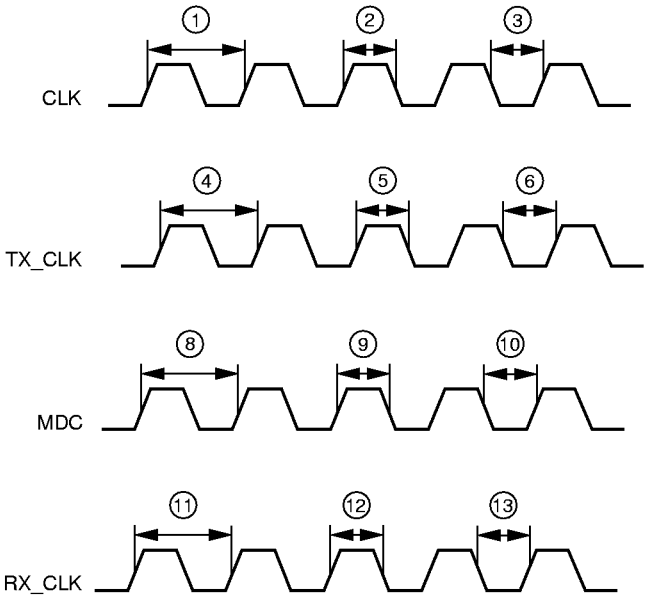


Figure 5. Clock Timing

Media Independent Interface

No.	Symbol	Parameter Description	Reference	Min	Max	Unit
		Transmit Timing				
21	t_S	TXD[3:0], TX_EN[3:0], TX_ER[3:0] setup time to TX_CLK or CLK ↑ edge (Note 1)		12		ns
22	t_H	TXD[3:0], TX_EN[3:0], TX_ER[3:0] hold time from TX_CLK or CLK ↑ edge (Note 1)		2.5		ns
35	t_{PD}	Transmit latency	1st TX_CLK after TX_EN ↑	80	90	ns
		MDC/MDIO Timing				
25	t_{PD}	MDIO output delay from MDC ↑ edge		10	40	ns
26	t_S	MDIO input setup time to MDC ↑ edge		8		ns
27	t_H	MDIO input hold time from MDC ↑ edge		8		ns
28	t_Z	MDC to high impedance			40	ns
36	t_S	$\overline{CS}$ input setup time to MDC ↑ edge		8		ns
37	t_H	$\overline{CS}$ input hold time from MDC ↑ edge		8		ns
		COL/CRS Timing				
29	t_{PD}	COL Assert latency	1st bit of /J/	100	150	ns
30	t_{PD}	COL De-assert latency	1st bit of /T/	140	190	ns
31	t_{PD}	CRS Assert latency	1st bit of /J/	80	130	ns
32	t_{PD}	CRS De-assert latency	1st bit of /T/	120	170	ns
33	t_{PD}	CRS Assert latency from TX_EN sampled high			40	ns
34	t_{PD}	CRS De-assert latency from TX_EN sampled low			40	ns
		Receive Timing				
38a	t_D	ENRCV delay from CRS asserted (Note 3)			20	ns
39a	t_{PD}	Receive Latency (to RXD, RX_DV, RX_ER Valid)	1st bit of /J/	140	180	
38b	t_{PD}	ENRCV delay from CRS asserted (Note 3)		40	100	ns
39b	t_{PD}	Receive Latency (to RXD, RX_DV, RX_ER Valid) (Note 4)	1st bit of data	140	180	ns
23	t_{PD}	RXD[3:0], RX_DV, RX_ER[3:0], FLS_CRS[3:0] setup time to RX_CLK ↑ edge (Note 2)		14		ns
24	t_H	RXD[3:0], RX_DV, RX_ER[3:0], FLS_CRS[3:0] hold time after RX_CLK ↑ edge (Note 2)		14		ns
40	t_{DZ}	ENRCV[3:0] low to RX_CLK, RX_DV, RX_ER, RXD high-impedance			20	ns
41	t_{PD}	RX_DV, RX_ER De-assert latency from start of ESD	1st bit of /T/	140	180	ns

Notes:

1. *Whether TX_CLK or CLK is used as the reference depends on the status of the CLK_SEL at rising edge of the $\overline{RESET}$.*
2. *In Shared MII mode, parameter 23 and 24 for each FLS_CRS signal are tested with the ENRCV of the corresponding port being asserted at all times.*
3. *The functionality of the device with respect to the ENRCV signal has been modified on the QFEXr+. If ENRCV is not generated within 20 ns of CRS (T38A), then RX_DV is suppressed for two cycles (to the end of the JK). As long as ENRCV arrives within 40 ns to 100 ns from CRS, the remainder of the transfer will take place as normal. This will not hamper the FLS_CRS condition since RXD/RX_ER pins carry the FLS_CRS information for four clock cycles, including the JK pair.*
4. *If ENRCV arrives within 40 ns to 100 ns from CRS, the /J/K/ pair will not be detected, but the remainder of the transfer, starting from the first bit of data, will be processed.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

SWITCHING WAVEFORMS

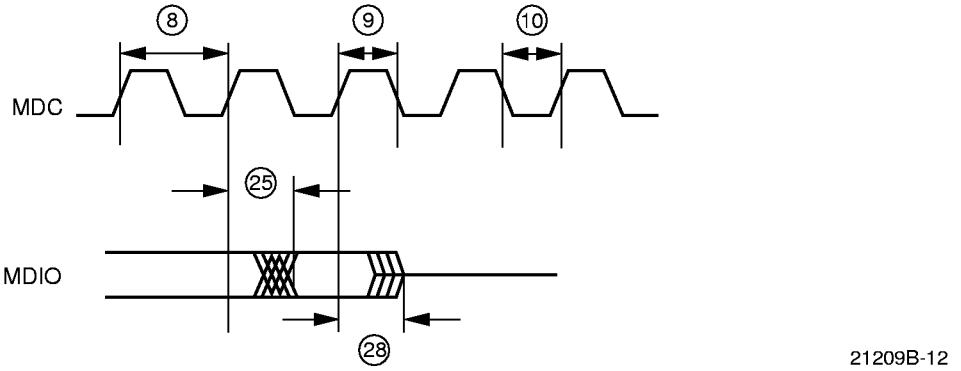


Figure 6. MII Management Port Read Timing

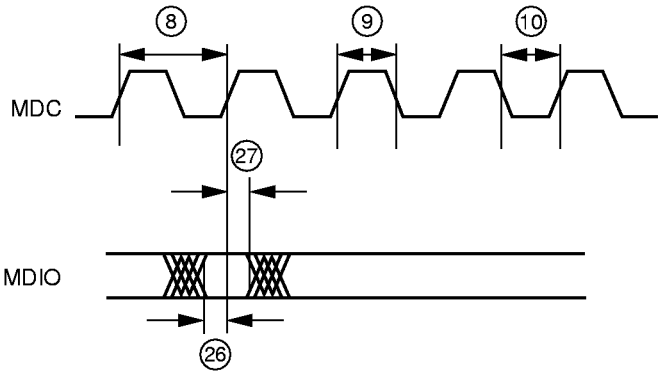


Figure 7. MII Management Port Write Timing

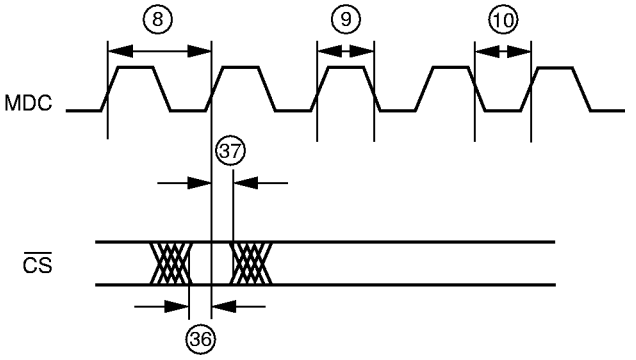


Figure 8. MII Management Address Assignment Timing

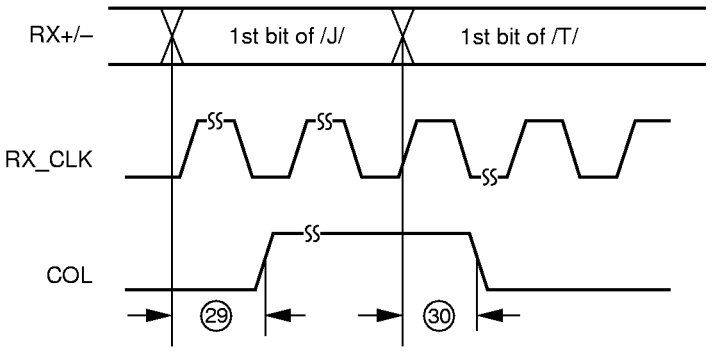


Figure 9. MII Collision Timing

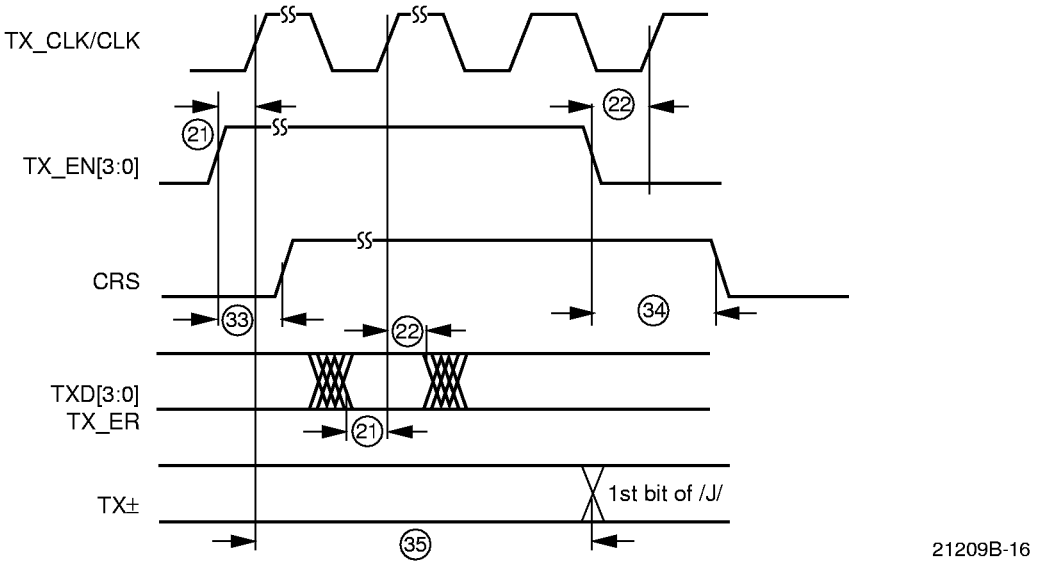
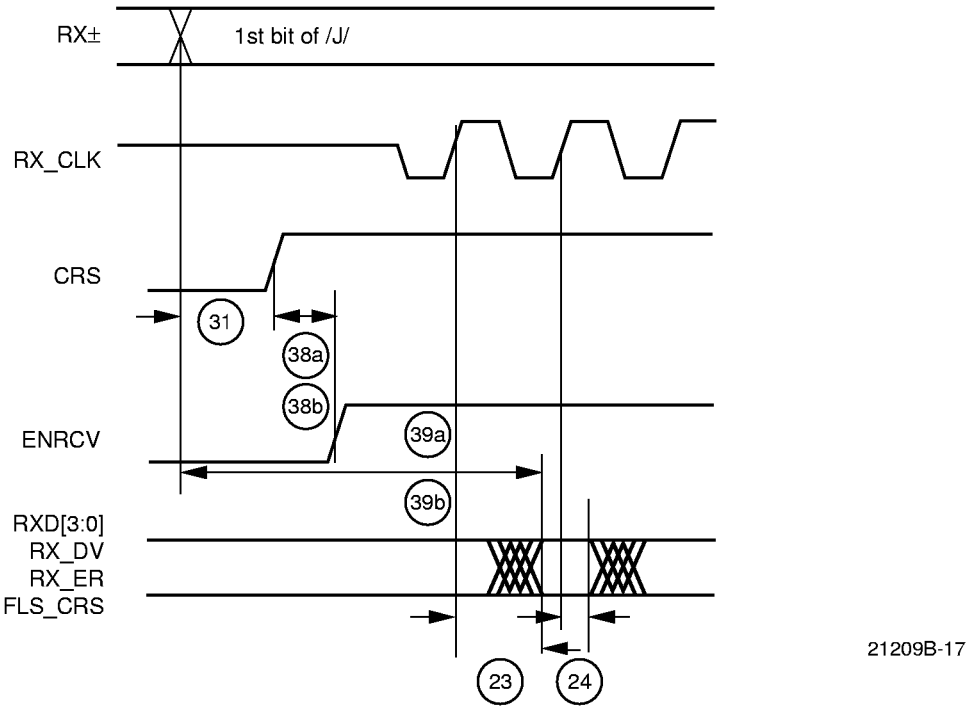


Figure 10. MII Carrier Sense Transmit Timing



Note:
Refer to Media Independent Interface Switching Characteristics to determine whether to use t38a/t39a or t38b/t39b.

Figure 11. Receive Start of Packet Timing

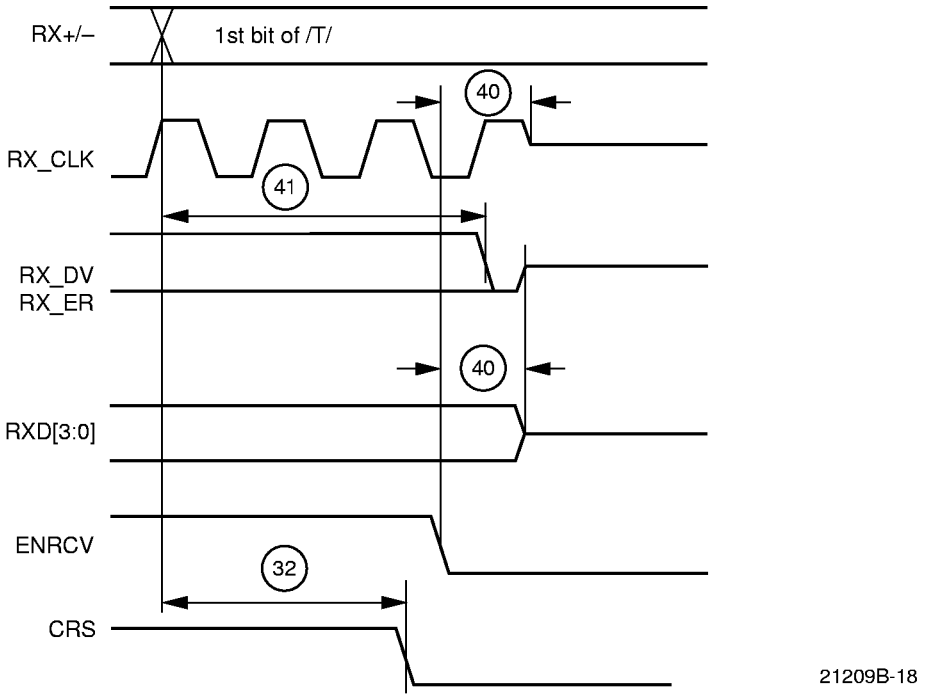


Figure 12. Receive End of Packet Timing

DEVICE CONFIGURATION INTERFACE

No.	Symbol	Parameter Description	Min	Max	Unit
60	t_{PWL}	$\overline{\text{RESET}}$ pulse width low	1.2		µs
61	t_S	DISSCR, CLK_SEL, ADDR[4:2] input setup time to $\overline{\text{RESET}}$ ↑ edge	10		ns
62	t_H	DISSCR, CLK_SEL, ADDR[4:2] input hold time from $\overline{\text{RESET}}$ ↑ edge	5		ns

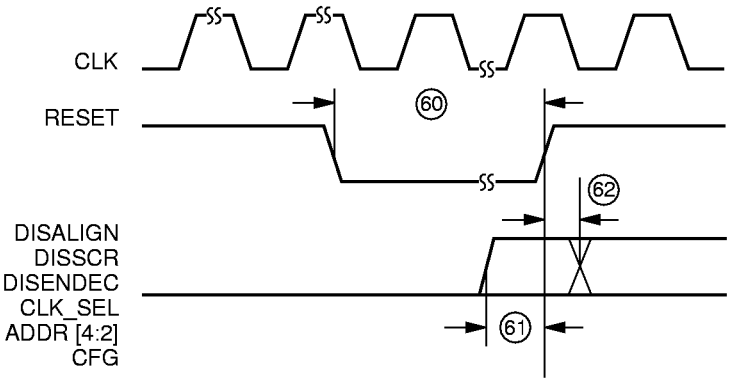


Figure 13. Device Configuration Timing

TEST INTERFACE

No.	Symbol	Parameter Description	Min	Max	Unit
100	t_{PER}	TCK Period	80	1000	ns
101	t_{PWH}	TCK Pulse width high	45%	55%	
102	t_{PWL}	TCK Pulse width low	45%	55%	
103	t_S	TDI, TMS setup time to TCK high	25		ns
104	t_H	TDI, TMS hold time from TCK high	6		ns
105	t_{INV}	TDO invalid from TCK low	0		ns
106	t_{PD}	TDO valid from TCK low		30	ns

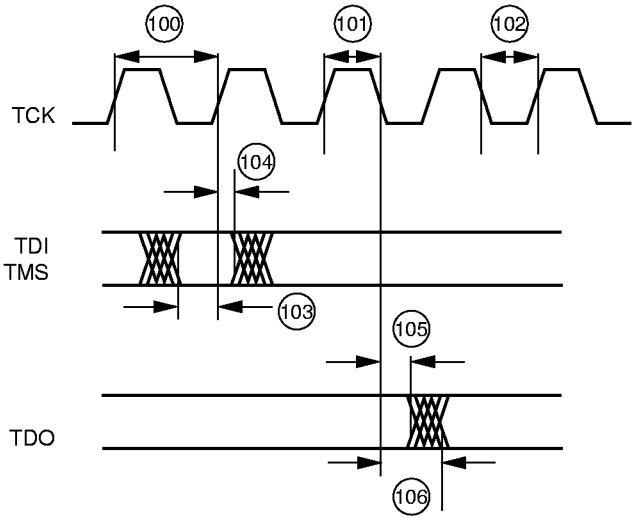


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Figure 14. TEST Interface Timing

PMD INTERFACE

No.	Symbol	Parameter Description	Test Conditions	Min	Max	Unit
150	t_R*	TX+, TX- Rise Time	PECL Load	0.3	3	ns
151	t_F*	TX+, TX- Fall Time	PECL Load	0.3	3	ns
152	t_{SK}*	TX+ to TX- skew	PECL Load		±200	ps
153	t_S	SDI setup time to CLK high		7		ns
154	t_H	SDI hold time from CLK high		5		ns

Note:
** - Not included in the production test.*

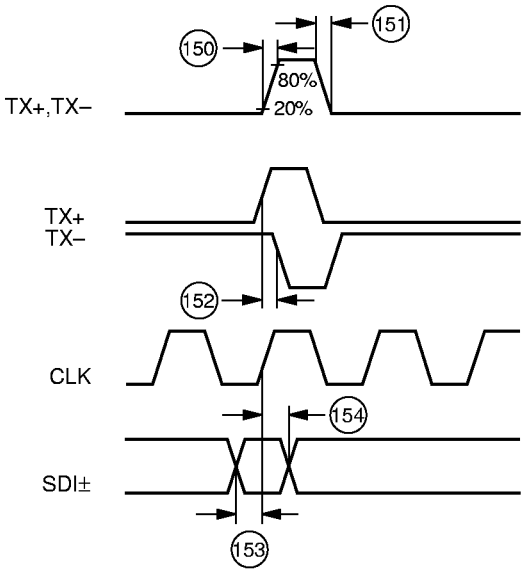


Figure 15. PMD Interface Timing

5-BIT SYMBOL INTERFACE

No.	Symbol	Parameter Description	Min	Max	Unit
155	t_S	SYMBOL_IN[4:0] setup time to TX_CLK/CLK ↑ edge	12		ns
156	t_H	SYMBOL_IN[4:0] hold time from TX_CLK/CLK ↑ edge	2.5		ns
157	t_{PD}	SYMBOL_OUT[4:0] valid to RX_CLK ↑ edge	14		ns
158	t_{PD}	SYMBOL_OUT[4:0] hold time to RX_CLK ↑ edge	14		ns

Note:
Symbol interface signals are mapped to the MII signals for each port when the 4B/5B encoder/decoder or data alignment is disabled (refer to pin description for DISENDEC and DISALIGN).

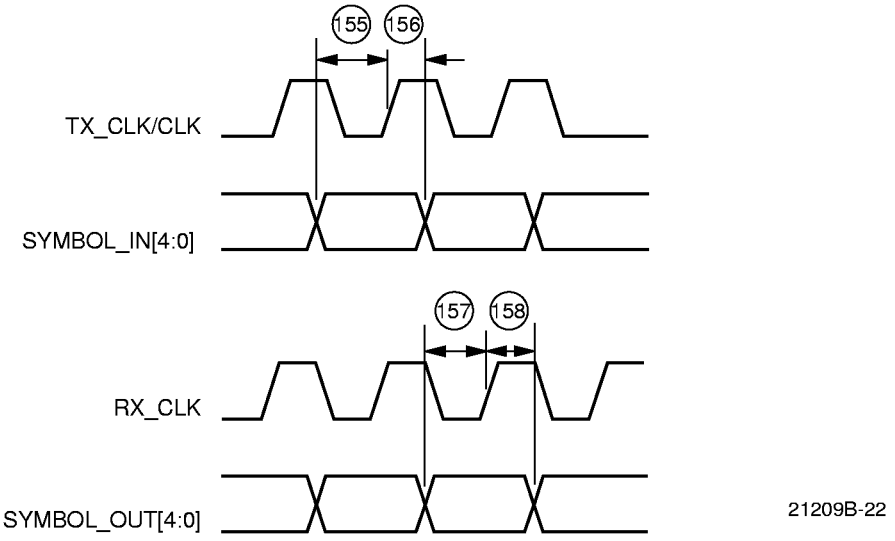
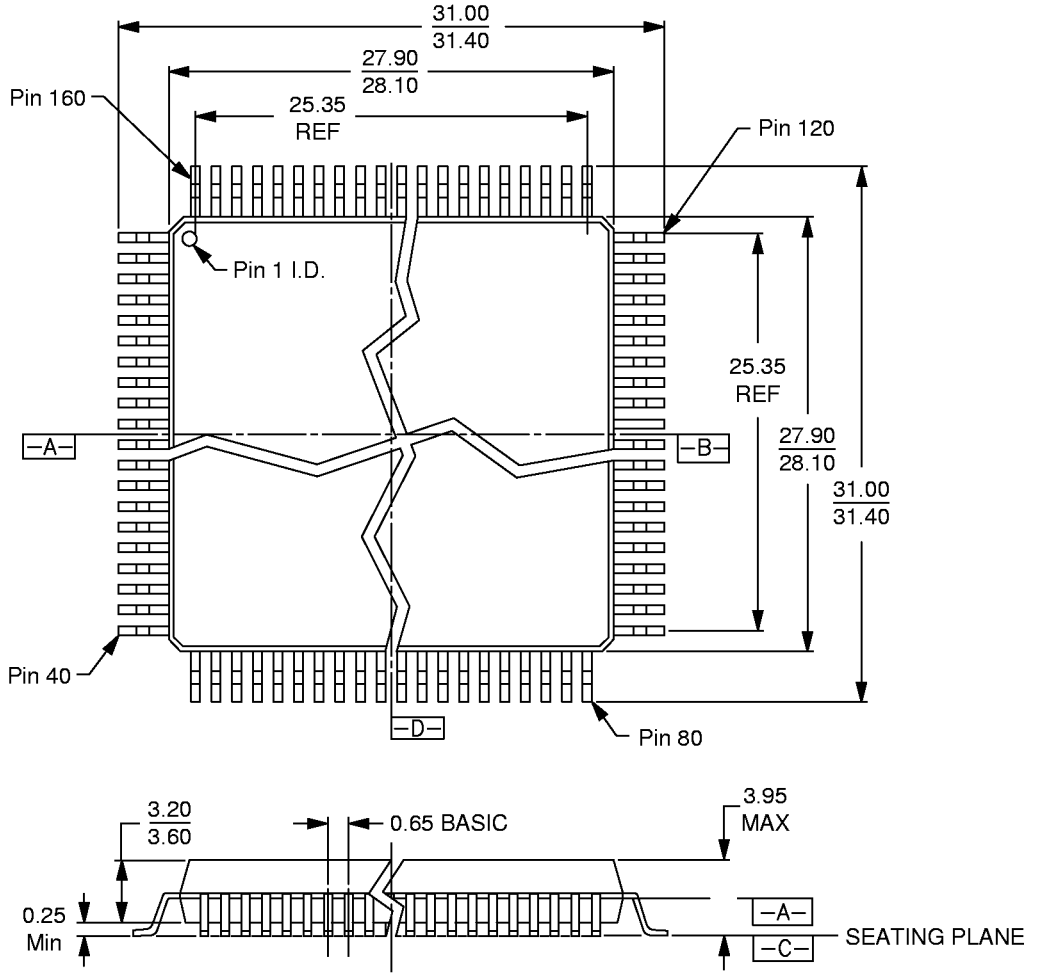


Figure 16. 5-bit Symbol Timing

PHYSICAL DIMENSIONS

PQR160

Plastic Quad Flat Pack (measured in millimeters)



16-038-PQR-1
PQR160
12-22-95 lv

ERRATA

Internal Loopback Path

The 4B/5B Loopback path (4B/5B encoder output to the 5B/4B decoder input) does not meet setup and hold times. Contact AMD for further details.

Symbol Mode

The QFEX+ device uses the falling edge instead of the rising edge of CLK/TX_CLK to latch TXD and RXD into the device. t155, t156, t157, and t158 remain the same, but are measured from the falling edge of CLK/TX_CLK and RX_CLK. This has the effect of not latching in data at the appropriate time for both transmitter and receiver. Contact AMD for further details and workaround solutions.