Features

- Fast Read Access Time - 150 ns
- Fast Byte Write - 200 µs or 1 ms
- Self-Timed Byte Write Cycle
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- Direct Microprocessor Control
  - DATA POLLING
- Low Power
  - 30 mA Active Current
  - 100 µa CMOS Standby Current
- High Reliability
  - Endurance: 10^4 or 10^5 cycles
  - Data Retention: 10 years
- 5 V ± 10% Supply
- CMOS & TTL Compatible Inputs and Outputs
- JEDEC Approved Byte Wide Pinout
- Full Military, Commercial, and Industrial Temperature Ranges

Note: Use AT28C16 For New Designs

2

4K (512 x 8) CMOS E^2PROM

Description

The AT28C04 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C04 is a 4K memory organized as 512 words x 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

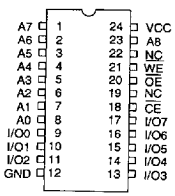
The AT28C04 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The end of a write cycle can be determined by $\overline{\text{DATA}}$ polling of I/O_7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100 µA. Atmel's 28C04 has additional features to ensure high quality and manufacturability, including internal error correction for extended endurance and for improved data retention characteristics.

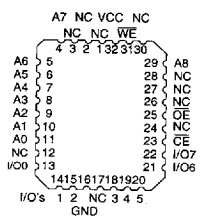
Pin Configurations

Pin Name	Function
A0 - A8	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect

PDIP Top View

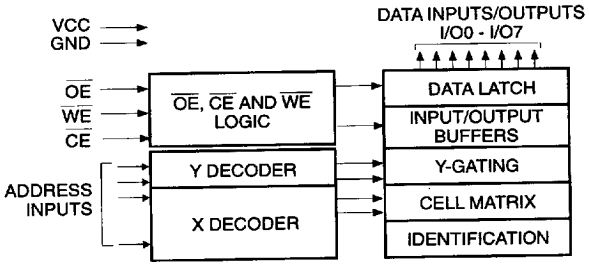


PLCC Top View



Note: PLCC package pins 1 and 17 are DON'T CONNECT.

Block Diagram



Absolute Maximum Ratings*

Temperature Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground	-0.6 V to Vcc +0.6 V
Voltage on $\overline{OE}$ with Respect to Ground	-0.6 V to +13.5 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Device Operation

READ: The AT28C04 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers increased flexibility in preventing bus contention.

BYTE WRITE: Writing data into the AT28C04 is similar to writing into a Static RAM. A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{OE}$ high and $\overline{CE}$ or $\overline{WE}$ low (respectively) initiates a byte write. The address location is latched on the last falling edge of $\overline{WE}$ (or $\overline{CE}$); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

FAST BYTE WRITE: The AT28C04E offers a byte write time of 200 µs maximum. This feature allows the entire device to be rewritten in 0.1 seconds.

$\overline{DATA}$ POLLING: The AT28C04 provides $\overline{DATA}$ POLLING to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O_7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

WRITE PROTECTION: Inadvertent writes to the device are protected against in the following ways. (a) Vcc sense— if Vcc is below 3.8 V (typical) the write function is inhibited. (b) Vcc power on delay— once Vcc has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high inhibits byte write cycles.

CHIP CLEAR: The contents of the entire memory of the AT28C04 may be set to the high state by the CHIP CLEAR operation. By setting $\overline{CE}$ low and $\overline{OE}$ to 12 volts, the chip is cleared when a 10 msec low pulse is applied to $\overline{WE}$.

D.C. and A.C. Operating Range

		AT28C04-15	AT28C04-20	AT28C04-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5 V ± 10%	5 V ± 10%	5 V±10%

Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H [3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to A.C. Programming Waveforms.
3. $V_H = 12.0\ V \pm 0.5\ V$.

D.C. Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	$V_{IN} = 0\ V$ to $V_{CC} + 1\ V$			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$=0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current CMOS	$\overline{CE} = V_{CC}$-0.3 V to $V_{CC} + 1.0\ V$			100	µA
I_{SB2}	V_{CC} Standby Current TTL	$\overline{CE} = 2.0\ V$ to $V_{CC} + 1.0\ V$	Com.		2	mA
			Ind., Mil.		3	mA
I_{CC}	V_{CC} Active Current A.C.	f = 5 MHz; I_{OUT} = 0 mA $\overline{CE} = V_{IL}$	Com.		30	mA
			Ind., Mil.		45	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1\ mA$			.4	V
V_{OH}	Output High Voltage	$I_{OH} = -400\ µA$		2.4		V

Pin Capacitance (f = 1 MHz, T = 25°C) [1]

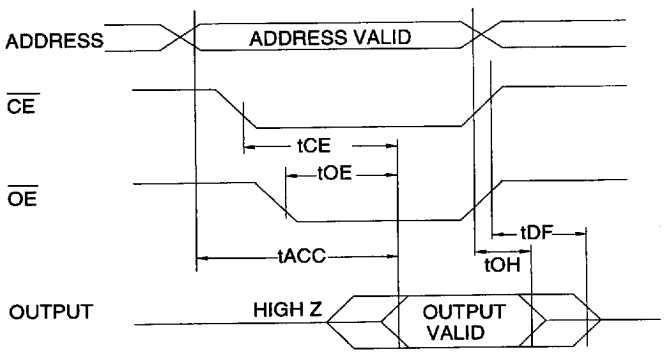
	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	$V_{IN} = 0\ V$
C_{OUT}	8	12	pF	$V_{OUT} = 0\ V$

Note: 1. This parameter is characterized and is not 100% tested.

A.C. Read Characteristics

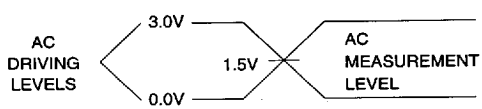
Symbol	Parameter	AT28C04-15		AT28C04-20		AT28C04-25		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		150		200		250	ns
t_{CE} (1)	$\overline{CE}$ to Output Delay		150		200		250	ns
t_{OE} (2)	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
t_{DF} (3,4)	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

A.C. Read Waveforms(1,2,3,4)



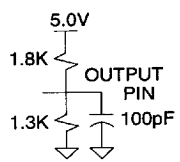
Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

Input Test Waveforms and Measurement Level



t_R, t_F < 20 ns

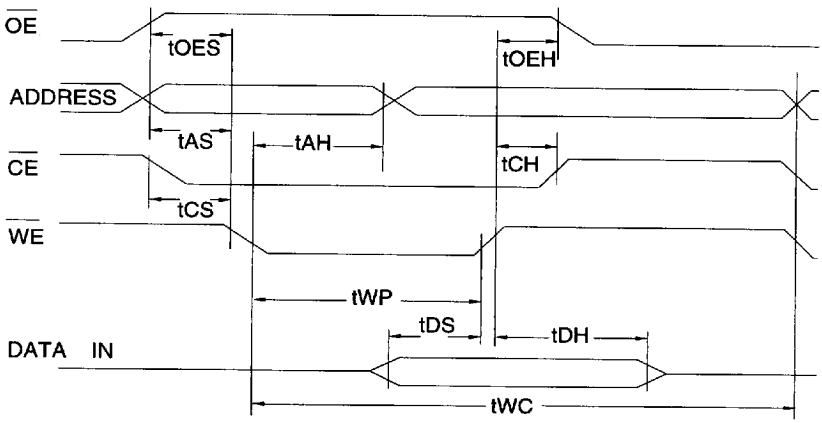
Output Test Load



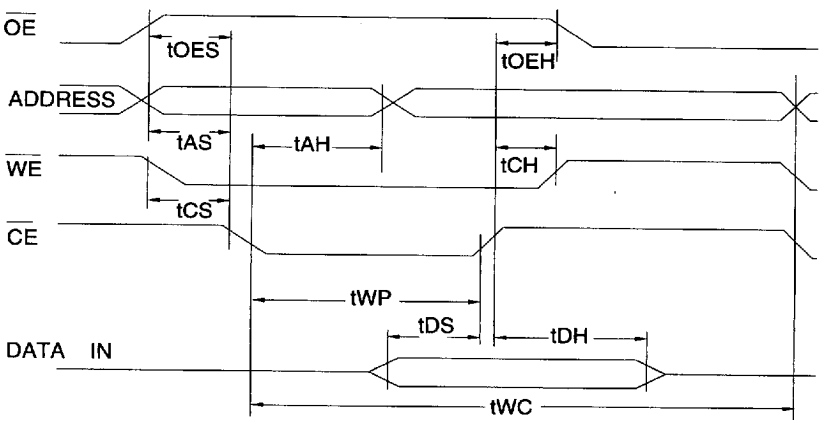
A.C. Write Characteristics

Symbol	Parameter		Min	Typ	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Set-up Time		10			ns
t_{AH}	Address Hold Time		50			ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)		100		1000	ns
t_{DS}	Data Set-up Time		50			ns
t_{DH},t_{OEH}	Data, $\overline{OE}$ Hold Time		10			ns
t_{CS},t_{CH}	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time		0			ns
t_{WC}	Write Cycle Time	AT28C04		0.5	1.0	ms
		AT28C04E		100	200	µs

A.C. Write Waveforms- $\overline{WE}$ Controlled



A.C. Write Waveforms- $\overline{CE}$ Controlled

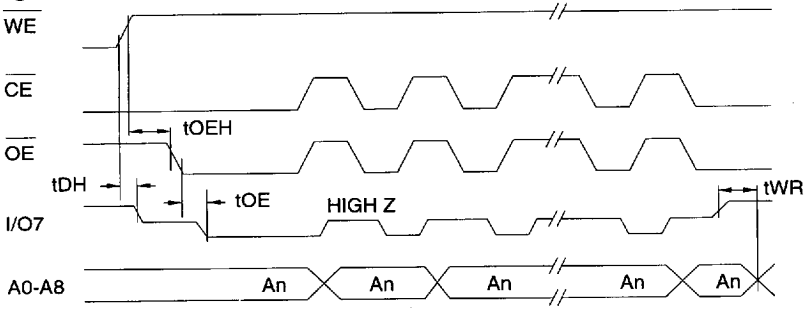


$\overline{\text{Data}}$ Polling Characteristics[1]

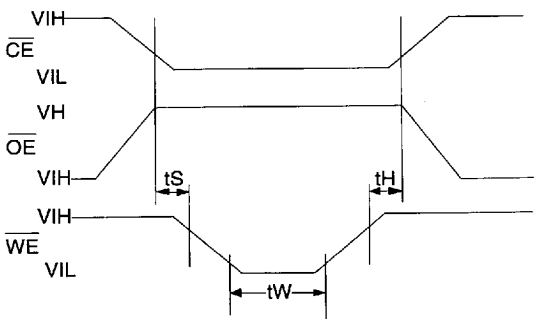
Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See A.C. Read Characterisitics.

$\overline{\text{Data}}$ Polling Waveforms

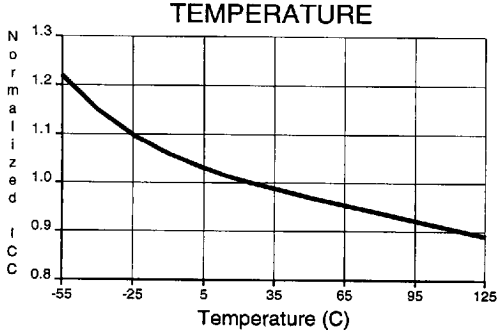


Chip Erase Waveforms

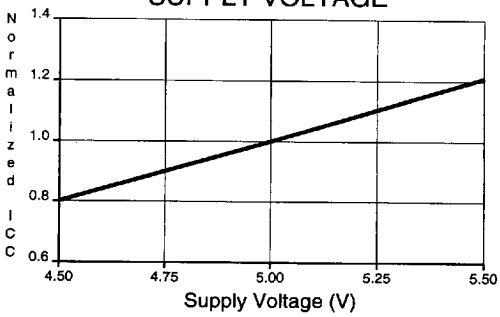


$t_S = t_H = 1\ \mu sec$ (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0\ V \pm 0.5\ V$

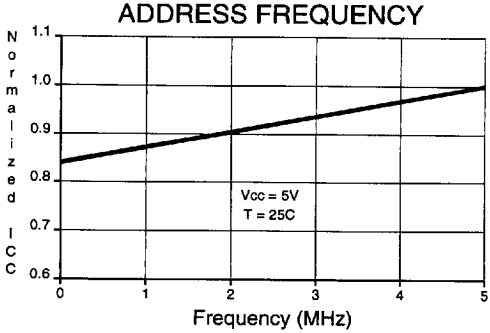
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



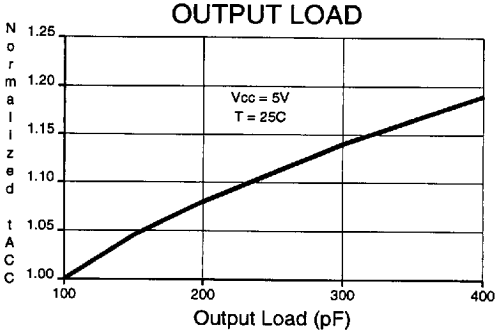
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



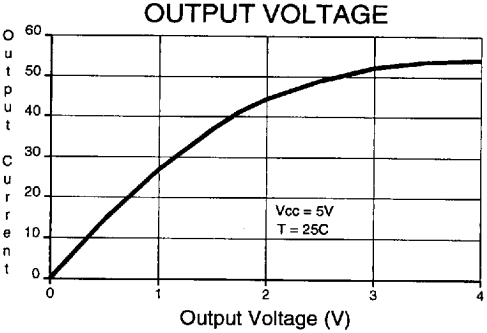
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



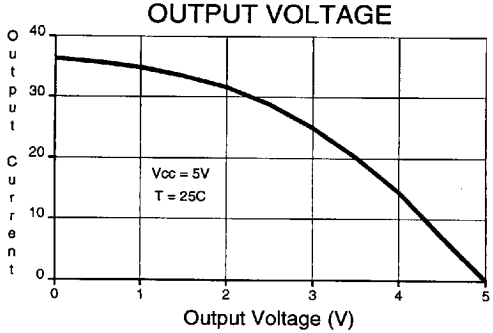
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C04(E)-15JC AT28C04(E)-15PC	32J 24P6	Commercial (0°C to 70°C)
150	45	0.1	AT28C04(E)-15JI AT28C04(E)-15PI	32J 24P6	Industrial (-40°C to 85°C)
200	30	0.1	AT28C04(E)-20JC AT28C04(E)-20PC	32J 24P6	Commercial (0°C to 70°C)
200	45	0.1	AT28C04(E)-20JI AT28C04(E)-20PI	32J 24P6	Industrial (-40°C to 85°C)
250	30	0.1	AT28C04(E)-25JC AT28C04(E)-25PC	32J 24P6	Commercial (0°C to 70°C)
250	45	0.1	AT28C04(E)-25JI AT28C04(E)-25PI	32J 24P6	Industrial (-40°C to 85°C)

Note: 1. See valid Part Number table below.

Valid Part Numbers

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C04	15	JC, JI, PC, PI
AT28C04E	15	JC, JI, PC, PI
AT28C04	20	JC, JI, PC, PI
AT28C04E	20	JC, JI, PC, PI
AT28C04	25	JC, JI, PC, PI
AT28C04E	25	JC, JI, PC, PI

Package Type	
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
24P6	24 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 µs