CA404/CA406

SUPERHETERODYNE FM RECEIVER CHIP SET

- **Low voltage (1.1 volt) operation for single battery cell applications**
- **Low power consumption**
- **On/Off gated operation for strobed (scanned) receiver applications**
- **High sensitivity; 0.5 microvolts for 12dB SINAD with appropriate external components**
- **Externally programmable low battery detect threshold**
- **Fast response when gated. Data outputs valid within 2 ms of gating on**
- **Balanced noise squelch circuit for strobed applications. Squelch output valid within 15 ms of gating on**
- **Separate enables for speech path and audio power amplifier, for flexibility. Can select speech or tone output**
- **Auxiliary open-collector driver with MOS compatible input. Can drive LED, for example**
- **Optional supply regulator for high voltage applications**

The CA404 and CA406 integrated circuits form the basis of a low power, high sensitivity FM radio receiver for speech and data. The chip set will operate at battery voltages as low as 1.1 volts. It is therefore particularly suitable for single battery cell applications where low power and minimum size are required.

The chip set was designed primarily for use in double conversion superheterodyne receivers with the CA404 mixer converting from a 21.4 MHz first IF to a 455 KHz second IF. However, an auxiliary RF amplifier stage on the CA404 allows it to operate as the front end of a single conversion HF receiver, operating up to 50MHz.

The system was configured as a two chip set rather than a single chip to optimize performance and flexibility. Separating the relatively high power output stage from the sensitive input stage makes the system less sensitive to on and off chip parasitics. Also, both performance and flexibility considerations demand a relatively high pin count, most cost effectively achieved with two chips.

Applications include use in pocket pagers, mobile radio, mobile data terminals, cordless telephones, and medical monitoring and alert systems.

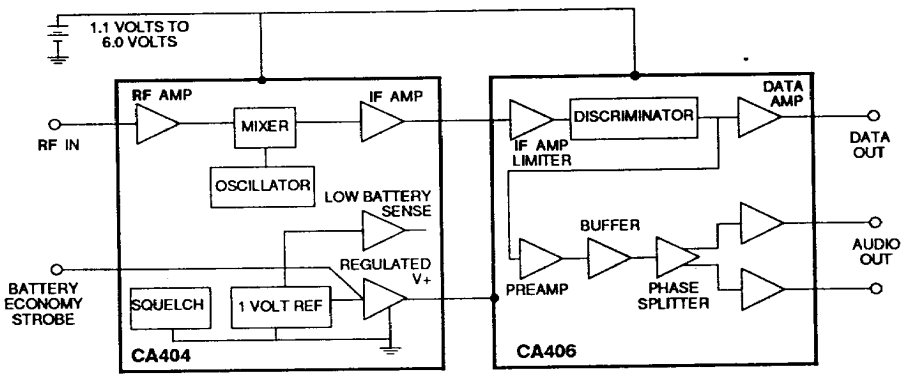

Figure 1 : CA404/CA406 CHIP SET BLOCK DIAGRAM

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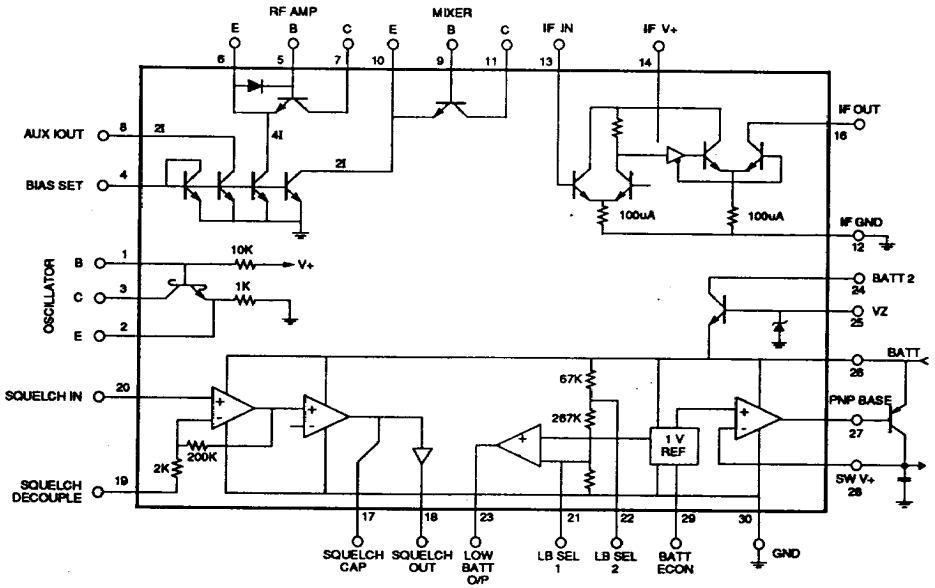


Figure 2 : CA404 BLOCK DIAGRAM

Note: Pin numbers correspond to 30 – lead Vinson Quill package

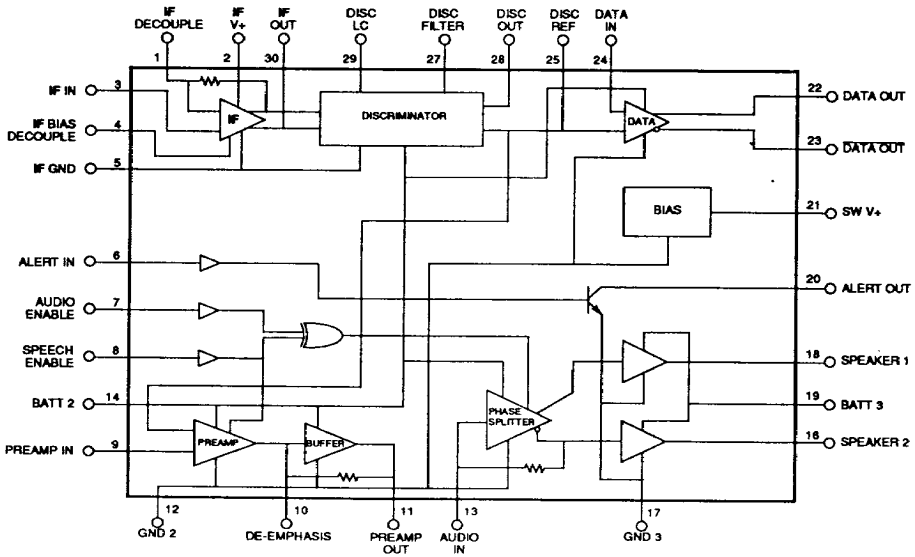


Figure 3 : CA406 BLOCK DIAGRAM

PIN CONFIGURATION DIAGRAMS

1	OSC B	15	IF OUT
2	OSC E	16	SQUELCH CAP
3	OSC C	17	SQUELCH OUT
4	BIAS SET	18	SQUELCH DECOUPLE
5	RF AMP B	19	SQUELCH IN
6	RF AMP E	20	LB SEL 1
7	RF AMP C	21	LB SEL 2
8	AUX IOUT	22	LOW BATT OUT
9	MIXER B	23	VZ
10	MIXER E	24	BATT
11	MIXER C	25	PNP BASE
12	IF GND	26	SW V+
13	IF IN	27	BATT ECON
14	IF V+	28	GND

a) CA404 L – 28

1	IF DECOUPLE	15	SPEAKER 2
2	IF V+	16	GND 3
3	IF IN	17	SPEAKER 1
4	IF BIAS DECOUPLE	18	BATT 3
5	IF GND	19	ALERT OUT
6	ALERT IN	20	SW V+
7	AUDIO ENABLE	21	DATA OUT
8	SPEECH ENABLE	22	$\overline{\text{DATA OUT}}$
9	PREAMP IN	23	DATA IN
10	DE-EMPHASIS	24	DISCRIMINATOR REF
11	PREAMP OUT	25	DISCRIMINATOR FILTER
12	GND 2	26	DISCRIMINATOR OUT
13	AUDIO IN	27	DISCRIMINATOR LC
14	BATT 2	28	IF OUT

b) CA406 L – 28

1	OSC B	16	IF OUT
2	OSC E	17	SQUELCH CAP
3	OSC C	18	SQUELCH OUT
4	BIAS SET	19	SQUELCH DECOUPLE
5	RF AMP B	20	SQUELCH IN
6	RF AMP E	21	LB SEL 1
7	RF AMP C	22	LB SEL 2
8	AUX IOUT	23	LOW BATT OUT
9	MIXER B	24	BATT 2
10	MIXER E	25	VZ
11	MIXER C	26	BATT
12	IF GND	27	PNP BASE
13	IF IN	28	SW V+
14	IF V+	29	BATT ECON
15	N/C	30	GND

c) CA404 30 – LEAD VINSON QUILL
Quill package is available for samples only

1	IF DECOUPLE	16	SPEAKER 2
2	IF V+	17	GND 3
3	IF IN	18	SPEAKER 1
4	IF BIAS DECOUPLE	19	BATT 3
5	IF GND	20	ALERT OUT
6	ALERT IN	21	SW V+
7	AUDIO ENABLE	22	DATA OUT
8	SPEECH ENABLE	23	$\overline{\text{DATA OUT}}$
9	PREAMP IN	24	DATA IN
10	DE-EMPHASIS	25	DISCRIMINATOR REF
11	PREAMP OUT	26	N/C
12	GND 2	27	DISCRIMINATOR FILTER
13	AUDIO IN	28	DISCRIMINATOR OUT
14	BATT 2	29	DISCRIMINATOR LC
15	N/C	30	IF OUT

d) CA406 30 – LEAD VINSON QUILL
Quill package is available for samples only

Figure 4 : CA404 and CA406 PINOUT DIAGRAMS for DIFFERENT PACKAGE CONFIGURATIONS

Table 1 : CA404 ELECTRICAL CHARACTERISTICS (Battery = 1.5V, T_A = 20°C)

Parameter	Condition	Min	Typ	Max	Units
Supply Voltage (battery)		1.1		6	V
Supply Current	From battery; power down		6	15	µA
	From battery; power up		2.4	3.1	mA
IF PreAmp	R_{IN}	30			KΩ
	Voltage gain @ 455 KHz into 40KΩ tuned load		50		dB
	Equivalent input noise (Figure 8)		1.8		µV
Oscillator, Mixer and	HFE @ IC = 250µA, V_{CE} = 0.5V)	80		400	
Auxiliary RF Amplifier	rbb (RF Amplifier and Mixer)		50		Ω
transistors	rbb (Oscillator)		100		Ω
(NPN transistors with	ft @ 250 µA		150		MHz
B,E & C nodes access)	ft @ 500µA		250		MHz
	ft @ 1mA		450		MHz
	ft @ 5mA (peak ft)		1		GHz
SW V+ Voltage	(External PNP collector current 2mA max; Figure 8)	0.95	1.0	1.05	V
SW V+ Voltage Temperature Coefficient			–0.6		mV/°C
Current Source Bias	BIAS SET Voltage @ I = 100µA	650	700	750	mV
For current I into bias	Mixer bias and IOUT	1.6	2.0	2.4	x I
Set Pin	Auxiliary RF Bias	3.2	4.0	4.8	x I
BATT ECON	I_{IH}			–0.5	µA
(to be driven from an open collector type gate or FET)	V_{IL} @ I_{IL} = –50µA (to guarantee BATT ECON low, sink 50µA or ground pin through 2 KΩ max.)			0.1	V
LOW BATT Output	V_{OL} @ I_{OL} = 5µA			0.1	V
	High State Leakage Current (V_{OH} ≥ 6V)			2.0	µA
Switching Threshold	a) LB SEL 1 connected to LB SEL 2	1.05	1.1	1.15	V
of BATT Voltage	b) LB SEL 1 and LB SEL 2 open circuit	2.1	2.2	2.3	V
Squelch	SQUELCH OUT Transition: High-Low		2.8		mV/RMS
Switching Thresholds	SQUELCH OUT Transition: Low-High		1.4		mV/RMS
@ 20KHz (differential	SQUELCH OUT				
RMS volts pins 19-20)	V_{OH} @ I_{OH} = 5µA	BATT – 0.2			V
	V_{OL} @ I_{OL} = -5µA			0.2	V

Note : Collectors of current mirror transistors must be connected to a positive voltage to prevent the saturation of the current mirror transistors

Recommended operating temperature range is: –20 °C to +70 °C

Table 2 : CA406 ELECTRICAL CHARACTERISTICS (Battery = 1.5V, SW V+ = 1.0V, T_A = 20°C)

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (battery)		1.1		6	V
Supply Current	From battery, power down		0	10	µA
	From battery, power up				
	SW V+		0.06	0.1	mA
	BATT 1		0.28	0.38	mA
	BATT 2		0.66	0.97	mA
	BATT 3 AUDIO OUT, ALERT OUT *off*		0	10	µA
	AUDIO OUT *on*		8	20	mA
	ALERT OUT *on*		8	15	mA
IF Amplifier	Voltage Gain @ 455KHz (to internal A-B; Figure 8)		60		dB
	Input Impedance	100			KΩ
	Input Limiting Threshold (20dB limiting @ 455 KHz)		1.5		mVRMS
Discriminator	Recovered Audio (external phase shift network with C = 100 pF; Q = 30)		10		mV/KHz
	Filter Resistor R13	10	14	18	KΩ
Audio PreAmp and Buffer	Input Impedance	6	10	13	KΩ
	Gain (without de-emphasis)		20		
	Output Impedance			3	KΩ
	Buffer Feedback Resistor	70	100	130	KΩ
Data Amplifier	Input Bias Current			0.5	µA
	Offset Voltage			7	mV
	Voltage Gain (RL > 1 MΩ)	2000			
	Open Collector Outputs: V_{OL} @ I_{OL} = 5µA			0.1	V
	High State Leakage Current (V_{OH} ≤ 6V)			2	µA
Audio Output Amplifier	Gain into Center-Tapped 16 Ω load (Output volts at SPEAKER 1, SPEAKER 2 current into AUDIO IN)	0.1	0.2	0.4	V/µA
	Output Swing into C.T. 16 Ω load; BATT 3 = 1.3V; peak swing @ SPEAKER 1, SPEAKER 2	0.8			Vpk
	Total Harmonic Distortion (0.5V peak swing @ SPEAKER 1, SPEAKER 2)		3	7	%

Table continued on next page

Table 2 : CA406 ELECTRICAL CHARACTERISTICS CON'T

Parameter	Conditions	Min	Typ	Max	Units
Control Inputs: SPEECH ENABLE, AUDIO ENABLE and ALERT IN	V_{IH}	0.8			V
	V_{IL}			0.2	V
	I_{IH} @ V_I = 0.9V				
	SPEECH ENABLE, AUDIO ENABLE			5	µA
	ALERT IN	–10	–20		µA
	I_{IL} @ V_I = 0.1V				
	SPEECH ENABLE, AUDIO ENABLE			–20	µA
	ALERT IN		–25	–40	µA
ALERT OUT	OFF Leakage Current @ V_O = 6V			10	µA
	ON Voltage @ IL = 50mA			0.5	V

Note: Recommended operating temperature range is: –20° to +70°C

Table 3 : ABSOLUTE MAXIMUM RATINGS

CA404	
Input Voltage	6 V
Storage Temperature Range	–65° to +150°C
CA406	
Input Voltage	6 V
Storage Temperature Range	–65° to +150°C

Stresses beyond those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

FUNCTIONAL DESCRIPTION

Operation of the CA404/CA406 chip set will be described with particular reference to the single conversion superheterodyne receiver application shown in Figure 8.

Power Supply and Bias

The CA404 and CA406 each have multiple power supply pins and ground pins as follows:

CA404	
BATT	General battery connection
IF V+	V+ for IF Preamp only
SW V+	Regulated 1 V rail; switched up and down by BATT ECON input
BATT 2	Auxiliary battery pin for high voltage supply, if required
GND	General ground
IF GND	Ground for IF Preamp only
CA406	
BATT 2	General battery
BATT 3	Battery for AUDIO OUTPUT & ALERT OUTPUT stages
IF V+	V+ for IF Amplifier only
SW V+	From CA404; switched up and down for power up power down conditions
GND 2	General ground
GND 3	Ground for AUDIO OUTPUT & ALERT OUTPUT stages
IF GND	Ground for IF Amplifier and Discriminator only

The SW V+ rail provides a switchable, regulated 1.0 volt supply. It is designed to operate with an external PNP transistor and capacitor. The output voltage follows a modified bandgap voltage reference which is switchable from 0 to 1.0 volts by the Battery Economy (BATT ECON) input pin. The SW V+ rail is used to establish regulated and temperature compensated bias currents on both the CA404 and the CA406, and to switch both chips between Power Up and Power Down modes.

In Figure 8, decoupling of supplies is provided by networks R16-C22/C23, R11-C18/R19, R1-C1, and C8/C11. Small decoupling caps in parallel with large ones provide low series resistance and inductance.

An external resistor connected from the SW V+ to the Bias Set pins on the CA404 establishes the Mixer and RF Amplifier stage currents as well as the AUX IOUT current. These currents have a positive temperature coeffecient to provide temperature compensated stage gains. In a double superhet application it may be desirable to disregard the Aux RF Amp transistor, and use its bias current along with AUX IOUT to bias external first RF and first Mixer transistors. All three current sources (MIXER-E, RF-E, and AUX IOUT) must always be connected to a positive voltage to prevent saturation of the current mirror bias circuitry (see Figure 2).

Signal Path

With reference to Figure 8, the RF signal is coupled to the base of RF amplifier transistor Q1 through C2. R2 provides base current to Q1. C4 is a decoupling capacitor. Q1 works into load L1/C3/R3 tuned to 21.4MHz with a Q of 10.

The local oscillator is a Colpitts configuration around Q2 with a 20.945MHz crystal. The oscillator output is coupled to the base of mixer transistor Q3 through C7.

The emitter of Q3 is decoupled to ground through C10. The collector of Q3 is connected to tuned load L2/C9, so that the signal swing is about V+. R6 and R7 correctly terminate the 455KHz ceramic filter.

The IF Preamp on the CA404, properly terminated, has a voltage gain of 50dB. Network L3/C14/R9 is a mid-IF noise filter tuned to 455KHz with a Q of 10. C15 is a decoupling capacitor. The IF amplifier on the CA406 has a voltage gain of 60dB and complementary outputs.

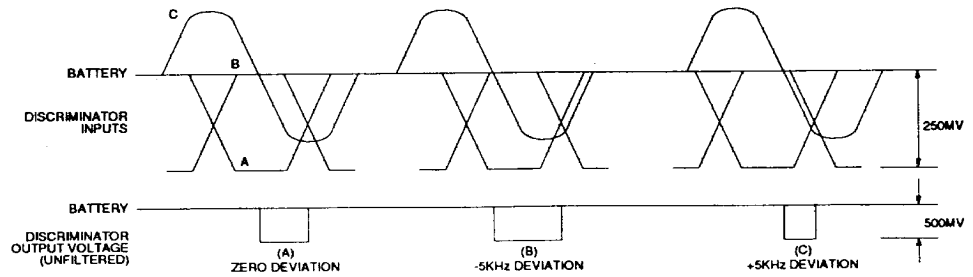


Figure 5 : DEMODULATION DIAGRAM (IF = 455KHz)

The discriminator has three inputs as shown in Figure 8 and the demodulation diagram of Figure 5. These are the complementary outputs of the IF plus the phase-shifted signal from the quadrature network C16/L4/C17/R10. The quadrature network is tuned to 455KHz (Q = 30). It shifts a 455KHz signal 90°. For a frequency deviation of ±5KHz, the shift change around 90° is ±35°.

The inputs to the discriminator are labelled A,B, and C in Figures 5 and 8. C leads B by 90° at 455KHz. The output of the discriminator is low only if B is higher than both A and C.

The unfiltered discriminator output is a 500mV amplitude pulse train with a duty cycle of 25% low at 455KHz. The duty cycle varies with the FM as shown in Figure 5. The recovered audio, obtained across filter capacitor C20, is (500mV)(35°/360°) / 5KHz ≈ 10mV/KHz. The filter cutoff frequency in Figure 8 is:

$$\text{FILTER CUTOFF} = \frac{1}{2\pi R_{13} C_{20}} = 5\text{KHz}$$

The demodulated signal appears at the emitter of buffer transistor Q10 for transmission to both the data and the audio channels. The cutoff frequency of data lowpass filter R12-C21 is selected for the data rate desired. The corner frequency in Hz should be approximately 0.6 times the data rate in bps, for example 300Hz for 512bps. The Data Amplifier has complementary outputs.

The demodulated signal is coupled to the Audio Preamp through C12. The cutoff frequency of the audio de-emphasis network is:

$$\text{AUDIO DE-EMPHASIS CUTOFF} = \frac{1}{2\pi R_{14} C_{13}} = 340\text{Hz}$$

R15 is the volume control resistor at the input to the phase splitter and audio output stage.

The audio output stage drives a 16Ω center-tapped load (speaker) with a 0-pk swing at either output of 0.8 volts minimum (battery voltage 1.3 volts). Distortion at that signal level is typically 3%. Output signal is determined by:

$$V_{OUT} = \left(\frac{V_{IN}}{R_{IN}}\right) Z$$

where V_{OUT} = Output voltage at either SPEAKER 1 or SPEAKER 2

V_{IN} = Voltage at Preamp Out

R_{IN} = External resistor R15

Z = Transimpedance gain of audio output stage, typically 200KΩ.

Other Features

The BATT 2 pin on the CA404 can be used for supply voltages greater than 8 volts. A resistor from BATT 2 to VZ is required. The BATT rail is regulated at about 6 volts.

The Low Battery Detector circuitry on the CA404 senses the battery voltage and compares it to the 1.0 volt reference. Pins LB SEL 1 and LB SEL 2 allow selection of the low battery detect level. With both pins open, the low battery detect level is 2.2 volts nominal for a 2-cell battery, and with the select pins shorted together, the detect level becomes 1.1 volts nominal for a 1-cell battery. Other threshold levels can be obtained by connecting an external resistor between select pins, or from a select pin to battery or ground. However, care must be taken to accommodate a ±30% tolerance on internal resistors, and a trim may be required. The LOW BATT output is open collector.

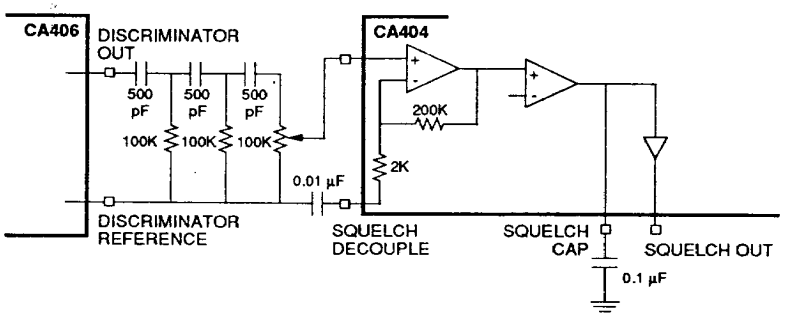


Figure 6 : CA404 NOISE SQUELCH CIRCUIT

Appropriate input levels on the SPEECH ENABLE and AUDIO ENABLE inputs allow selection of speech or tone output. The desired tone is input on the AUDIO IN pin either directly or through h the volume control resistor R15.

The Alert Channel has a MOS-compatible input (ALERT IN) and an open collector output (ALERT OUT). The output can be used to drive a LED.

Squelch

The squelch external circuit connection is given in Figure 6. In operation, the presence or absence of carrier is determined by detecting the noise above the audio range that is present when the carrier is low or absent.

The output from the discriminator on the CA406 is highpass filtered at about 3KHz and fed to the squelch detect circuitry on the CA404. The SQUELCH OUT pin has a high-to-low transition for a 2.8mV RMS 20KHz signal at the squelch inputs to the CA404, and a low-to-high transition for a 1.4mV RMS signal. The circuit threshold is adjustable by either the potentiometer shown in Figure 6, or by an external resistor in series with the SQUELCH DECOUPLE pin and the internal 2K resistor.

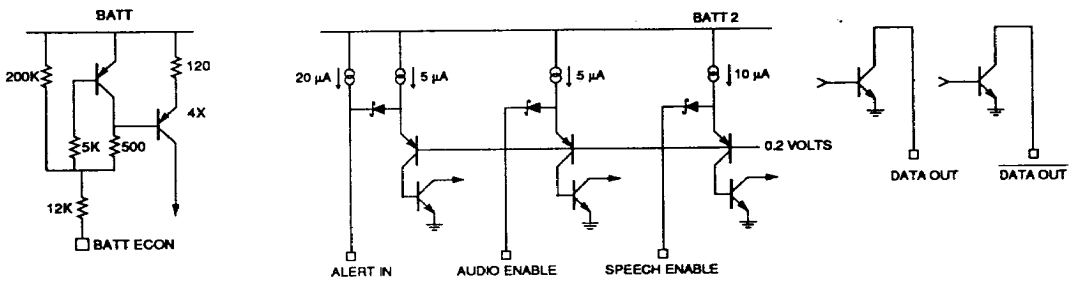
The squelch detect circuitry is balanced in order to respond quickly in a strobed receiver application. The Squelch output level is valid within 15ms of the chip being gated ON.

Table 4 : CA404 FUNCTION TABLE

BATT ECON input	0	Chip Set Power Up
	1	Chip Set Power Down
LOW BATT output	0	Battery Low
	1	Battery Okay

Table 5 : CA406 FUNCTION TABLE

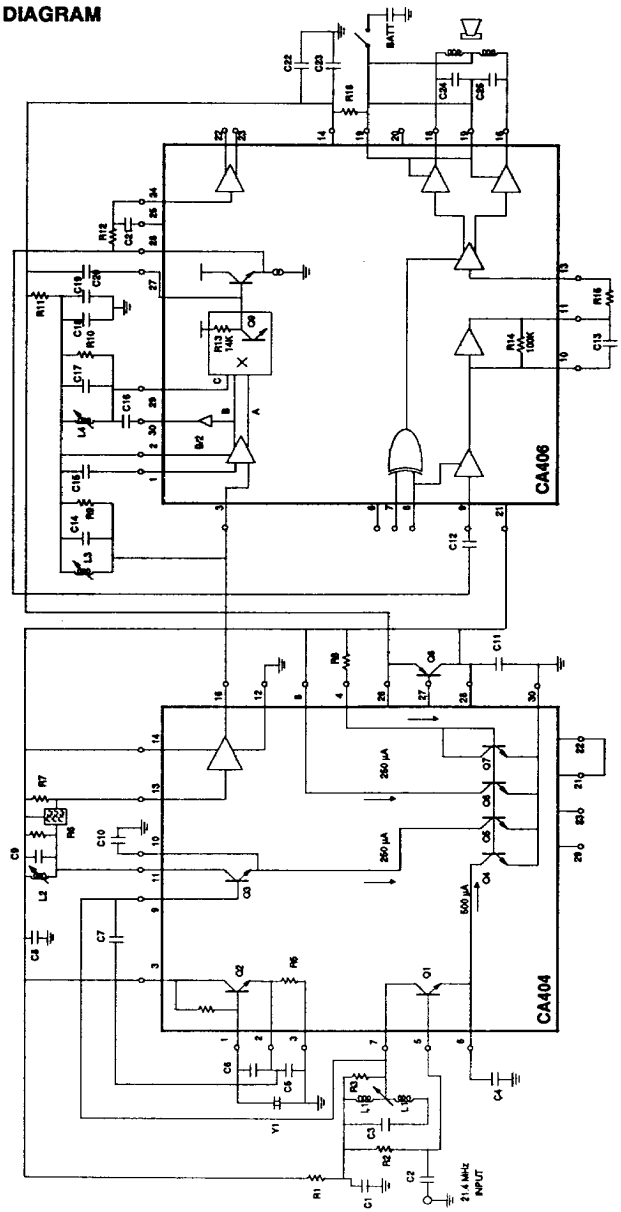
AUDIO ENABLE	SPEECH ENABLE	ALERT IN	AUDIO PREAMP	AUDIO OUT	ALERT OUT
0	0		OFF	OFF	
1	0		OFF	ON	
0	1		ON	ON	
1	1		ON	OFF	
		0			OFF
		1			ON



a) CA404 b) CA406

Figure 7 : CA404/CA406 INTERFACE SCHEMATICS

APPLICATION DIAGRAM



Note: Pin numbers correspond to 30 – lead Vinson Quill package

Figure 8 : CA404/CA406 21.4 MHz RECEIVER and TEST CIRCUIT

Table 6 : APPLICATION PARTS LIST (per Figure 8)

#	Value	#	Value	#	Value	#	Value
R1	100Ω	R14	100K (on-chip)	C10	0.1µF	C23	0.1µF
R2	10K	R15	24K	C11	4.7µF	C24	0.1µF
R3	510Ω	R16	20Ω	C12	0.1µF	C25	0.1µF
R4	10K (on-chip)			C13	0.0047µF		
R5	1K (on-chip)	C1	0.1 µF	C14	100pF	L1	5.5µH, turns ratio tapped 1:4 as shown
R6	1.5K	C2	0.001µF	C15	0.0068µF		
R7	1.5K	C3	10pF	C16	10pF	L2	1.22mH
R8	2.2K	C4	0.01µF	C17	100pF	L3	1.22mH
R9	to give Q = 10	C5	82pF	C18	4.7µF	L4	1.22mH
R10	to give Q = 30	C6	39pF	C19	0.01µF	Y1	20.945 MHz Crystal
R11	51Ω	C7	2pF	C20	0.0022µF	F1	Ceramic Filter Murata CFW 455 or equiv.
R12	10K	C8	0.1µF	C21	0.022µF		
R13	14K (on-chip)	C9	100pF	C22	50µF	Q8	2N3906 or equiv.

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