PCI Clock Generator with Buffers

Features

- Generates preset CPU and PCI frequencies, 1 peripheral clock, and buffers the input reference frequency
- 5 CPU output buffers and one Early CPU buffer
- Supports both synchronous and asynchronous PCI clocks with up to 8 PCI output buffers
- Low skew output buffers
- Additional general purpose buffers
- Power down, slow down, or stop clock feature supporting "Green PC" applications
- External loop filter provides exceptionally smooth, glitch-free frequency transitions
- Low, short-term and long-term jitter
- Supports Pentium™ and all x86-based designs
- Supports ISA, VESA, and PCI-based designs
- CMOS technology in 32-pin SOIC
- 5V or 3.3V supply

Description

CH9088 is a triple PLL clock generator designed for high performance computer motherboards. CH9088 buffers the 14.318 MHz reference frequency into two outputs, generates multiple CPU and PCI clocks from a preset ROM table, and provides a 24 MHz peripheral clock.

The CPU output frequencies are selected by the frequency select inputs, FS[1:0]. An Early CPU output is available and typically precedes the CPU outputs by 2 to 5 ns.

Both synchronous and asynchronous PCI clocks are supported using the PSYNC* select pin. When PSYNC* is high, the PCI clocks are at 33.3 MHz. Otherwise, the PCI clock outputs are synchronous with the CPU clock and runs at half the CPU clock. In addition, CH9088 has built in on-chip buffers to provide the necessary buffering required for PCI or VESA applications.

CH9088 is available with power down (PD*), slow down (SD*), or stop clock (CPUEN) options, which are ideal for low power "Green PC" applications.

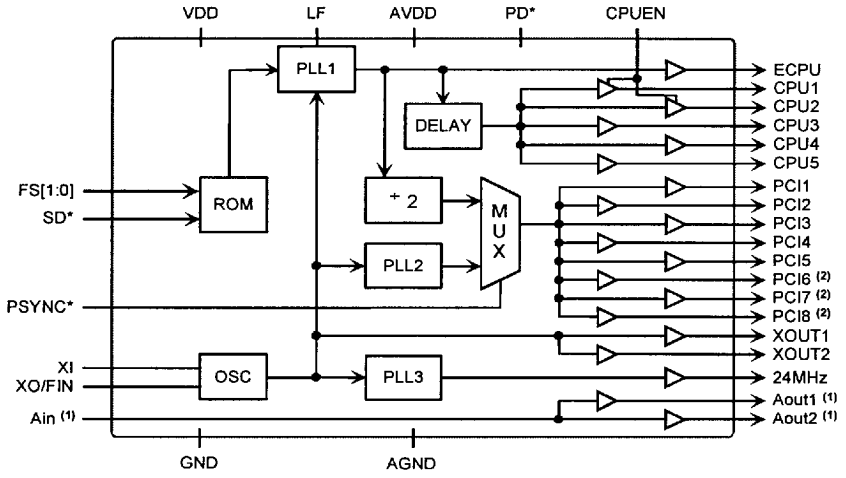

Figure 1: Block Diagram

(1) Available only with Version A

(2) Available only with Version B

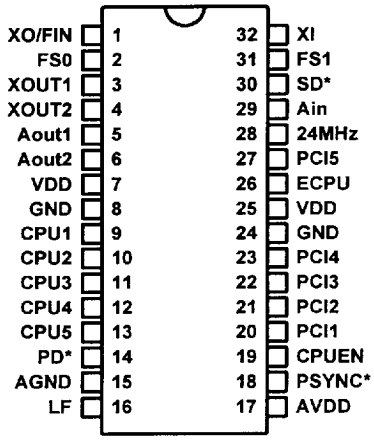

Figure 2: CH9088A

Table 1 • Pin Description CH9088A

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2, 31	In	FS0, FS1	CPU clock select inputs (internal pull-up)
3, 4	Out	XOUT1, XOUT2	Buffered reference (14.318 MHz) clock outputs
5, 6	Out	Aout1, Aout2	Buffered output pins of Ain
7, 25	Power	VDD	5V or 3.3V supply
8, 24	Power	GND	Ground
9 – 13	Out	CPU1 – CPU5	CPU clock outputs
14	In	PD*	Power down input (active low, internal pull-up). When PD* is low, internal PLLs are disabled and all outputs are tristated with a weak pull-low.
15	Power	AGND	Analog ground
16	Out	LF	External loop filter
17	Power	AVDD	Analog 5V supply
18	In	PSYNC*	Synchronous or asynchronous PCI clock select input (active low, internal pull-up)
19	In	CPUEN	CPU1 and CPU2 clock enable pin (active high, internal pull-up). When CPUEN is low, both CPU1 and CPU2 are disabled and held at a low state.
20 – 23, 27	Out	PCI1 – PCI4, PCI5	PCI clock outputs
26	Out	ECPU	Early CPU clock output
28	Out	24 MHz	24 MHz clock output
29	In	Ain	On-chip buffer input (internal pull-up)
30	In	SD*	Slow down input (active low, internal pull-up)
32	In	XI	Crystal input

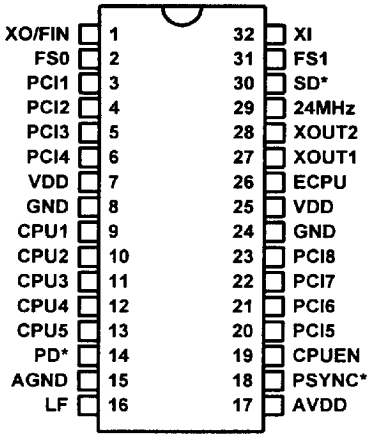

Figure 3: CH9088B

Table 2 • Pin Description CH9088B

Pin	Type	Symbol	Description
1	Out / In	XO / FIN	Crystal output or external FREF input
2, 31	In	FS0, FS1	CPU clock select inputs (internal pull-up)
3 – 6, 20 – 23	Out	PCI1 – PCI4, PCI5 – PCI8	PCI clock outputs
7, 25	Power	VDD	5V or 3.3V supply
8, 24	Power	GND	Ground
9 – 13	Out	CPU1 – CPU5	CPU clock outputs
14	In	PD*	Power down input (active low, internal pull-up). When PD* is low, internal PLLs are disabled and all outputs are tristated with a weak pull-low.
15	Power	AGND	Analog ground
16	Out	LF	External loop filter
17	Power	AVDD	Analog 5V supply
18	In	PSYNC*	Synchronous or asynchronous PCI clock select input (active low, internal pull-up)
19	In	CPUEN	CPU1 and CPU2 clock enable pin (active high, internal pull-up). When CPUEN is low, both CPU1 and CPU2 are disabled and held at a low state.
26	Out	ECPU	Early CPU clock output
27, 28	Out	XOUT1, XOUT2	Buffered reference (14.318 MHz) clock outputs
29	Out	24 MHz	24 MHz clock output
30	In	SD*	Slow down input (active low, internal pull-up)
32	In	XI	Crystal input

Table 3 • CPU Clock Output Frequency (in MHz)

CPU Clock Select Inputs		ECPU and CPU Output	
FS1	FS0	SD* = 1	SD* = 0
0	0	40.0	8.0
0	1	50.0	33.3
1	0	60.0	33.3
1	1	66.6	33.3

Note: ECPU typically precedes CPU outputs by 2 – 5 ns

Table 4 • PCI Clock Output Frequency (in MHz)

PSYNC*	PCI Output
0	CPU ÷ 2
1	33.3

Table 5 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	–0.5 TO +7.0	V
VIN	Input voltage on any pin with respect to GND	–0.5 TO VDD+0.5	V
TSTOR	Storage temperature	–55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 12mA	2.4			V
VOL	Output low voltage	VDD = 4.75V, IOL = 12mA			0.4	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			5	20	µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD[1]	Operating current	VDD = 5V CPU = 40 MHz, No load CPU = 80 MHz, No load		35 45		mA

Note: 1 Indicates values when on-chip buffers are inactive

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Table 7 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency (crystal pin)		1	14.318	32	MHz
FAIN	Input frequency (buffer input Ain)				100	MHz
TR	Output clock rise time	30 pF load, VOUT = 0.8V to 2.0V			2	ns
TF	Output clock fall time	30 pF load, VOUT = 0.8V to 2.0V			2	ns
TDC	Duty cycle		45	50	55	%
TJCC	Jitter, cycle to cycle	CPU = 50 MHz		TBD		ps
TFT	Frequency transition time	8 – 80 MHz with 0.1 µF LF capacitor		10		ms
TPU	Power up time	From OFF to 100 MHz with 0.1 µF LF capacitor		15		ms
TPLH1, TPHL1	Propagation delay (Ain to Aout)			3.2		ns
TPLH2, TPHL2	Propagation delay (ECPU to CPU)			3.2		ns
TSKEW1	Buffer out skew (same buffer group)				0.7	ns
TSKEW2	PCI to CPU (synchronous PCI)				1.5	ns

Table 8 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 3.0V, IOH = 1.5mA	VDD – 0.5			V
VOL	Output low voltage	VDD = 3.0V, IOL = 3mA			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			3		µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IDD[1]	Operating current	VDD = 3.3V CPU = 40 MHz, No load CPU = 80 MHz, No load		25 30		mA

Note: 1 Indicates values when on-chip buffers are inactive

Table 9 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @T_A = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency (crystal pin)		1	14.318	20	MHz
FAIN	Input frequency (buffer input Ain)				100	MHz
TR	Output clock rise time	30 pF load, VOUT = 0.8V to 2.0V			5	ns
TF	Output clock fall time	30 pF load, VOUT = 0.8V to 2.0V			5	ns
TDC	Duty cycle		45	50	55	%
TJCC	Jitter, cycle to cycle	CPU = 50 MHz		TBD		ps
TFT	Frequency transition time	8 – 80 MHz with 0.1 µF LF capacitor		10		ms
TPU	Power up time	From OFF to 100 MHz with 0.1 µF LF capacitor		15		ms
TPLH1, TPHL1	Propagation delay (Ain to Aout)			5		ns
TPLH2, TPHL2	Propagation delay (ECPU to CPU)			5		ns
TSKEW1	Buffer out skew (same buffer group)				0.7	ns
TSKEW2	PCI to CPU (synchronous PCI)				1.5	ns

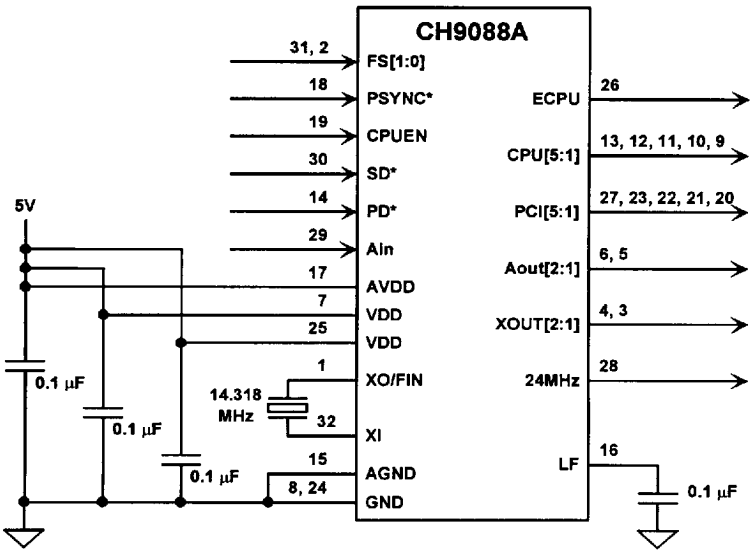

Figure 4: Application Schematic

Note: For other versions, please refer to pin descriptions for exact pin numbers and functions

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ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9088x-S	300 mil SOIC	32	5V
CH9088x-S-L	300 mil SOIC	32	3.3V
Note: x = pin description version			