

# MC74HC240A

## Octal 3-State Inverting Buffer/Line Driver/Line Receiver

### High-Performance Silicon-Gate CMOS

The MC74HC240A is identical in pinout to the LS240. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This octal noninverting buffer/line driver/line receiver is designed to be used with 3-state memory address drivers, clock drivers, and other sub-oriented systems. The device has inverting outputs and two active-low output enables.

The HC240A is similar in function to the HC244A.

#### Features

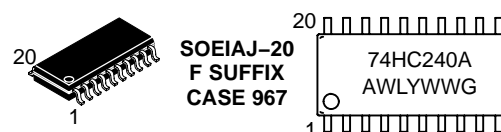
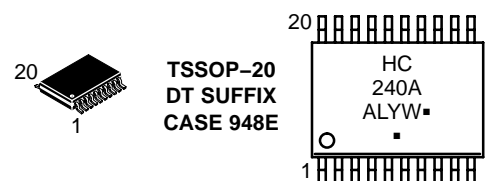
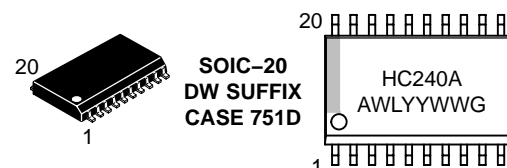
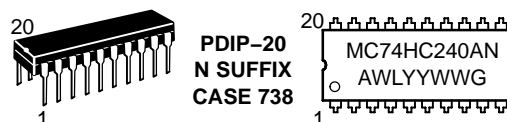
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 120 FETs or 30 Equivalent Gates
- Pb-Free Packages are Available\*



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#### MARKING DIAGRAMS



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Package  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

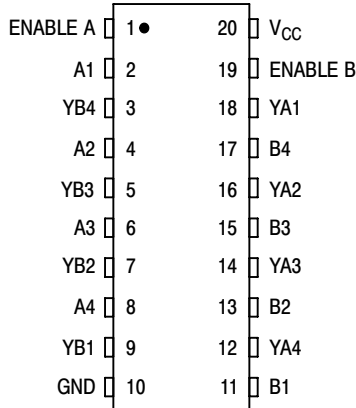
#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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## PIN ASSIGNMENT

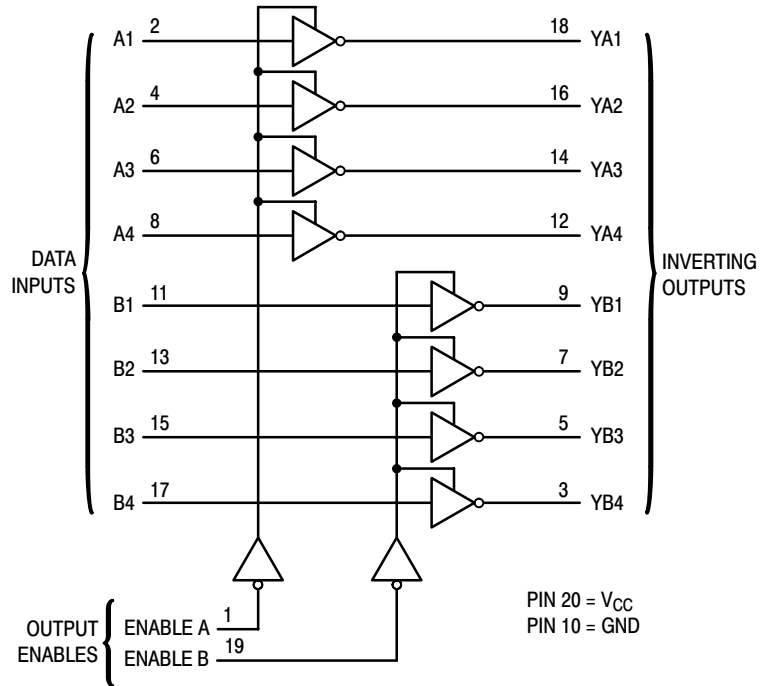


## FUNCTION TABLE

| Inputs                |      | Outputs |  |
|-----------------------|------|---------|--|
| Enable A,<br>Enable B | A, B | YA, YB  |  |
| L                     | L    | H       |  |
| L                     | H    | L       |  |
| H                     | X    | Z       |  |

Z = high impedance

## LOGIC DIAGRAM



## ORDERING INFORMATION

| Device          | Package                   | Shipping†        |
|-----------------|---------------------------|------------------|
| MC74HC240AN     | PDIP-20                   | 18 Units / Box   |
| MC74HC240ANG    | PDIP-20<br>(Pb-Free)      | 18 Units / Box   |
| MC74HC240ADW    | SOIC-20 WIDE              | 38 Units / Rail  |
| MC74HC240ADWG   | SOIC-20 WIDE<br>(Pb-Free) | 38 Units / Rail  |
| MC74HC240ADWR2  | SOIC-20 WIDE              | 1000 Tape & Reel |
| MC74HC240ADWR2G | SOIC-20 WIDE<br>(Pb-Free) | 1000 Tape & Reel |
| MC74HC240ADTR2  | TSSOP-20*                 | 2500 Tape & Reel |
| MC74HC240ADTR2G | TSSOP-20*                 | 2500 Tape & Reel |
| MC74HC240AF     | SOEIAJ-20                 | 40 Units / Rail  |
| MC74HC240AFG    | SOEIAJ-20<br>(Pb-Free)    | 40 Units / Rail  |
| MC74HC240AFEL   | SOEIAJ-20                 | 2000 Tape & Reel |
| MC74HC240AFELG  | SOEIAJ-20<br>(Pb-Free)    | 2000 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## MAXIMUM RATINGS

| Symbol    | Parameter   | Value                   | Unit |
|-----------|---|-------------------------|------|
| $V_{CC}$  | DC Supply Voltage (Referenced to GND)   | - 0.5 to + 7.0          | V    |
| $V_{in}$  | DC Input Voltage (Referenced to GND)  | - 0.5 to $V_{CC} + 0.5$ | V    |
| $V_{out}$ | DC Output Voltage (Referenced to GND)   | - 0.5 to $V_{CC} + 0.5$ | V    |
| $I_{in}$  | DC Input Current, per Pin   | $\pm 20$                | mA   |
| $I_{out}$ | DC Output Current, per Pin  | $\pm 35$                | mA   |
| $I_{CC}$  | DC Supply Current, $V_{CC}$ and GND Pins  | $\pm 75$                | mA   |
| $P_D$     | Power Dissipation in Still Air,<br>Plastic DIP†<br>SOIC Package†<br>TSSOP Package†      | 750<br>500<br>450       | mW   |
| $T_{stg}$ | Storage Temperature   | - 65 to + 150           | °C   |
| $T_L$     | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP, SOIC or TSSOP Package) | 260                     | °C   |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C  
SOIC Package: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol            | Parameter  | Min  | Max         | Unit               |    |
|-------------------|--|--|-------------|--------------------|----|
| $V_{CC}$          | DC Supply Voltage (Referenced to GND)                | 2.0  | 6.0         | V                  |    |
| $V_{in}, V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0  | $V_{CC}$    | V                  |    |
| $T_A$             | Operating Temperature, All Package Types             | - 55   | + 125       | °C                 |    |
| $t_r, t_f$        | Input Rise and Fall Time<br>(Figure 1)               | $V_{CC} = 2.0 \text{ V}$<br>$V_{CC} = 4.5 \text{ V}$<br>$V_{CC} = 6.0 \text{ V}$ | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol   | Parameter                         | Test Conditions  | $V_{CC}$<br>V | Guaranteed Limit |                         |                          | Unit |
|----------|-----------------------------------|--|---------------|------------------|-------------------------|--------------------------|------|
|          |                                   |  |               | - 55 to<br>25°C  | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ |      |
| $V_{IH}$ | Minimum High-Level Input Voltage  | $V_{out} = V_{CC} - 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$  | 2.0           | 1.5              | 1.5                     | 1.5                      | V    |
|          |                                   |  | 3.0           | 2.1              | 2.1                     | 2.1                      |      |
|          |                                   |  | 4.5           | 3.15             | 3.15                    | 3.15                     |      |
|          |                                   |  | 6.0           | 4.2              | 4.2                     | 4.2                      |      |
| $V_{IL}$ | Maximum Low-Level Input Voltage   | $V_{out} = 0.1 \text{ V}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 2.0           | 0.5              | 0.5                     | 0.5                      | V    |
|          |                                   |  | 3.0           | 0.9              | 0.9                     | 0.9                      |      |
|          |                                   |  | 4.5           | 1.35             | 1.35                    | 1.35                     |      |
|          |                                   |  | 6.0           | 1.8              | 1.8                     | 1.8                      |      |
| $V_{OH}$ | Minimum High-Level Output Voltage | $V_{in} = V_{IH}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 2.0           | 1.9              | 1.9                     | 1.9                      | V    |
|          |                                   |  | 4.5           | 4.4              | 4.4                     | 4.4                      |      |
|          |                                   |  | 6.0           | 5.9              | 5.9                     | 5.9                      |      |
|          |                                   | $V_{in} = V_{IH}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 6.0 \text{ mA}$<br>$ I_{out}  \leq 7.8 \text{ mA}$ | 3.0           | 2.48             | 2.34                    | 2.2                      |      |
|          |                                   |  | 4.5           | 3.98             | 3.84                    | 3.7                      |      |
|          |                                   |  | 6.0           | 5.48             | 5.34                    | 5.2                      |      |
| $V_{OL}$ | Maximum Low-Level Output Voltage  | $V_{in} = V_{IL}$<br>$ I_{out}  \leq 20 \mu\text{A}$   | 2.0           | 0.1              | 0.1                     | 0.1                      | V    |
|          |                                   |  | 4.5           | 0.1              | 0.1                     | 0.1                      |      |
|          |                                   |  | 6.0           | 0.1              | 0.1                     | 0.1                      |      |
|          |                                   | $V_{in} = V_{IL}$<br>$ I_{out}  \leq 2.4 \text{ mA}$<br>$ I_{out}  \leq 6.0 \text{ mA}$<br>$ I_{out}  \leq 7.8 \text{ mA}$ | 3.0           | 0.26             | 0.33                    | 0.4                      |      |
|          |                                   |  | 4.5           | 0.26             | 0.33                    | 0.4                      |      |
|          |                                   |  | 6.0           | 0.26             | 0.33                    | 0.4                      |      |

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol          | Parameter                                      | Test Conditions   | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|-----------------|--|---|----------------------|------------------|--------|---------|------|
|                 |  |   |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| I <sub>in</sub> | Maximum Input Leakage Current                  | V <sub>in</sub> = V <sub>CC</sub> or GND  | 6.0                  | ± 0.1            | ± 1.0  | ± 1.0   | μA   |
| I <sub>oZ</sub> | Maximum Three-State Leakage Current            | Output in High-Impedance State<br>V <sub>in</sub> = V <sub>IL</sub> or V <sub>IH</sub><br>V <sub>out</sub> = V <sub>CC</sub> or GND | 6.0                  | ± 0.5            | ± 5.0  | ± 10    | μA   |
| I <sub>CC</sub> | Maximum Quiescent Supply Current (per Package) | V <sub>in</sub> = V <sub>CC</sub> or GND<br>I <sub>out</sub> = 0 μA   | 6.0                  | 4.0              | 40     | 160     | μA   |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

## AC ELECTRICAL CHARACTERISTICS (C<sub>L</sub> = 50 pF, Input t<sub>r</sub> = t<sub>f</sub> = 6 ns)

| Symbol                                 | Parameter  | V <sub>CC</sub><br>V | Guaranteed Limit |        |         | Unit |
|--|--|----------------------|------------------|--------|---------|------|
|  |  |                      | - 55 to<br>25°C  | ≤ 85°C | ≤ 125°C |      |
| t <sub>PLH</sub> ,<br>t <sub>PHL</sub> | Maximum Propagation Delay, A to YA or B to YB<br>(Figures 1 and 3)         | 2.0                  | 80               | 100    | 120     | ns   |
|  |  | 3.0                  | 40               | 50     | 60      |      |
|  |  | 4.5                  | 16               | 20     | 24      |      |
|  |  | 6.0                  | 14               | 17     | 20      |      |
| t <sub>PLZ</sub> ,<br>t <sub>PHZ</sub> | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4)  | 2.0                  | 110              | 140    | 165     | ns   |
|  |  | 3.0                  | 60               | 70     | 80      |      |
|  |  | 4.5                  | 22               | 28     | 33      |      |
|  |  | 6.0                  | 19               | 24     | 28      |      |
| t <sub>PZL</sub> ,<br>t <sub>PZH</sub> | Maximum Propagation Delay, Output Enable to YA or YB<br>(Figures 2 and 4)  | 2.0                  | 110              | 140    | 165     | ns   |
|  |  | 3.0                  | 60               | 70     | 80      |      |
|  |  | 4.5                  | 22               | 28     | 33      |      |
|  |  | 6.0                  | 19               | 24     | 28      |      |
| t <sub>TLH</sub> ,<br>t <sub>THL</sub> | Maximum Output Transition Time, Any Output<br>(Figures 1 and 3)            | 2.0                  | 60               | 75     | 90      | ns   |
|  |  | 3.0                  | 23               | 27     | 32      |      |
|  |  | 4.5                  | 12               | 15     | 18      |      |
|  |  | 6.0                  | 10               | 13     | 15      |      |
| C <sub>in</sub>                        | Maximum Input Capacitance  | –                    | 10               | 10     | 10      | pF   |
| C <sub>out</sub>                       | Maximum Three-State Output Capacitance<br>(Output in High-Impedance State) | –                    | 15               | 15     | 15      | pF   |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C <sub>PD</sub> | Power Dissipation Capacitance (Per Transceiver Channel)* | Typical @ 25°C, V <sub>CC</sub> = 5.0 V | pF |
|-----------------|--|---|----|
|                 |  | 32                                      |    |

\* Used to determine the no-load dynamic power consumption: P<sub>D</sub> = C<sub>PD</sub> V<sub>CC</sub><sup>2</sup>f + I<sub>CC</sub> V<sub>CC</sub>. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

# MC74HC240A

## SWITCHING WAVEFORMS

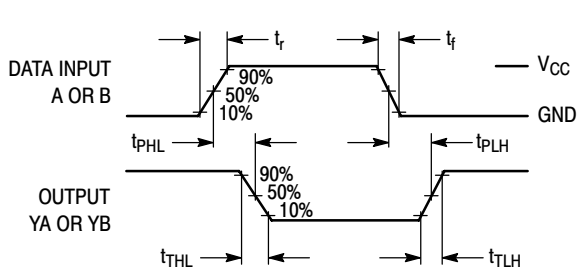


Figure 1.

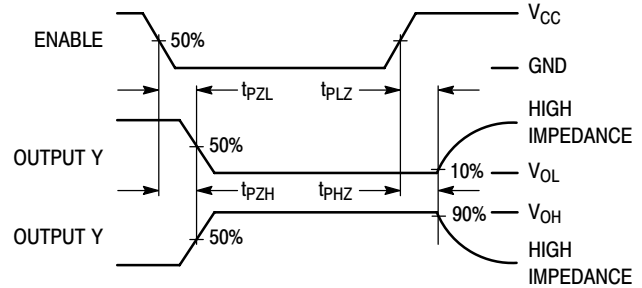
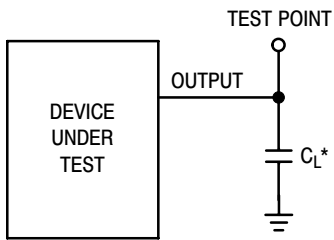
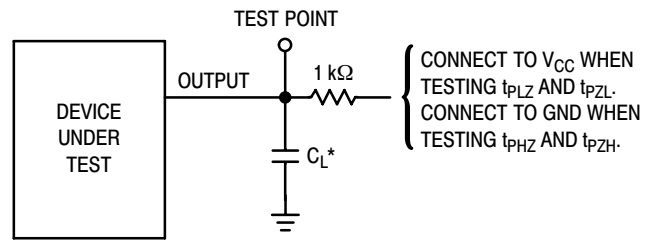


Figure 2.



\*Includes all probe and jig capacitance

Figure 3. Test Circuit



\*Includes all probe and jig capacitance

Figure 4. Test Circuit

## PIN DESCRIPTIONS

### INPUTS

**A1, A2, A3, A4, B1, B2, B3, B4**  
(Pins 2, 4, 6, 8, 11, 13, 15, 17)

Data input pins. Data on these pins appear in inverted form on the corresponding Y outputs, when the outputs are enabled.

### CONTROLS

**Enable A, Enable B (Pins 1, 19)**

Output enables (active-low). When a low level is applied to these pins, the outputs are enabled and the devices

function as inverters. When a high level is applied, the outputs assume the high-impedance state.

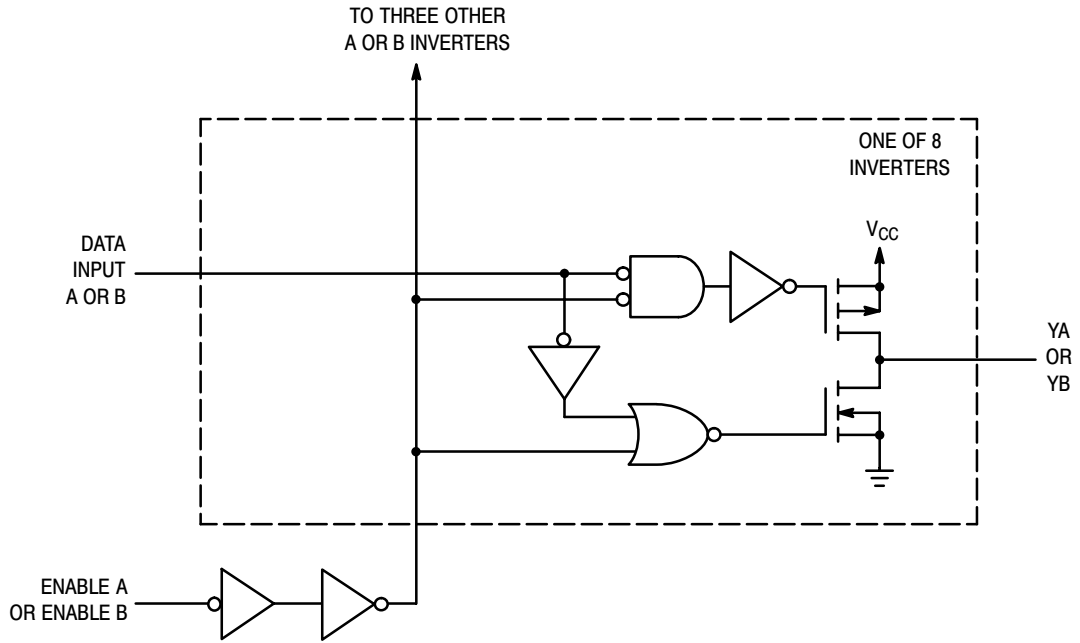
### OUTPUTS

**YA1, YA2, YA3, YA4, YB1, YB2, YB3, YB4**  
(Pins 18, 16, 14, 12, 9, 7, 5, 3)

Device outputs. Depending upon the state of the output-enable pins, these outputs are either inverting outputs or high-impedance outputs.

# MC74HC240A

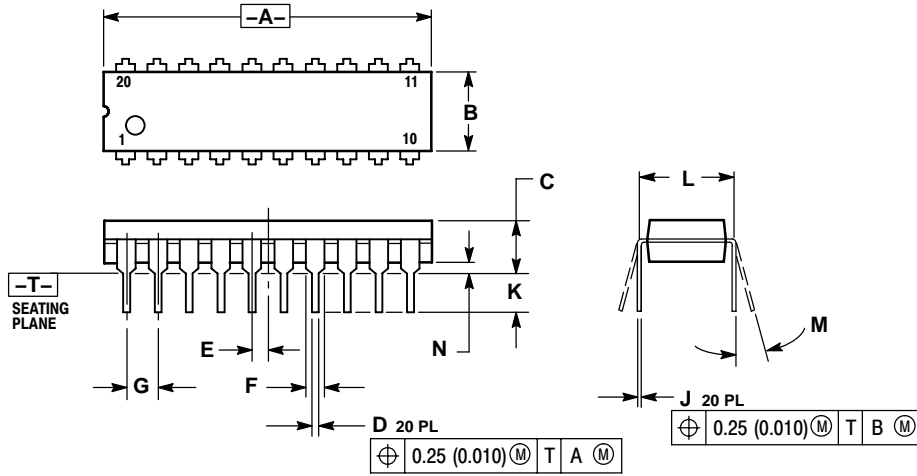
## LOGIC DETAIL



# MC74HC240A

## PACKAGE DIMENSIONS

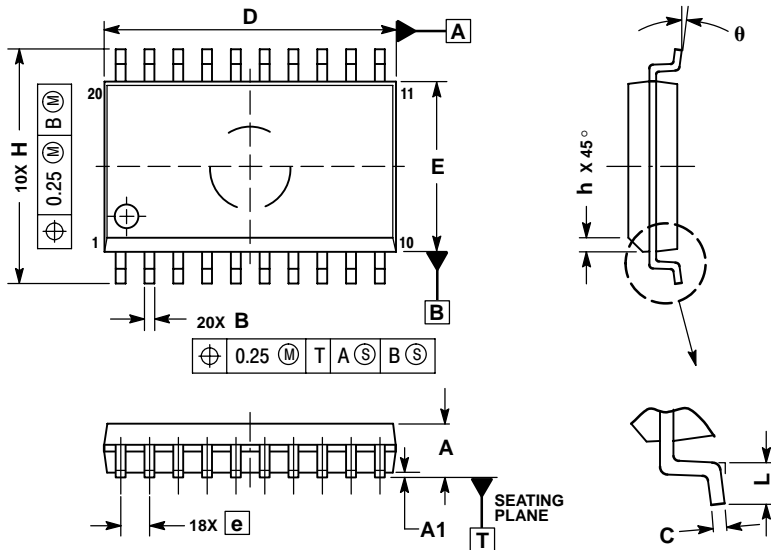
PDIP-20  
N SUFFIX  
PLASTIC DIP PACKAGE  
CASE 738-03  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
  4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES    |       | MILLIMETERS |       |
|-----|-----------|-------|-------------|-------|
|     | MIN       | MAX   | MIN         | MAX   |
| A   | 1.010     | 1.070 | 25.66       | 27.17 |
| B   | 0.240     | 0.260 | 6.10        | 6.60  |
| C   | 0.150     | 0.180 | 3.81        | 4.57  |
| D   | 0.015     | 0.022 | 0.39        | 0.55  |
| E   | 0.050 BSC |       | 1.27 BSC    |       |
| F   | 0.050     | 0.070 | 1.27        | 1.77  |
| G   | 0.100 BSC |       | 2.54 BSC    |       |
| J   | 0.008     | 0.015 | 0.21        | 0.38  |
| K   | 0.110     | 0.140 | 2.80        | 3.55  |
| L   | 0.300 BSC |       | 7.62 BSC    |       |
| M   | 0° 15°    |       | 0° 15°      |       |
| N   | 0.020     | 0.040 | 0.51        | 1.01  |

SOIC-20  
DW SUFFIX  
CASE 751D-05  
ISSUE G



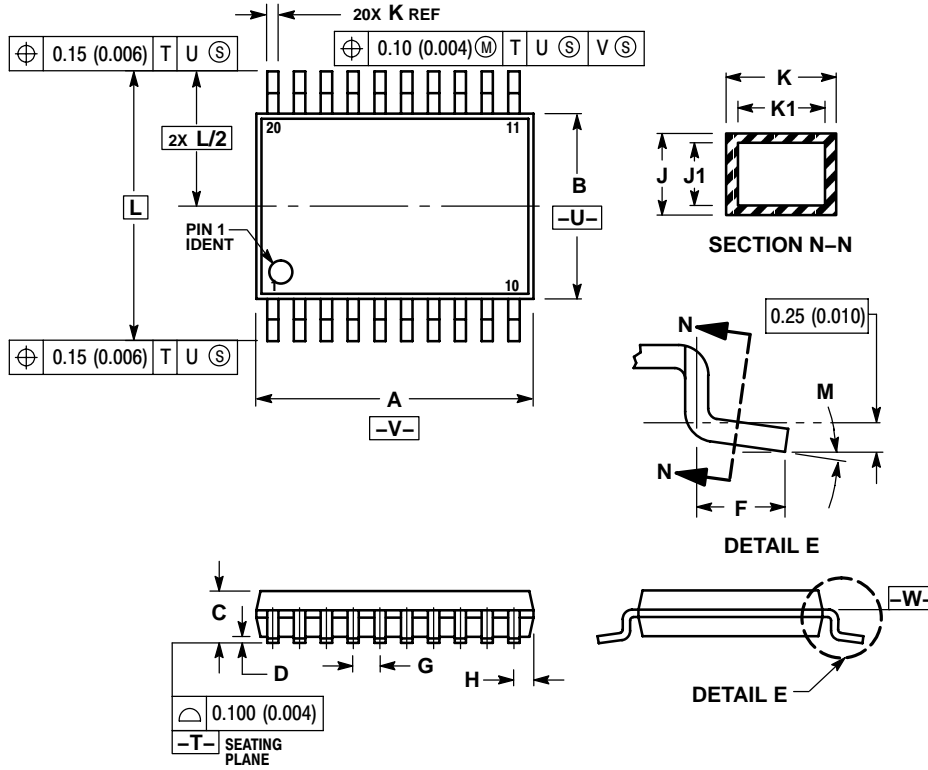
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM      | MILLIMETERS |       |
|----------|-------------|-------|
|          | MIN         | MAX   |
| A        | 2.35        | 2.65  |
| A1       | 0.10        | 0.25  |
| B        | 0.35        | 0.49  |
| C        | 0.23        | 0.32  |
| D        | 12.65       | 12.95 |
| E        | 7.40        | 7.60  |
| e        | 1.27 BSC    |       |
| H        | 10.05       | 10.55 |
| h        | 0.25        | 0.75  |
| L        | 0.50        | 0.90  |
| $\theta$ | 0° 7°       |       |

# MC74HC240A

## PACKAGE DIMENSIONS

TSSOP-20  
DT SUFFIX  
CASE 948E-02  
ISSUE B



### NOTES:

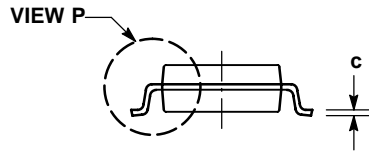
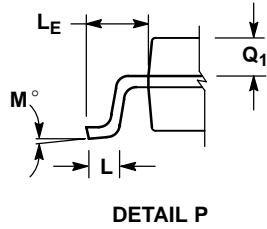
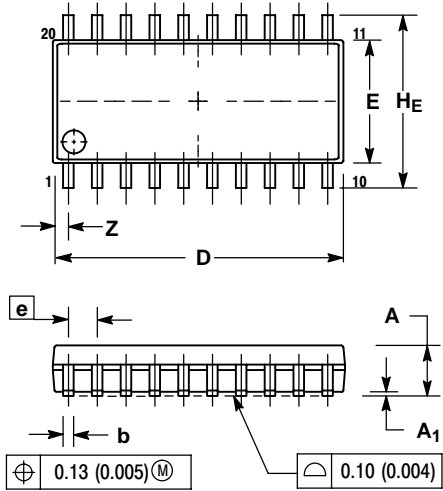
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.



# MC74HC240A

## PACKAGE DIMENSIONS

SOEIAJ-20  
F SUFFIX  
CASE 967-01  
ISSUE O



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 12.35       | 12.80 | 0.486     | 0.504 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| HE             | 7.40        | 8.20  | 0.291     | 0.323 |
| LE             | 0.50        | 0.85  | 0.020     | 0.033 |
| L              | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 0.81  | ---       | 0.032 |

# MC74HC240A

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