T-46-23-12

Military Standard Products

UT6M628 Radiation-Hardened 8K x 16 SRAM -- SEU Hard

Preliminary Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

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FEATURES

- ☐ 55ns maximum address access time, single-event upset less than 1.0E-10 errors/bit-day (-55°C to +125°C)
- ☐ High-density 128K-bit CMOS SRAM utilizing UTMC's high performance 64K-bit SRAM
- ☐ Organized 8K x 16, separate control of upper byte (DQ15 through DQ8) and lower byte (DQ7 through DQ0)
- ☐ CMOS-compatible output levels
- ☐ Three-state bidirectional data bus
- ☐ Low operating and standby current
- ☐ Full military operating temperature range, -55°C to +125°C, screened to specific test methods listed in Table I MIL-STD-883 Method 5004 for Class S or Class B
- ☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883 Method 1019
  - Total-dose: 1.0E6 rads(Si)
  - Dose rate upset: 1.0E9 rads(Si)/sec
  - Dose rate survival: 1.0E12 rads(Si)/sec
  - Single-event upset: <1.0E-10 errors/bit-day
- ☐ Packaging options:
  - 40-pin 100-mil center DIP (.610 x 2.0)
- ☐ 5-volt operation
- ☐ Post-radiation AC/DC performance characteristics guaranteed by MIL-STD-883 Method 1019 testing at 1.0E6 rads(Si)

Advanced CMOS processing along with a device enable/disable function result in a high performance, power saving SRAM. Inputs $\overline{UB}$, $\overline{LB}$, and E control this unique feature, negation of $\overline{UB}$ or $\overline{LB}$ disables all or segments of the 128K-bit memory. Negation of E deselects the entire 8K x 16 of memory. The combination of radiation-hardness, fast access time, and low power consumption make the UT6M628 ideal for high-speed systems designed for operation in radiation environments.

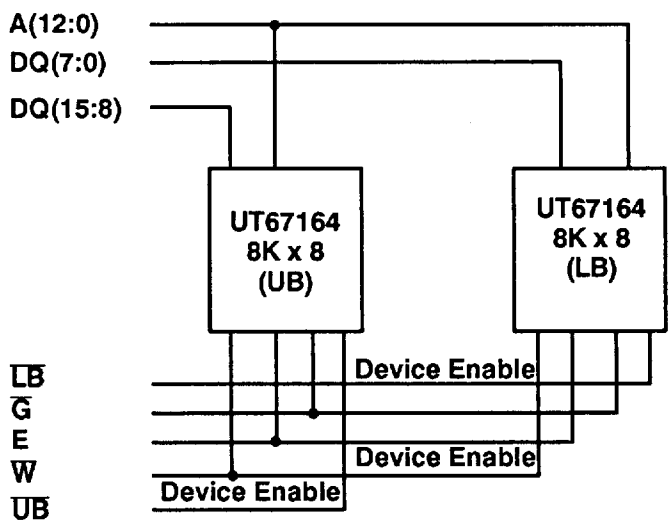


Figure 1. SRAM Block Diagram

INTRODUCTION

The UT6M628 SRAM is a high performance, asynchronous, radiation-hardened, 8K x 16 random access memory device. The UT6M628 features fully static operation requiring no external clocks or timing strobes. Comprised of two 8K x 8 SRAMs, the system designer has the flexibility to access either the upper byte or lower byte of any word. The maximum access time for this device is 55ns over the full military temperature range.

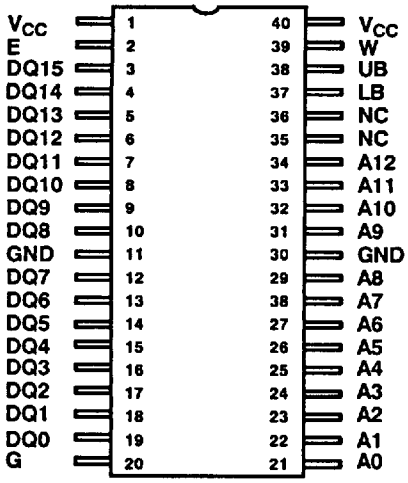


Figure 2. SRAM Pinout

PIN NAMES

A(12:0)	Address	$\overline{W}$	Write
DQ(15:0)	Data Input/Output	$\overline{G}$	Output Enable
$\overline{LB}$	Low Byte Select	V_{DD}	Power
$\overline{UB}$	High Byte Select	V_{SS}	Ground
E	Chip Enable		

DEVICE OPERATION

The UT6M628 has five control inputs called Upper Byte ($\overline{UB}$), Lower Byte ($\overline{LB}$), Chip Enable (E), Write Enable ($\overline{W}$), and Output Enable ($\overline{G}$); thirteen address inputs, A(12:0); and sixteen bidirectional data lines, DQ(15:0). Inputs $\overline{LB}$ and $\overline{UB}$ in conjunction with E control the selection of each 8K x 8 page of memory. For byte wide systems (i.e., x 8) inputs $\overline{LB}$ and $\overline{UB}$ function as high order address bits. Systems implementing word organization (i.e., x 16) use inputs $\overline{LB}$ and $\overline{HB}$ as device selects along with E. Input E is a global device select that requires assertion to gain access (read or write) to the SRAM device. $\overline{W}$ controls read and write operations. During a read cycle, assert $\overline{G}$ to enable the outputs. Asserting E and either or both $\overline{UB}$ or $\overline{LB}$ enables the device, resulting in a rise of I_{DD} to its active value, and the decode of address input A(12:0) to select one of 8,192 memory locations. Please note that $\overline{LB}$ and $\overline{UB}$ also function as device selects; negation of both these inputs disables the entire SRAM.

Table 1. Device Operation Truth Table

$\overline{G}$	$\overline{W}$	E	$\overline{UB}$	$\overline{LB}$	I/O Mode	Mode
X[1]	X	0	X	X	3-state	Standby
X	X	X	1	1	3-state	Standby
1	1	1	X	X	3-state	Read [2]
X	0	1	X/0	0/X	Data in	Write [3,5]
0	1	1	X/0	0/X	Data out	Read [4,5]

Notes:
1. "X" is defined as a "don't care."
2. Device active; outputs disabled. If $\overline{UB}$=$\overline{LB}$ then I/O Mode is 3-state and Mode is stand-by.
3. Write mode. If $\overline{UB}$=$\overline{LB}$ then I/O Mode is 3-state and Mode is stand-by.
4. Read mode. If $\overline{UB}$=$\overline{LB}$ then I/O Mode is 3-state and Mode is stand-by.
5. Either $\overline{UB}$ or $\overline{LB}$ must be low.

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH} (min), $\overline{UB}$ and/or $\overline{LB}$ less than V_{IL} (max), $\overline{G}$ less than V_{IL} (max), and E greater than V_{IH} (min) defines a read cycle. Read access time is measured from the latter assertion of device enable, byte select ($\overline{UB}$ and/or $\overline{LB}$), Output Enable, or valid address to valid data output.

Read Cycle 1, the Address Access read in figure 3a, is initiated by a change in address inputs while the device is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid eight or sixteen-bit data appears on data outputs after the specific t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as device enables and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}).

Figure 3b shows Read Cycle 2, the Device Enable-controlled Access. For this cycle, $\overline{G}$ remains asserted, $\overline{W}$ remains negated, and the addresses remain stable for the entire cycle. After the specified t_{ELQV} is satisfied, the eight or sixteen-bit word addressed by A(12:0) is accessed and appears at the data outputs.

Figure 3c shows Read Cycle 3, the Output Enable-controlled Access. For this cycle, assert E and either or both $\overline{UB}$ and $\overline{LB}$, $\overline{W}$ is deasserted, and the address inputs are stable before $\overline{G}$ is enabled. Read access time is t_{GLQV} unless t_{AVQV} or t_{ETQV} have not been satisfied.

WRITE CYCLE

A combination of $\overline{W}$ less than V_{IL} (max), $\overline{UB}$ and/or $\overline{LB}$ less than V_{IL} (max), and E greater than V_{IH} (min) defines a write cycle. The state of $\overline{G}$ is a "don't care" for a write cycle. The outputs are placed in the high-impedance state when either $\overline{G}$ is greater than V_{IH} (min), or when $\overline{W}$ is less than V_{IL} (max).

Write Cycle 1, the Write Enable-controlled Access shown in figure 4a, is defined as a write cycle terminated by the negation of $\overline{W}$, with E and $\overline{UB}$ and/or $\overline{LB}$ still active. The write pulse width is defined by t_{WLWH} when the write is initiated and terminated by $\overline{W}$, and by t_{ETWH} when the write is initiated by the latter device enable assertion (i.e., E, $\overline{LB}$, $\overline{UB}$). Unless the outputs have been previously placed in the high-impedance state by negating $\overline{G}$, the user must wait t_{WLQZ} before applying data to the data input bus to avoid bus contention.

Write Cycle 2, the Device Enable-controlled Access shown in figure 4b, is defined by a write cycle terminated by the negation of a device enable (i.e., E, $\overline{LB}$, $\overline{UB}$). The write pulse width is defined by t_{WLEF} when the write cycle is initiated by $\overline{W}$, and by t_{ETEF} when the write is initiated and terminated by a device enable assertion. For the $\overline{W}$ initiated write, unless the outputs have been previously placed in the high-impedance state by $\overline{G}$, the user must wait t_{WLQZ} before applying data to the data input bus to avoid bus contention.

RADIATION HARDNESS

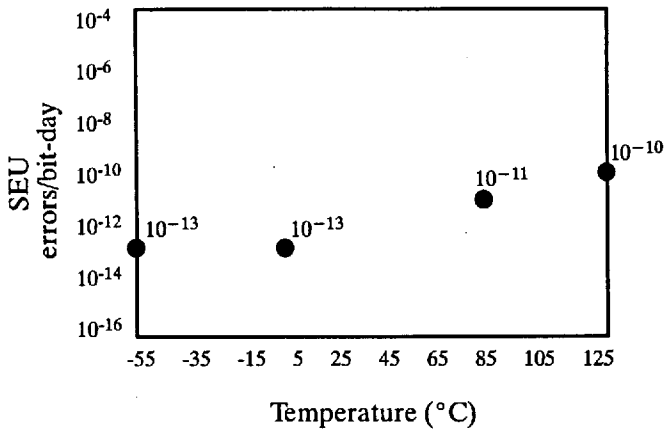
The UT6M628 SRAM device incorporates two UTMC 8K x 8 SRAMs designed for operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

Table 2. Radiation Hardness Design Specifications [1]

Total Dose	1.0E6	rads(Si)
Dose Rate Upset	1.0E9	rads(Si)/s 20ns pulse
Dose Rate Survival	1.0E12	rads(Si)/s 20ns pulse
Single-Event Upset [2]	1.0E-10	errors/bit-day
Neutron Fluence	3.0E14	n/cm^2

Notes:
1. The SRAM will not latchup during radiation exposure under recommended operating conditions.
2. 90% Adam's worst case spectrum (-55°C to +125°C).

Table 3. SEU versus Temperature



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ABSOLUTE MAXIMUM RATINGS [1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS
V_{DD}	DC supply voltage	-0.3 to 7.0V
$V_{I/O}$	Voltage on any pin	-0.5V to V_{DD} + 0.5
T_{STG}	Storage temperature	-65 to +150°C
P_D	Maximum power dissipation	2.5W
T_J	Maximum junction temperature	+175°C
Θ_{JC} [2]	Thermal resistance, junction-to-case	10°C/W
I_{LU}	Latchup immunity	± 150 mA
I_I	DC input current	± 10 mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS
V_{DD}	Positive supply voltage	4.5 to 5.5V
T_C	Case temperature range	-55 to +125°C
V_{IN}	DC input voltage	0V to V_{DD}

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DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2.2		V
V_{IL}	Low-level input voltage			0.8	V
V_{OL}	Low-level output voltage	I_{OL} = 8mA, V_{DD} = 4.5V		0.4	V
V_{OH}	High-level output voltage	I_{OH} = -8mA, V_{DD} = 4.5V	2.4		V
C_{IN} [1]	Input capacitance	f = 1MHz @ 0V, V_{DD} = 4.5V		30	pF
C_{IO} [1]	Bidirectional I/O capacitance	f = 1MHz @ 0V, V_{DD} = 4.5V		40	pF
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-20	20	µA
I_{OZ}	Three-state output leakage current TTL outputs	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V $\overline{G}$ = 5.5V	-10	10	µA
I_{OS} [2,3]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	 -90	90	mA mA
I_{DD}(OP)	Supply current operating @ 1MHz (x16) @ 18MHz (x16)	CMOS inputs (i.e., I_{OUT} = 0) V_{DD} = 5.5V V_{DD} = 5.5V		 80 160	mA
I_{DD}(SB) **pre-rad** **post-rad**	Supply current standby (x 16)	CMOS inputs (i.e., I_{OUT} = 0) $\overline{E}$ = V_{SS} +0.5 V_{DD} = 5.5V or $\overline{UB}$ and $\overline{LB}$ = V_{DD} -.05V		 400 6	 µA mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

1. Measured only for initial qualification, and after process or design changes that could affect input/output capacitance.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.

AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

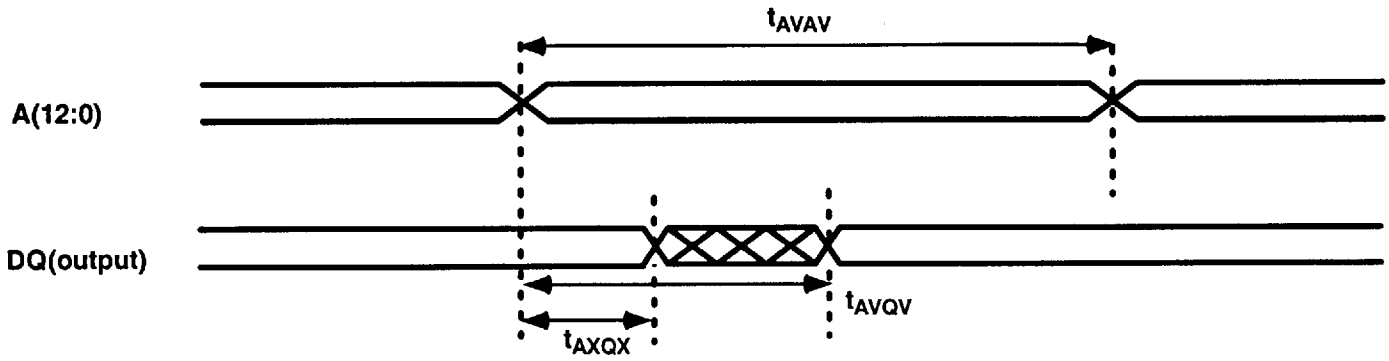
(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	6M628-85 MIN	6M628-85 MAX	6M628-70 MIN	6M628-70 MAX	6M628-55 MIN	6M628-55 MAX	UNIT
t_{AVAV}	Read cycle time	85		70		55		ns
t_{AVQV}	Read access time		85		70		55	ns
t_{AXQX}	Output hold time	5		5		5		ns
t_{GLQX}	$\overline{G}$-controlled output enable time	0		0		0		ns
t_{GLQV}	$\overline{G}$-controlled output enable time (Read Cycle 3)		30		15		15	ns
t_{GHQZ}	$\overline{G}$-controlled output three-state time		15		15		15	ns
t_{ETQX} [1]	E-controlled output enable time	0		0		0		ns
t_{ETQV} [1]	E-controlled access time		85		70		55	ns
t_{EFQZ} [2]	E-controlled output three-state time		25		20		20	ns

Notes:

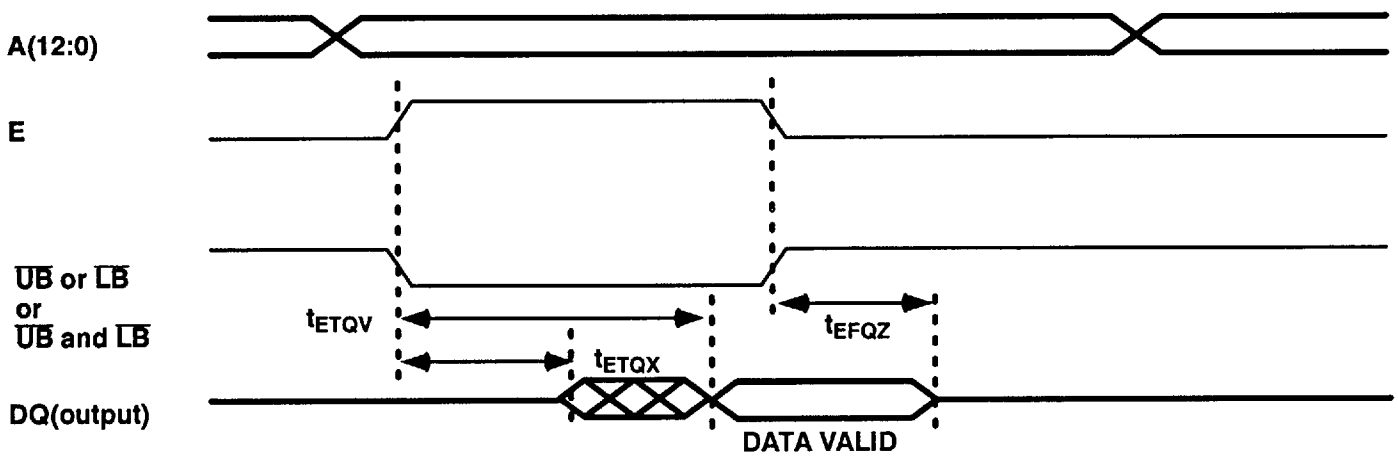
* Post-radiation performance guaranteed at 25°C to meet MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

1. The ET (enable true) notation refers to the assertion of E, $\overline{UB}$, or $\overline{LB}$, or $\overline{UB}$ and $\overline{LB}$, whichever comes last. SEU immunity does not affect the read parameters.
2. The EF (enable false) notation refers to the negation of E, $\overline{UB}$, or $\overline{LB}$, or $\overline{UB}$ and $\overline{LB}$, whiver comes first. SEU immunity does not affect the read parameters.



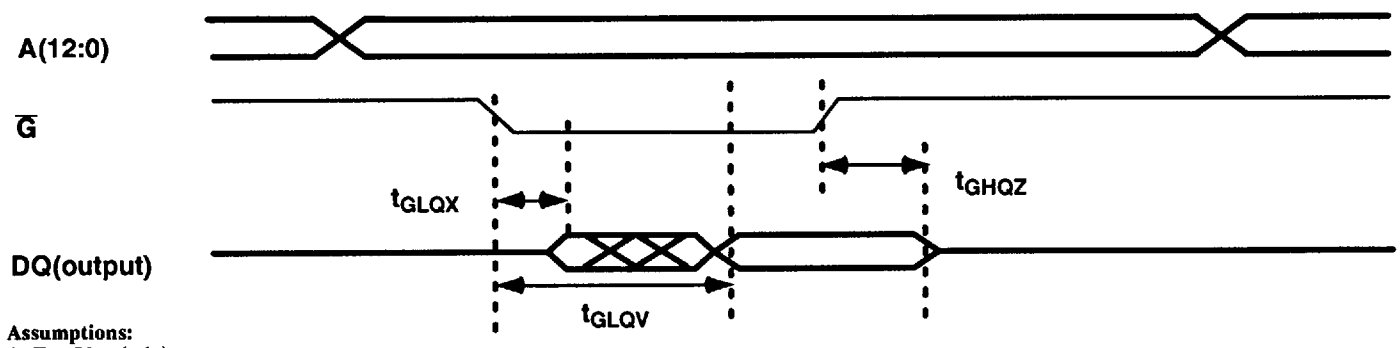
Assumptions:
1. $E \geq V_{IH}$ (min)
2. $\overline{LB}$ or $\overline{UB} \leq V_{IL}$ (max), or $\overline{LB}$ and $\overline{UB} \leq V_{IL}$ (max)

Figure 3a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 3b. SRAM Read Cycle 2: Chip Enable Access



Assumptions:
1. $E \geq V_{IH}$ (min)
2. $W > V_{IH}$ (min)
3. $\overline{LB}$ or $\overline{UB} \leq V_{IL}$ (max), or $\overline{LB}$ and $\overline{UB} \leq V_{IL}$ (max)

Figure 3c. SRAM Read Cycle 3: Output Enable Access

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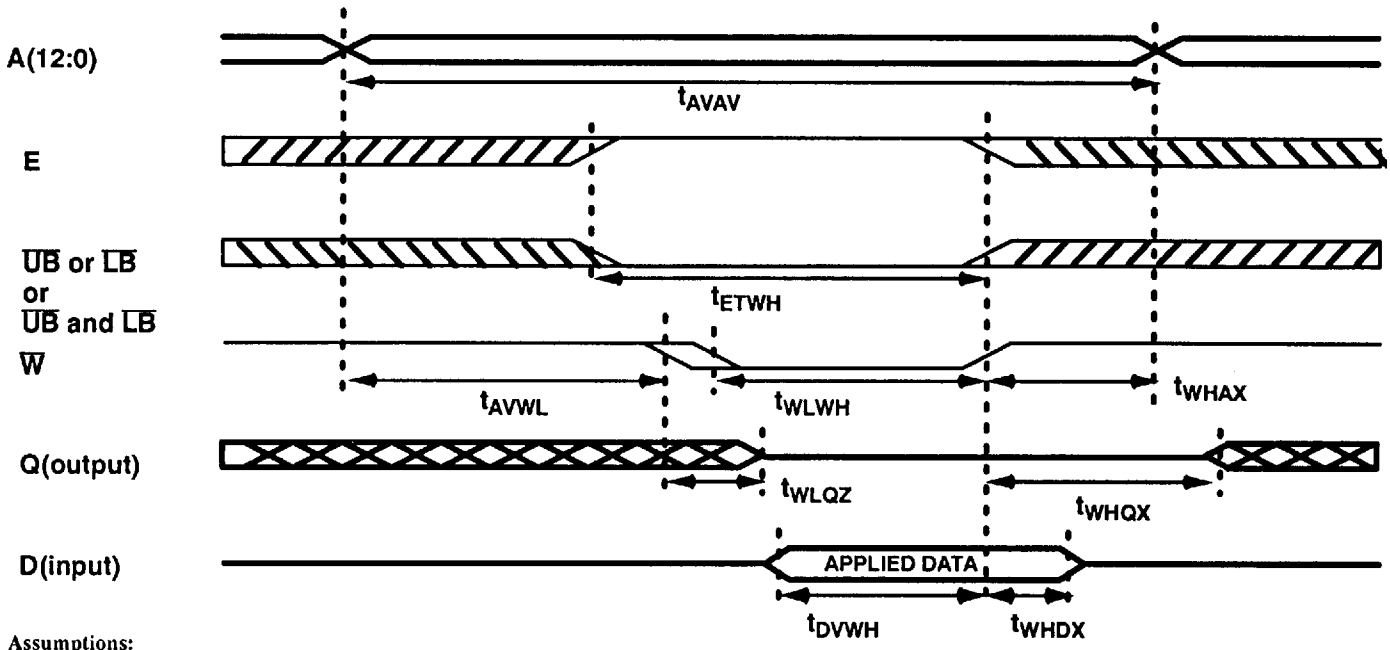
AC CHARACTERISTICS WRITE CYCLE (Post-Radiation)*

(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

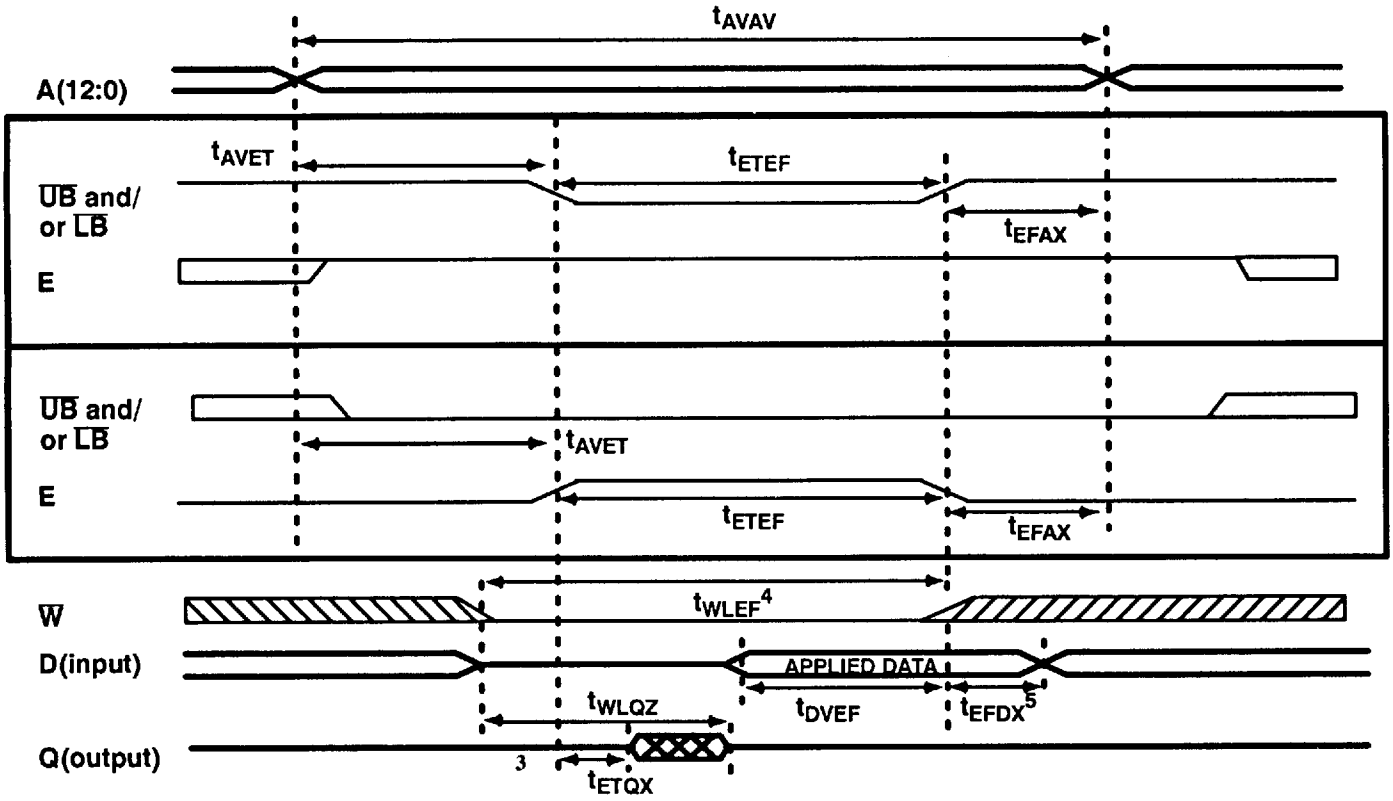
SYMBOL	PARAMETER	6M628-85 MIN	6M628-85 MAX	6M628-70 MIN	6M628-70 MAX	6M628-55 MIN	6M628-55 MAX	UNIT
t_{AVAV}	Write cycle time	85		70		55		ns
t_{ETWH}	Device enable to end of write	65		60		50		ns
t_{AVET}	Address setup time for write (Enable - controlled)	0		0		0		ns
t_{AVWL}	Address setup time for write ($\overline{W}$ - controlled)	0		0		0		ns
t_{WLWH}	Write pulse width	50		35		35		ns
t_{WHAX}	Address hold time for write ($\overline{W}$ - controlled)	0		0		0		ns
t_{EFAX}	Address hold time for device enable (Enable - controlled)	0		0		0		ns
t_{WLQZ}	$\overline{W}$-controlled three-state time		15		15		15	ns
t_{WHQX}	$\overline{W}$-controlled output enable time	0		0		0		ns
t_{ETEF}	Device enable pulse width (Enable - controlled)	65		60		50		ns
t_{DVWH}	Data setup time	50		35		35		ns
t_{WHDX}	Data hold time	0		0		0		ns
t_{WLEF}	Device enable controlled write pulse width	65		60		50		ns
t_{DVEF}	Data setup time	50		35		35		ns
t_{EFDX}	Data setup time	0		0		0		ns

Note:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(15:0) will be in three-state for the entire cycle.

Figure 4a. SRAM Write Cycle 1: $\overline{W}$-Controlled Access



Assumptions & Notes:
1. $\overline{G} \leq V_{IL}$ (max). If $\overline{G} \geq V_{IH}$ (min) then Q(15:0) will be in three-state for the entire cycle.
2. If $\overline{E}$, $\overline{UB}$ and/or $\overline{LB}$ assert simultaneously with or after the $\overline{W}$ low transition, the outputs will remain in a high-impedance state.
3. $t_{WLEF} = t_{ETWH}$
4. $t_{EFDX} = t_{WHDX}$
5. $t_{DVEF} = t_{DVWH}$

Figure 4b. SRAM Write Cycle 2: Enable-Controlled Access

DATA RETENTION CHARACTERISTICS (Post-Radiation)*

(T_C = 25°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM V_{DD} @ 2.0V	MAXIMUM V_{DD} @ 3.0V	UNIT
V_{DR}	V_{DD} for data retention	2.0	--	--	V
V I_{DDDR} [1]	Data retention current	--	75	90	µA
t_{EFR} [1]	Chip deselect to data retention time	0			ns
t_R [1]	Operation recovery time	t_{AVAV}			ns

Notes:
* Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
1. V_{LC} = 0.2V
   $V_{HC} = V_{DD}$ - 0.2V
   $E \geq LC$, $\overline{UB}$ and $\overline{LB} \leq V_{LC}$

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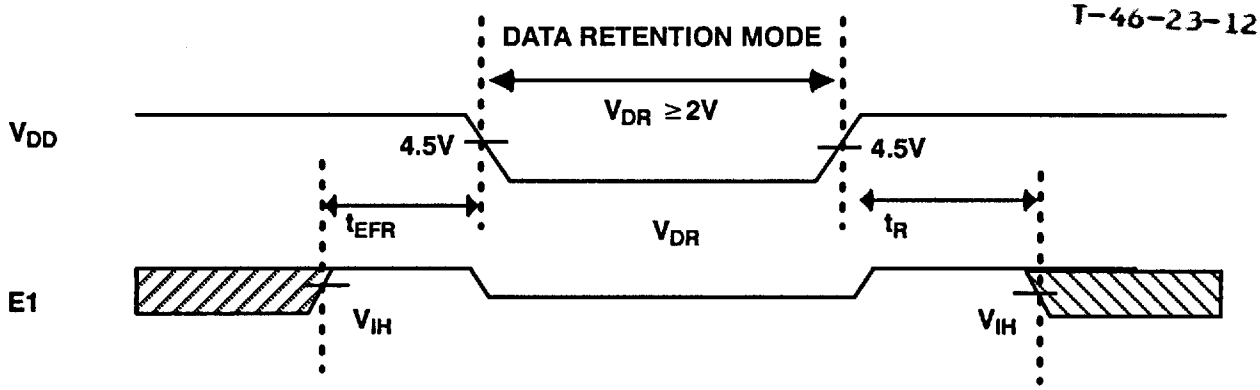
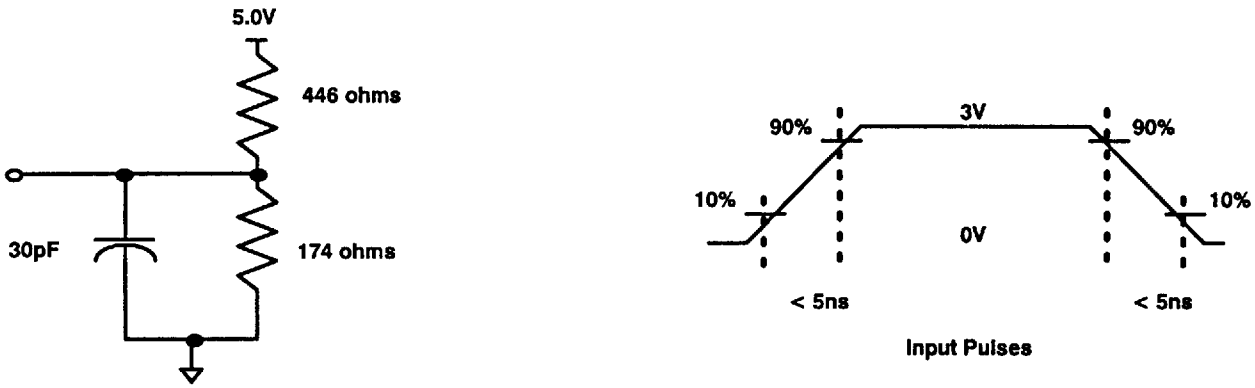


Figure 5. Low V_{DD} Data Retention Waveform



Assumptions:
1. 30pF including scope probe and test socket.
2. Measurement of data output occurs at the low-to-high or high-to-low transition mid-point.

Figure 6. AC Test Loads and Input Waveforms

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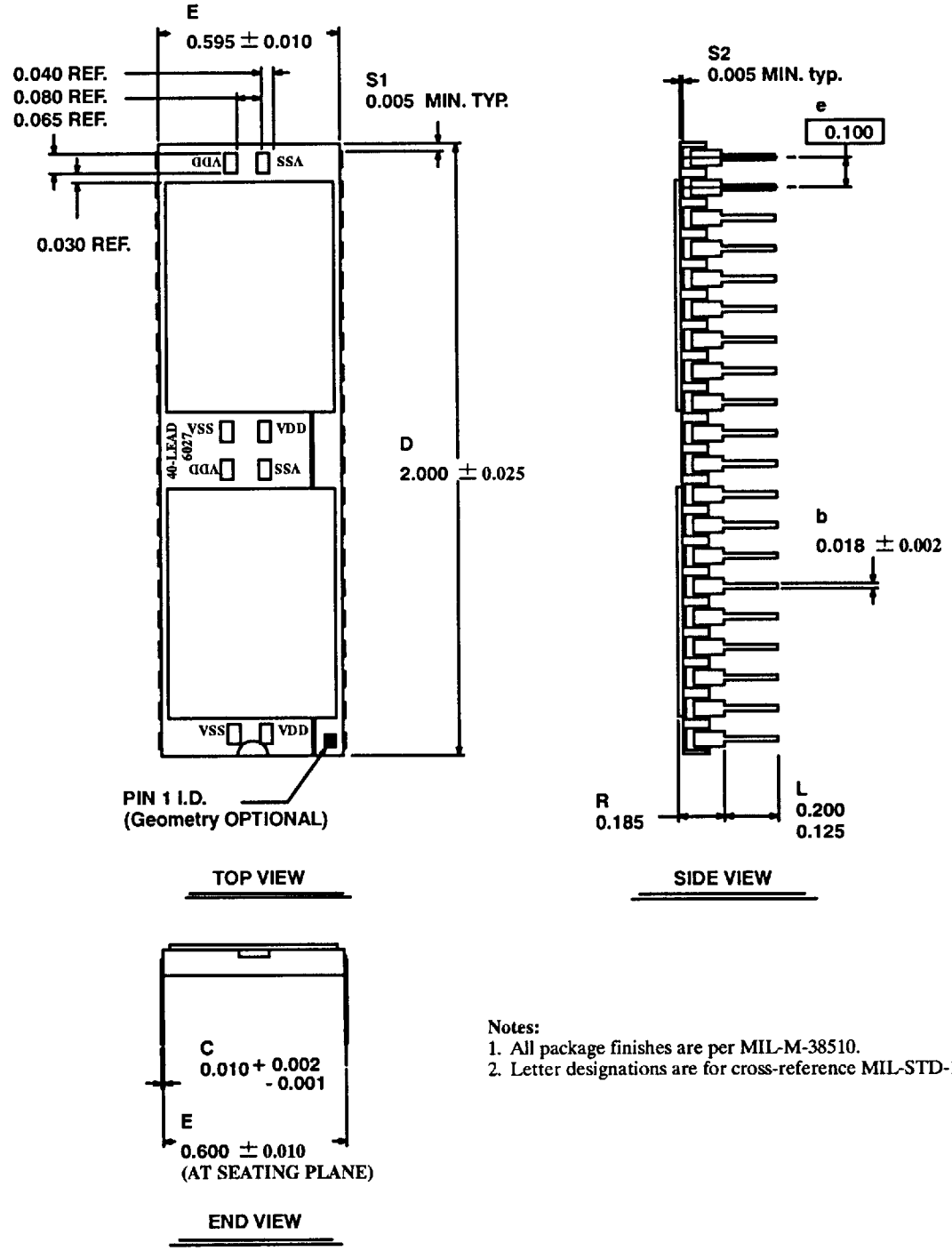

Notes:
1. All package finishes are per MIL-M-38510.
2. Letter designations are for cross-reference MIL-STD-1835.

Figure 7. 40-pin Side-Brazed DIP