synchro/resolver to digital converter
low profile two speed 16 bit
series 168T500

NEW LOW PROFILE!

FEATURES

- Latched 3-state 8/16 bit byte outputs
- 1:36 and binary speed ratios
- Single low profile module
- Over-voltage and transient protection
- High input impedance
- No external transformer modules required
- High speed tracking

APPLICATIONS

Ordinance Control—Radar Tracking Systems—Navigation Systems—Collision Avoidance Systems

GENERAL DATA

The Series 168T500 is a complete two-speed, high performance, synchro (or resolver) to digital converter packaged in a single low profile module. Module includes two-speed combining, crossover network and stickoff circuits necessary for two speed conversion. Units can be specified over the frequency ranges of either 47 to 3000 Hz or 350 to 3000 Hz.

Typical of tracking-type converters, two-speed synchro (or resolver) input data is accurately and continuously converted to 16 bits with no velocity induced errors at up to specified tracking rates. The binary angle output is 3-state addressed as either two 8 bit bytes or a single 16 bit word. The binary output can be latched indefinitely via the Inhibit input pin.

All units are completely trimmed and adjustment-free, allowing absolute interchangeability. Reliability is assured by the use of high grade components rigidly encapsulated and electrically stressed to the lowest possible levels.

THEORY OF OPERATION

The theory of operation for a single-speed tracking synchro to digital (S/D) converter is explained first. The same principles apply for a resolver to digital converter.

Single-Speed Converter (See Figure 1)

The S/D converter determines the value of the input angle ϕ by comparing a digital feedback angle Θ with the synchro input angle. When the difference between the input angle and the feedback angle is zero, the output angle contained in the up-down counter is equal to the synchro input angle.

The Function Generator performs the trigonometric computation: $\sin(\phi - \Theta) = \sin\phi\cos\Theta - \cos\phi\sin\Theta$.

Note that for small angles, $\sin(\phi - \Theta) \cong (\phi - \Theta)$. The equality given by the above equation is true only in the first quadrant, i.e., 0° to 90°. The analog inputs to the Function Generator have different values depending on the quadrant in which the input angle lies.

$\phi - \Theta$ is an analog representation of the error between ϕ the input angle, and Θ the output angle. This analog error is first demodulated then fed to an analog integrator whose output controls the frequency of a voltage-controlled oscillator (VCO). The VCO clocks the up-down counter. The up-down counter is functionally an integrator, therefore the tracking converter in itself is a closed-loop servo mechanism with two lags, making it a "Type II" servo loop. The "Type II" servo loop tracking converter exhibits no velocity errors and only minor acceleration errors.

Two-Speed Converter (See Figure 2)

The operation of a two-speed S/D converter is essentially the same as the single speed except there are two solid state CT's (SSCT) generating two error voltages. Assuming an off-null condition (the input angle does not equal the output angle), the crossover detector feeds the coarse (1X) SSCT error signal output to the demodulator. As the output angle Θ approaches the input angle ϕ the coarse SSCT output approaches a null. When the coarse SSCT output drops below a preset threshold, the crossover detector switches the fine (36X) SSCT error signal into the demodulator. The feedback angle Θ to the fine SSCT is multiplied by the speed ratio (in this case 36); the gradient of the fine SSCT then is 36X the coarse SSCT. The servo loop then is able to seek an even finer null. The converter will continue to use the fine error signal for continuous tracking. In order to eliminate false stable nulls of 180°, an angle offset produced by the Digital Adder and stickoff voltage (SO) is introduced into the coarse SSCT.

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ELECTRICAL SPECIFICATIONS

Parameter	Value
Resolution	16 bits (0.0055°)
Accuracy[1]	20 seconds 40 seconds (1:16) 1.1 minutes (1:8)
Speed Ratio	1:8, 1:16, 1:32, 1:36, 1:64
Allowable Synchro Misalignment[2]	±2 degrees ±1 degree (1:64)
Synchro Input Rates[3]	47 to 3000 Hz / 350 to 3000 Hz
Max Tracking Rate	250°/sec. / 1000°/sec.
Ka	4,500 sec^{-2} / 70,000 sec^{-2}
Power Supplies	
+11.5 to +16.5V	12mA max (7mA typ)
−11.5 to −16.5V	17mA max (9mA typ)
+4.75 to +5.25V	10mA max (3mA typ)
Digital Inputs/Outputs[4]	
Parallel binary angle	3-state positive logic 1 = MSB 16 = LSB
Enable M (ENM)	Logic 'O' enables 1-8 Logic '1' Hi-Z
Enable L (ENL)	Logic 'O' enables 9-16 Logic '1' Hi-Z
Inhibit (INH)	Logic 'O' latches output
Built in Test (BIT)	Logic 'O' = tracking Logic '1' = error
Converter Busy (CB)	3 us max positive pulse 7 us max (168T502)
Velocity Output	
Range	±10V for max tracking
Polarity	+ = increasing angle
Loading	10K ohms min
Synchro/Resolver Input[5][6]	
11.8V L-L	75K ohms min
90V L-L	600K ohms min
Reference Input[5][6]	
23 to 29Vrms	180K ohms min
103 to 127Vrms	800K ohms min
Temperature Ranges	
Operating	0° to 70° C
Storage	−55° to 125° C
Dimensions	3.12″ x 2.62″ x .4″
Weight	3.5 oz.

NOTES

(1) Accuracy applies for:
  (a) ±10% signal amplitude variations
  (b) 10% harmonic distortion in the reference
  (c) over power supply range
  (d) over operating temperature range

(2) With two-speed synchro converters, it is important to understand that the output of the fine synchro dominates in the determination of the coarse shaft angle despite any misalignment of the two synchros. No ambiguities will exist unless the allowable misalignment is exceeded.

(3) Higher tracking and acceleration rates available; consult factory.

(4) The Inhibit input is CMOS with a 51K ohm pull-up to +5V. Enable M and L are CMOS inputs with 51K ohm pull-down to ground. All digital outputs are TTL/CMOS compatable and can drive up to 2 TTL load equivalents.

(5) Other voltages available; consult factory.

(6) Inputs are solid state differential, any one stator and/or rotor line may be grounded. Common mode voltages up to specified L-L voltage have no effect on operation.

DIGITAL INPUTS/OUTPUTS

Digital outputs consist of 16 parallel data bits (1-16), a converter busy (CB), and a built-in test output (BIT).

The 16 bit parallel binary angle is outputted through 3-state transparent latches which can be enabled as one 16 bit word or two 8 bit bytes. By use of the Inhibit input, the 16 bit angle data can be latched without affecting the operation of the converter servo loop. Inputs ENM and ENL are the 3-state controls, when at logic '1' the parallel binary outputs are in the high impedance state, outputs are valid 0.5 microseconds after ENM or ENL are driven to logic 'O'.

The converter busy output (CB) is a positive pulse which brackets the parallel data code changes. Data is guaranteed valid at the trailing edge of the CB pulse.

The (BIT) logic output is a built-in test feature which indicates whenever the digital output is not tracking the synchro or resolver input within fine speed range. This is indicated by a logic '1' on the BIT output.

The Inhibit (INH) input locks the 16-bit transparent latch so that the data bits will remain stable while data is being transferred. If a CB pulse occurs after an INH has been applied, logic 'O', the 16-bit latch will remain locked and its data cannot change until INH is driven back to logic '1' and CB returns to logic 'O'. If an INH is applied during a CB pulse, the 16-bit latch will not lock until the CB pulse is over. Inhibit commands do not affect the updating of the converter no matter how long they are applied.

TIMING

Whenever an input angle change occurs, the converter changes the digital angle in steps of 1 LSB and generates a CB pulse. During the CB pulse, the data is changing and should not be transferred. The converter will ignore an INH command applied during a CB pulse. There are two methods of interfacing with a computer: (1) synchronously, and (2) asynchronously. A simple method of synchronous loading is to (a) apply the inhibit, (b) wait the equivalent of one CB pulse, (c) transfer data, and (d) release the inhibit. Asynchronous loading is accomplished by transferring data on the trailing edge of the CB pulse.

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DYNAMIC PERFORMANCE

The 168T500 series employs a Type II servo loop (Kv = ∞) and very high acceleration constants (Ka). The loop dynamics are completely independent of power supply variations over their specific ranges. As long as the maximum tracking rate is not exceeded there will be no velocity lag and only minor acceleration lags in the converter output.

The open loop transfer functions for both frequency options are given below:

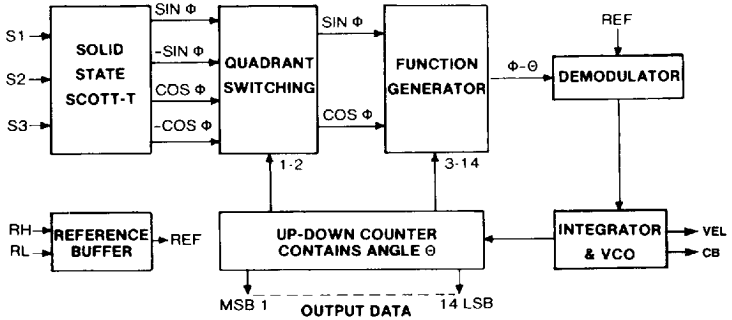
$$G_{60} = \frac{70^2\left(\frac{S}{50} + 1\right)}{S^2\left(\frac{S}{200} + 1\right)} \qquad G_{400} = \frac{266^2\left(\frac{S}{178} + 1\right)}{S^2\left(\frac{S}{666} + 1\right)}$$

ANALOG VELOCITY OUTPUT

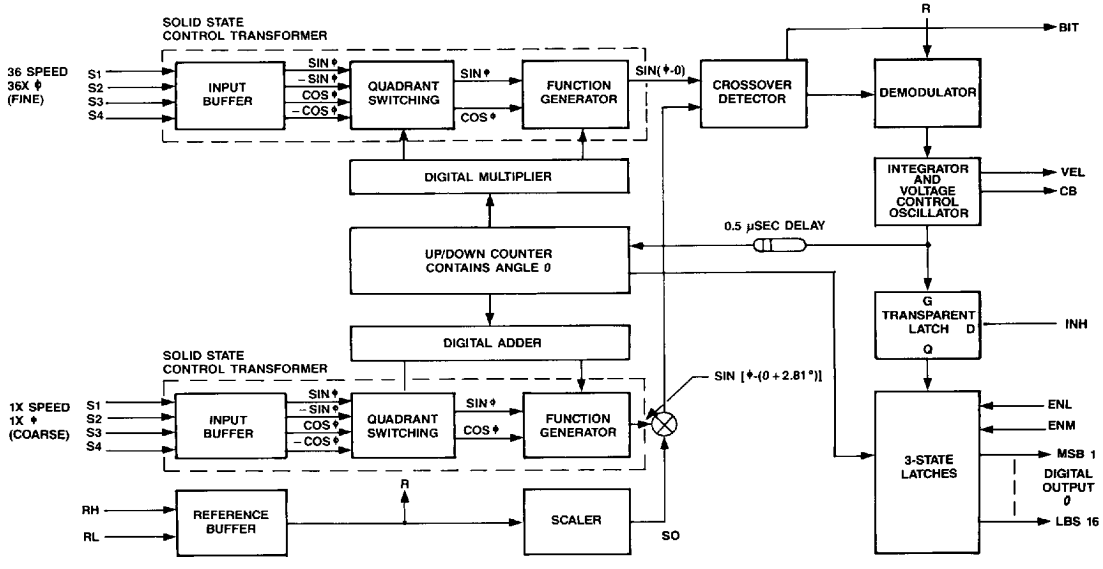
Velocity (VEL) is a DC voltage proportional to the angular velocity of the synchro or resolver shaft. Voltage polarity is positive for an increasing digital angle and negative for a decreasing digital angle. Other characteristics are listed in the specifications table.

BLOCK DIAGRAMS

SINGLE-SPEED CONVERTER BLOCK DIAGRAM
FIGURE 1



TWO-SPEED CONVERTER BLOCK DIAGRAM
FIGURE 2



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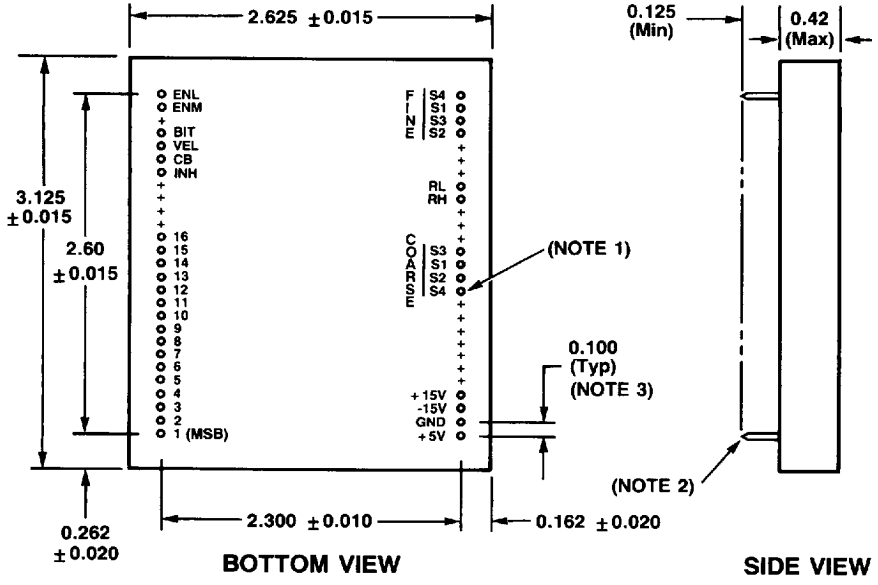
MECHANICAL OUTLINE



NOTES:

1. S4 pin appears on resolver input model only.
2. Rigid 0.025 diameter pins for solder-in or plug-in applications.
3. Noncumulative.
4. Dimensions are in inches.

BIT WEIGHT TABLE

Bit	Deg/Bit	Min/Bit
1 MSB	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	337.5
7	2.813	108.75
8	1.406	84.38
9	0.703	42.19
10	0.3516	21.09
11	0.1758	10.55
12	0.0879	5.27
13	0.0439	2.64
14	0.0220	1.32
15	0.0110	0.66
16	0.0055	0.33

ORDERING INFORMATION

168T Suffix	Input Type	Stator Voltage	Reference Voltage	Frequency	Speed Ratio
500	Synchro	11.8V	26V	400 Hz	1:36
501	Synchro	90V	115V	400 Hz	1:36
502	Synchro	90V	115V	60 Hz	1:36
503	Resolver	11.8V	26V	400 Hz	1:36

NOTES:

1. Standard temperature range 0° to 70°C.
2. To order other speed ratios add ratio suffix to part number, i.e., 168T500-16.

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