

# NP100N055PUK

## MOS FIELD EFFECT TRANSISTOR

R07DS0589EJ0100 Rev.1.00 Dec 12, 2011

## **Description**

The NP100N055PUK is N-channel MOS Field Effect Transistor designed for high current switching applications.

#### **Features**

• Super low on-state resistance

 $R_{DS(on)} = 3.25 \text{ m}\Omega \text{ MAX.} (V_{GS} = 10 \text{ V}, I_D = 50 \text{ A})$ 

- Low  $C_{iss}$ :  $C_{iss} = 4900 \text{ pF TYP.} (V_{DS} = 25 \text{ V})$
- Designed for automotive application and AEC-Q101 qualified

## **Ordering Information**

Part No.	Lead Plating	Pac	Package	
NP100N055PUK-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP100N055PUK-E2-AY *1			Taping (E2 type)	

Note: \*1 Pb-free (This product does not contain Pb in the external electrode)

## **Absolute Maximum Ratings** $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	55	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	±100	А
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±400	А
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T1</sub>	176	W
Total Power Dissipation (T <sub>A</sub> = 25°C)	P <sub>T2</sub>	1.8	W
Channel Temperature	T <sub>ch</sub>	175	°C
Storage Temperature	T <sub>stg</sub>	-55 to 175	°C
Repetitive Avalanche Current *2	I <sub>AR</sub>	38	A
Repetitive Avalanche Energy *2	E <sub>AR</sub>	144	mJ

Notes: \*1  $\,T_{C}$  = 25°C,  $P_{W} \leq$  10  $\mu s,\, Duty\,\, Cycle \leq$  1%

## **Thermal Resistance**

<sup>\*2</sup> R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V

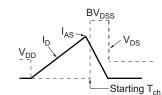
## **Electrical Characteristics** (T<sub>A</sub> = 25°C)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	_	_	1	μΑ	$V_{DS} = 55 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
Forward Transfer Admittance *1	y <sub>fs</sub>	40	80	_	S	$V_{DS} = 5 \text{ V}, I_{D} = 50 \text{ A}$
Drain to Source On-state Resistance *1	R <sub>DS(on)</sub>	_	2.70	3.25	mΩ	$V_{GS} = 10 \text{ V}, I_{D} = 50 \text{ A}$
Input Capacitance	C <sub>iss</sub>	_	4900	7350	pF	V <sub>DS</sub> = 25 V
Output Capacitance	Coss	_	500	750	pF	$V_{GS} = 0 V$
Reverse Transfer Capacitance	C <sub>rss</sub>	_	180	330	pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>	_	28	70	ns	$V_{DD} = 28 \text{ V}, I_D = 50 \text{ A}$
Rise Time	t <sub>r</sub>	_	12	30	ns	$V_{GS} = 10 \text{ V}$
Turn-off Delay Time	t <sub>d(off)</sub>	_	70	140	ns	$R_G = 0 \Omega$
Fall Time	t <sub>f</sub>	_	7	20	ns	
Total Gate Charge	$Q_G$	_	80	120	nC	V <sub>DD</sub> = 44 V
Gate to Source Charge	Q <sub>GS</sub>	_	21	_	nC	V <sub>GS</sub> = 10 V
Gate to Drain Charge	$Q_{GD}$	_	20	_	nC	I <sub>D</sub> = 100 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$	_	0.9	1.5	V	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>	_	52	_	ns	I <sub>F</sub> = 100 A, V <sub>GS</sub> = 0 V
Reverse Recovery Charge	Q <sub>rr</sub>	_	95	_	nC	di/dt = 100 A/μs

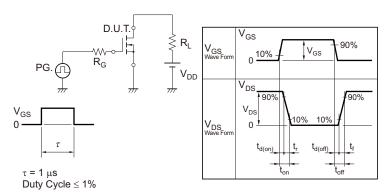
Note: \*1 Pulsed test

## **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $V_{GS} = 20 \rightarrow 0 \text{ V}$ $V_{GS} = \frac{25 \Omega}{M}$ $V_{DD}$ $V_{DD}$ $V_{DD}$



## **TEST CIRCUIT 2 SWITCHING TIME**



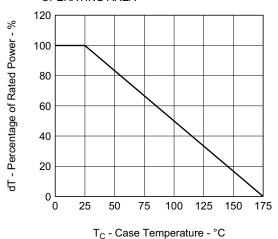
## **TEST CIRCUIT 3 GATE CHARGE**

$$\begin{array}{c|c} D.U.T. \\ \hline I_G = 2 \text{ mA} \\ \hline WV \\ \hline \end{array}$$

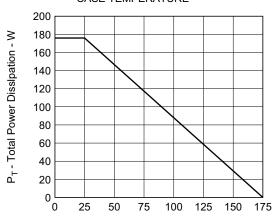
$$\begin{array}{c|c} PG. \\ \hline \end{array} \begin{array}{c} S \\ S \\ O \\ \end{array} \begin{array}{c} D.U.T. \\ \hline \end{array}$$

## **Typical Characteristics** $(T_A = 25^{\circ}C)$

# DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

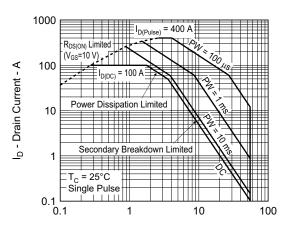


# TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



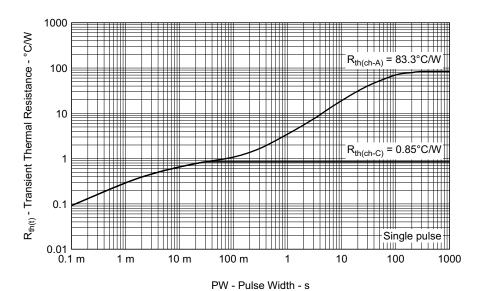
T<sub>C</sub> - Case Temperature - °C

#### FORWARD BIAS SAFE OPERATING AREA

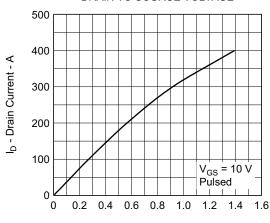


 $V_{DS}$  - Drain to Source Voltage - V

#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

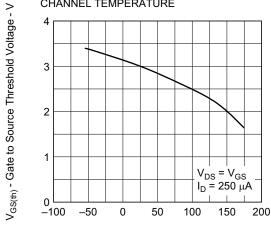


# DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



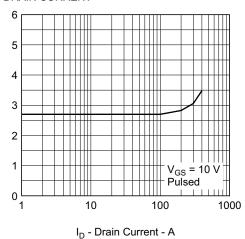
# GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

V<sub>DS</sub> - Drain to Source Voltage - V

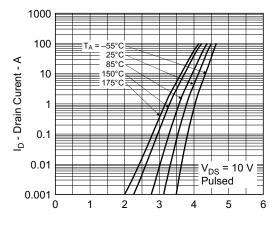


T<sub>ch</sub> - Channel Temperature - °C

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

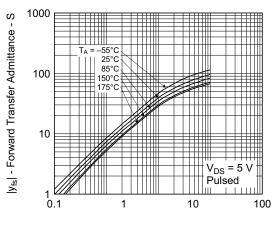


#### FORWARD TRANSFER CHARACTERISTICS



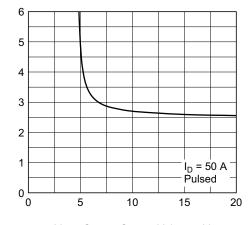
V<sub>GS</sub> - Gate to Source Voltage - V

# FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



I<sub>D</sub> - Drain Current - A

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



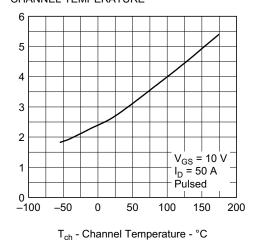
V<sub>GS</sub> - Gate to Source Voltage - V

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

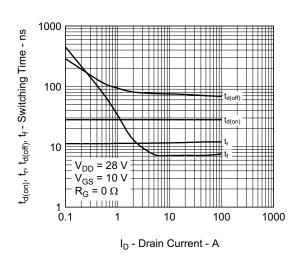
 $R_{\text{DS(on)}}$  - Drain to Source On-State Resistance -  $m\Omega$ 

 $R_{DS(on)}$  - Drain to Source On-State Resistance -  $m\Omega$ 

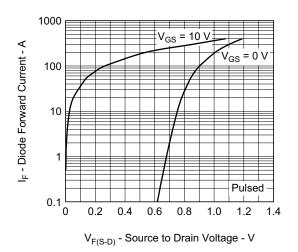
# DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



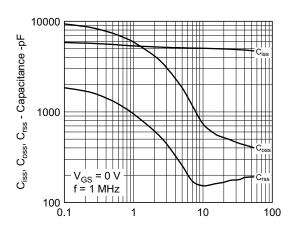
## SWITCHING CHARACTERISTICS



#### SOURCE TO DRAIN DIODE FORWARD VOLTAGE

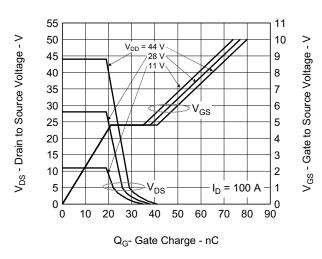


#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

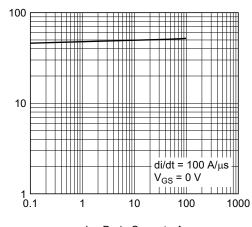


V<sub>DS</sub> - Drain to Source Voltage - V

#### DYNAMIC INPUT/OUTPUT CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT

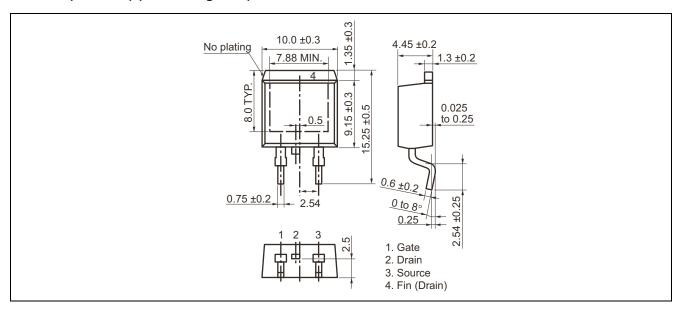


I<sub>F</sub> - Drain Current - A

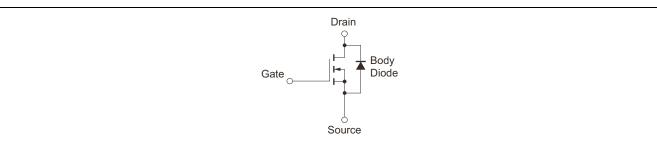
t<sub>rr</sub> - Reverse Recovery Time - ns

## Package Drawing (Unit: mm)

## TO-263 (MP-25ZP) (Mass: 1.5 g TYP.)



## **Equivalent Circuit**



Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

**Revision History** 

## NP100N055PUK Data Sheet

		Description		
Rev.	Date	Page	Summary	
1.00	Dec 12, 2011	_	First Edition Issued	

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