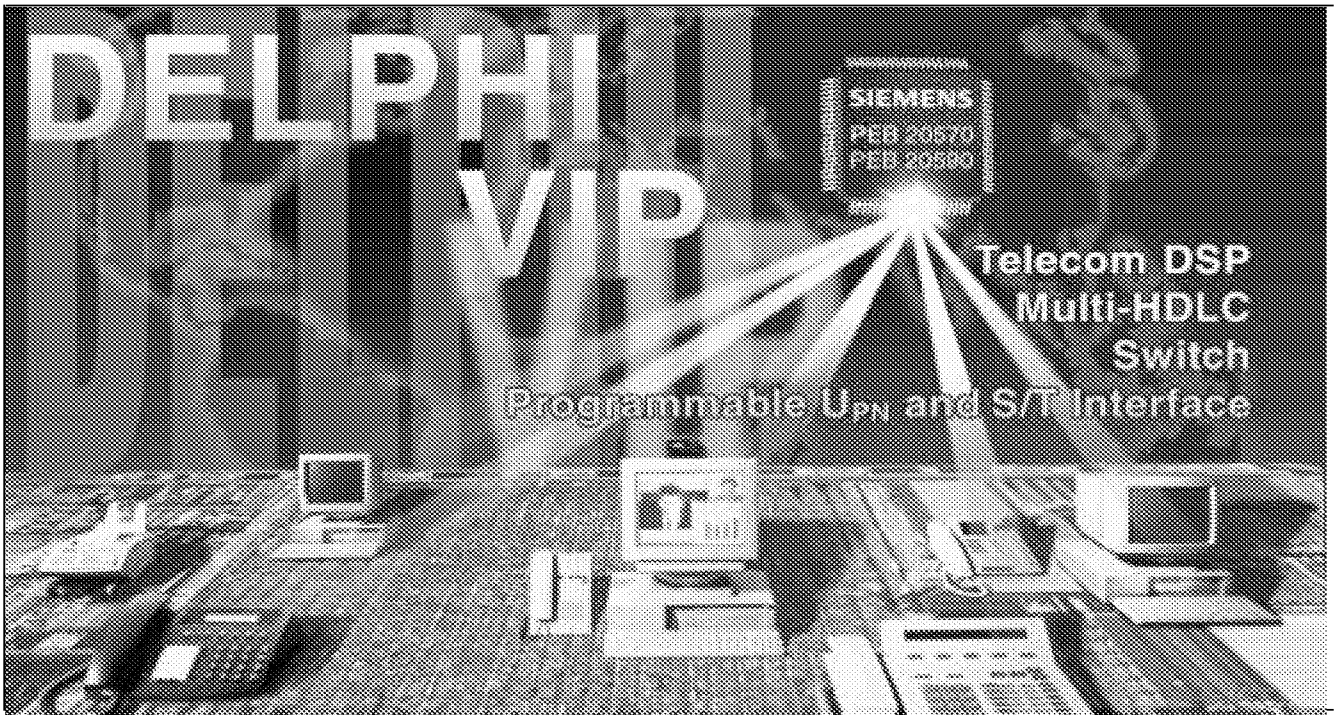# SIEMENS

ICs for Communications

Telecom DSP Concept

DSP Embedded Line Ports Controller with HDLC Integration
DELPHI
PEB 20570/PEB 20571 Version 1.1

Versatile Interface Port
VIP
PEB 20590 Version 1.1

Preliminary Product Overview   11.98

DS 4

PEB 20570 PEB 20571 PRELIMINARY Revision History:		Current Version: 11.98
Previous Version:		11.97
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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1 Overview

The DELPHI and VIP chipset is a most flexible and optimized solution for telecom applications like digital linecards in PBX and Central Office systems or central controllers in small and midsize PBX systems.

DELPHI will be available in three dedicated versions (further versions being prepared):

- **DELPHI-LC PEB 20570** is a linecard controller providing switching, multiple HDLC and layer-1 control for up to three VIPs (24 ISDN channels). Other transceiver ICs (32 analog or 16 digital channels) may additionally be connected via IOM-2/GCI interface.
- **DELPHI-PB PEB 20571** additionally provides a programmable DSP including program and data RAM. This allows the user to implement dedicated PBX software like DTMF and tone generation and detection, conferencing, and modem emulation.
- **DELPHI-HD PEB 20572** (in definition) includes up to 64 time slot oriented HDLC controllers, and 4 independent serial communication controllers. Additional transfer and signalling protocols such as async and SS7 will be provided in DSP software.

The system software design for DELPHI-PB is eased by a complete portfolio of DSP programming and simulation tools and a reference board (refer to **chapter 3**).

DELPHI is software compatible to DOC PEB 20560.

The following table shows an overview of the main differences of the DELPHI derivatives:

Table 1 DELPHI Product Family

	DELPHI-LC	DELPHI-PB	DELPHI-HD[1]
Applications	Linecards (U_{PN},S/T)	Small PBXs	HDLC Controller
DSP User MIPS	-	available [2]	available [2]
DSP User Program RAM	-	available [2]	available [2]
DSP User Data RAM	-	available [2]	available [2]
HDLC Controllers (16 / 64 kbit/s)	32	16	64
Serial Communication Channels	1	1	4
IOM-2/GCI/PCM Ports	2 x 32 TS	1 x 32 TS	2 x 32 TS
PCM Ports	4 x 32 TS	1 x 32 TS	2 x 32 TS
N° of VIPs on IOM-2000	3	1	-
N° of ISDN Channels	40	16	-
N° of Analog Channels	32	16	-
DMA Interface	available	available	available

1) DELPHI version in definition. More information on request.
2) The DSP memory sizes and MIPS performance available for the user in this DELPHI version depend on the system configuration (e.g. number of layer-1 ports connected to the DELPHI, data rates, size of switching matrix, signaling traffic etc.)

VIP PEB 20590 is a flexible transceiver compoment, programmable to U_{PN} and S/T mode. It provides up to eight layer-1 subscriber or trunk lines. The VIP is programmed by the DELPHI via the IOM-2000 interface.

VIP's eight channels are programmable in the following maximum partition between U_{PN} and S/T channels:

	Max. number of U_{PN} and S/T Channels								
U_{PN}	8	7	6	5	4	3	2	1	0
S/T	0	1	2	3	4	4	4	4	4

Note: Up to 3 VIP can be connected to one DELPHI.
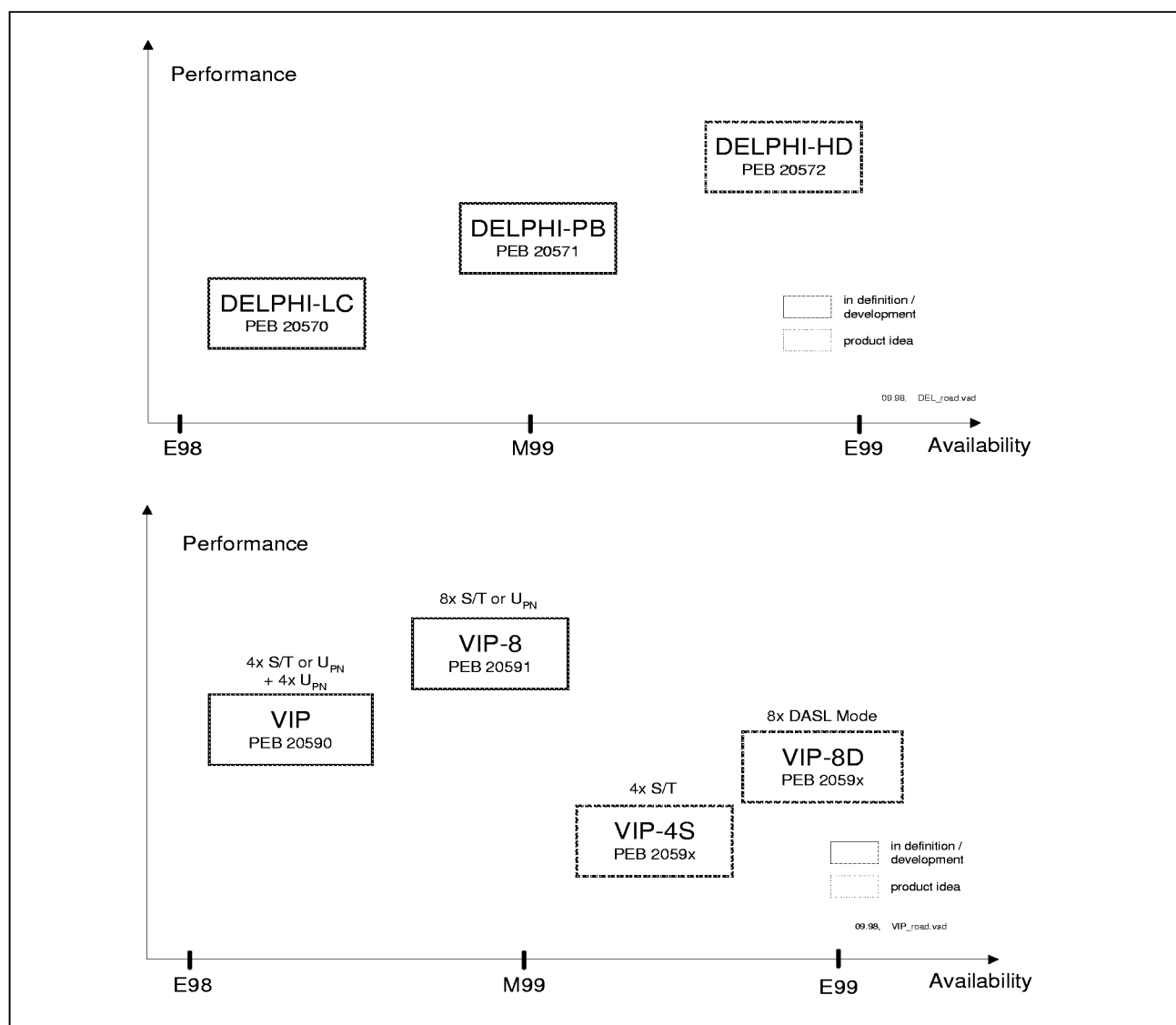
Roadmap of DELPHI and VIP

SIEMENS

DELPHI-LC (Linecard version)   **PEB 20570**
DELPHI-PB (PBX version)   **PEB 20571**

**Version 1.1**   **CMOS**

1.1 DELPHI-LC Key Features

DELPHI-LC is optimized for linecard applications:

- Three VIPs supporting up to 24 ISDN channels, connected via IOM-2000 interface
- Two IOM-2 (GCI) ports (configurable as PCM ports) supporting up to 16 ISDN channels or 32 analog subscribers
- Four PCM ports with up to 4 x 2.048 Mbit/s (4 x 32 TS) or 2 x 4.096 Mbit/s or 1 x 8.192 Mbit/s
- Switching matrix 160 x 128 TS
- 32 HDLC controllers assignable to any D- or B-channel (at 16 kbit/s or 64 kbit/s)
- Serial communication controller: high-speed signaling channel of up to 16.384 Mbit/s
- Standard multiplexed and de-multiplexed µP interface: Siemens, Intel, Motorola
- Dedicated DMA support mailbox
- Programmable PLL based Master/Slave clock generator, providing all system clocks from a single 16.384 MHz crystal source
- JTAG compliant test interface; single 3.3 V power supply

P-TQFP-100-1
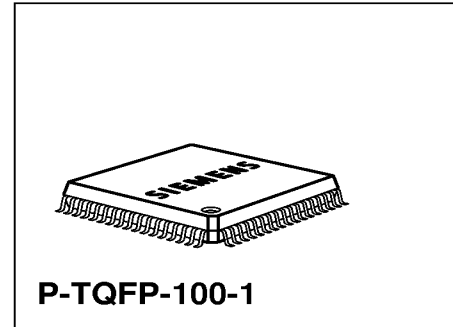
1.2 DELPHI-PB Key Features (additionally to DELPHI-LC)

DELPHI-PB is optimized for small PBX applications:

- User programmable DSP core OAK+ (up to 60 MIPS, depending on application)
- On-chip user program and data memory
- Complete DSP tooling package (including evaluation board) provided
- PBX demo-software available (e.g., tone/DTMF generation and recognition, conferencing, modem emulation)
- DSP work load measurement for run-time statistics
- Serial DSP program debugging interface connected via JTAG port
- a-/µ-law conversion for all B-channels

Note: DELPHI-PB is software compatible to DOC PEB 20560

Type	Package
PEB 20570 / PEB 20571	P-TQFP-100-1

SIEMENS

**Versatile Interface Port**   **PEB 20590**
VIP

Version 1.1   **CMOS**

1.3 VIP Key Features

VIP is a very flexible ISDN transceiver device:

- Eight 2B+D interfaces with full duplex transceivers, up to four S/T or eight U_{PN} (2-wire) interfaces
- S/T interfaces according to ITU-T I.430 compatible to QUAT-S PEB 2084
- U_{PN} interfaces compatible to OCTAT-P PEB 2096
- Receive timing recovery via on-chip PLL
- Adaptive line amplifiers with peak detectors, central biasing, and oversampling control
- Execution of analog test loops
- Conversion between pseudo-ternary AMI code and binary code
- Frame alignment in trunk applications with maximum wander correction of 25 µs
- Programmable selection of reference clock sources in trunk applications
- IOM-2000 interface for connecting up to three VIPs to DELPHI
- JTAG compliant test interface; 3.3 V power supply
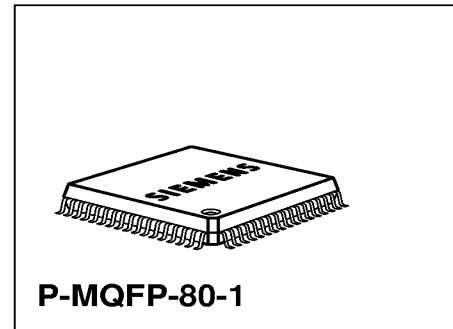
P-MQFP-80-1

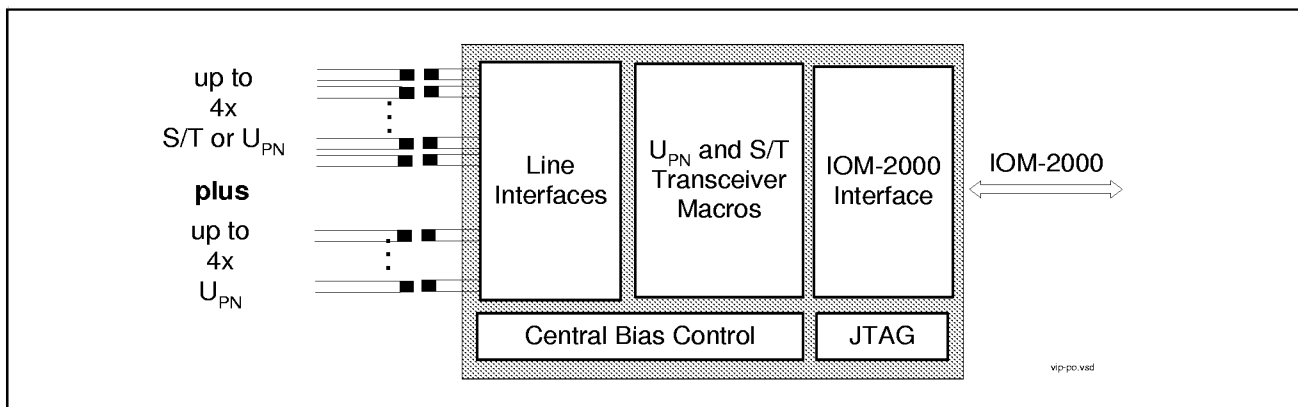*Note: U_{PN} refers to a version of the U_{P0} interface with reduced loop length (up to 1.3 km)*

Figure 1   VIP Functional Blocks Overview

Type	Package
PEB 20590	P-MQFP-80-1

1.4 Typical Applications

1.4.1 DELPHI-LC in Linecard Applications

In the following application examples, the DELPHI-LC operates as linecard controller performing layer-1 handling, switching and signaling control:

- Up to 24 U_{PN} or 12 S/T channels via IOM-2000 (three VIPs as layer-1 interface)
- Up to 16 ISDN channels via IOM-2/GCI (standard ISDN transceivers)
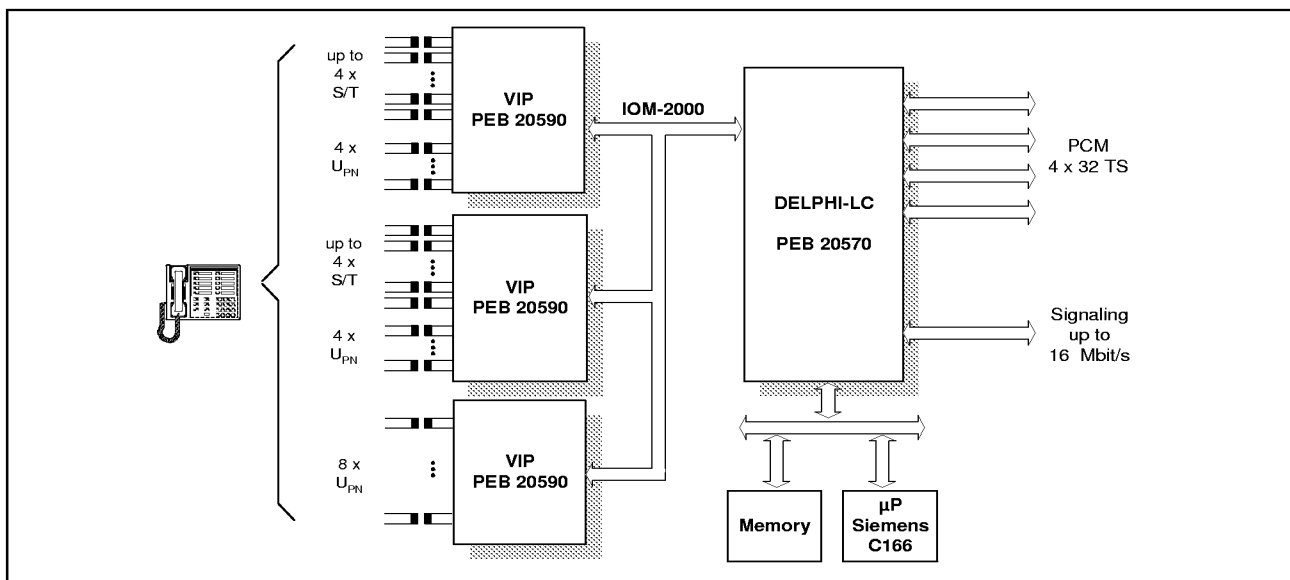- Up to 32 analog channels via IOM-2/GCI (standard analog transceivers)

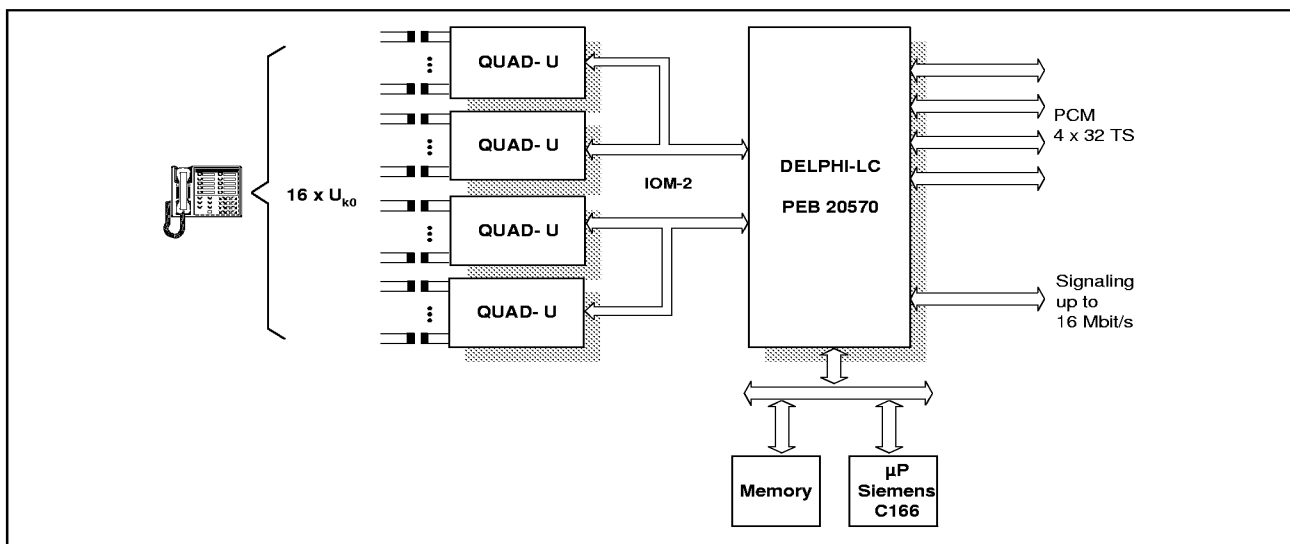**Figure 2   DELPHI-LC and VIP in a Mixed Line Card (e.g., 8x S/T and 16x U_{PN})**

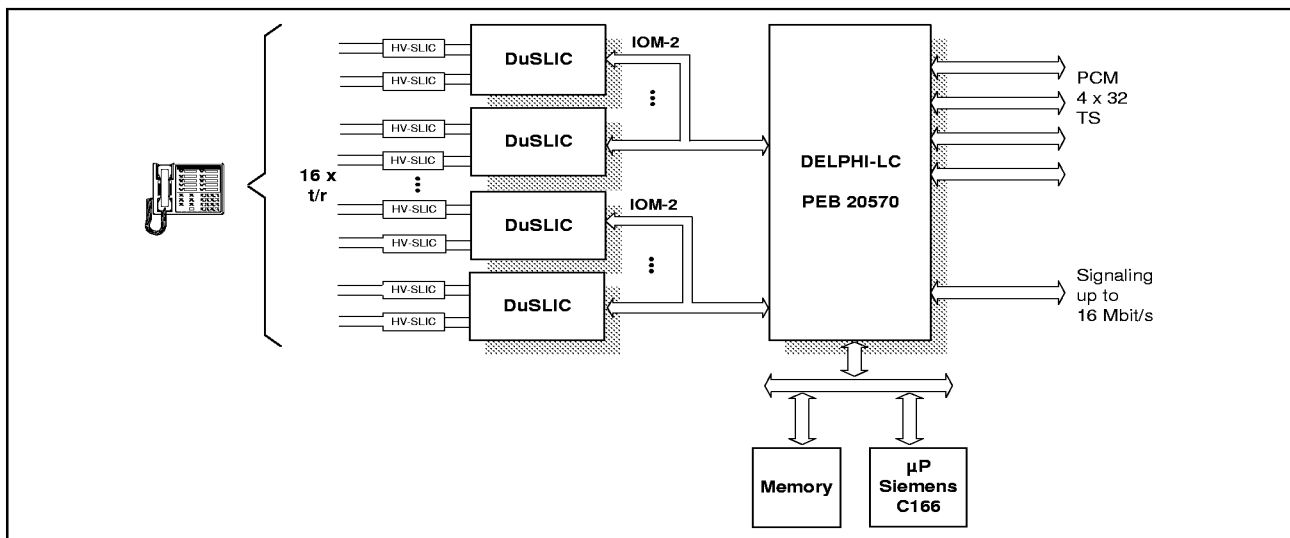**Figure 3   DELPHI-LC in an U_{k0} Line Card for 16 Subscribers**

Figure 4   DELPHI-LC in an Analog Line Card for 16 t/r Subscribers

1.4.2   DELPHI-PB and VIP in Small PBX Applications

In the following example, the DELPHI-PB operates as central controller in a small PBX key system, performing layer-1 handling, switching, and signaling control. User specific PBX software (e.g. tone/DTMF generation or recognition, conferencing) can be developed and implemented efficiently on the integrated DSP core.

The VIP connects the digital subscribers or trunk line. Analog lines are connected via IOM-2/GCI interface.
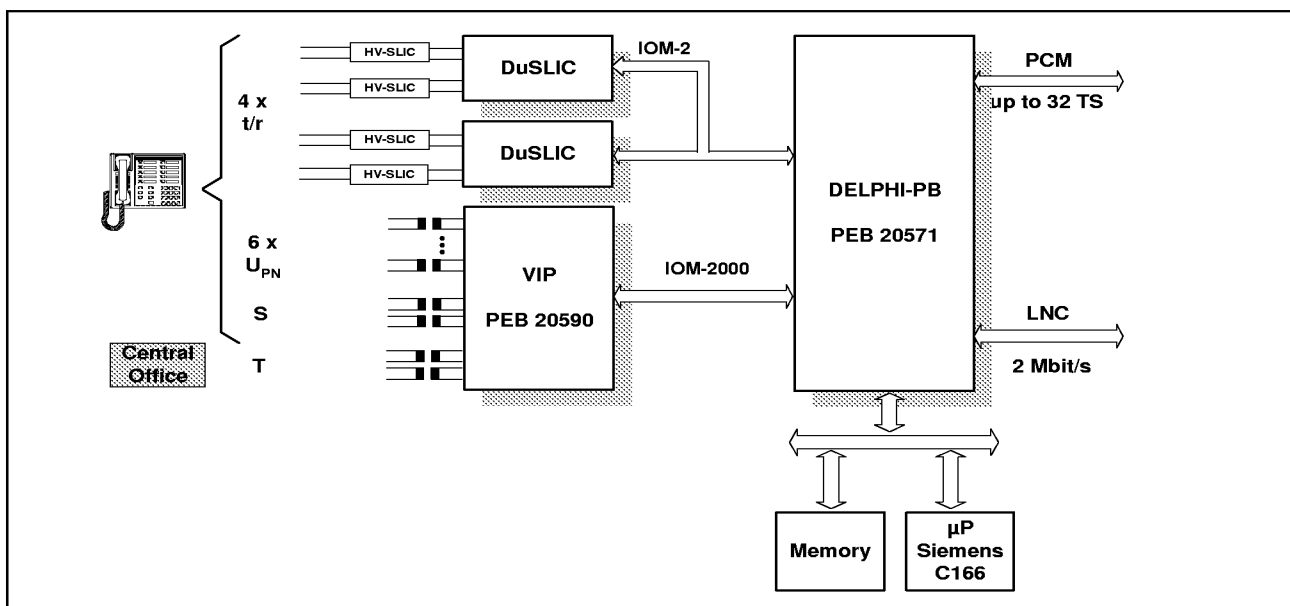

Figure 5   DELPHI-PB and VIP in a Small PBX Application

2 DELPHI Functional Blocks Overview

2.1 DELPHI-LC and VIP Logic Symbols

The following figure shows as an example the connection between DELPHI-LC and one VIP, and the interfaces of both devices with the associated number of pins.
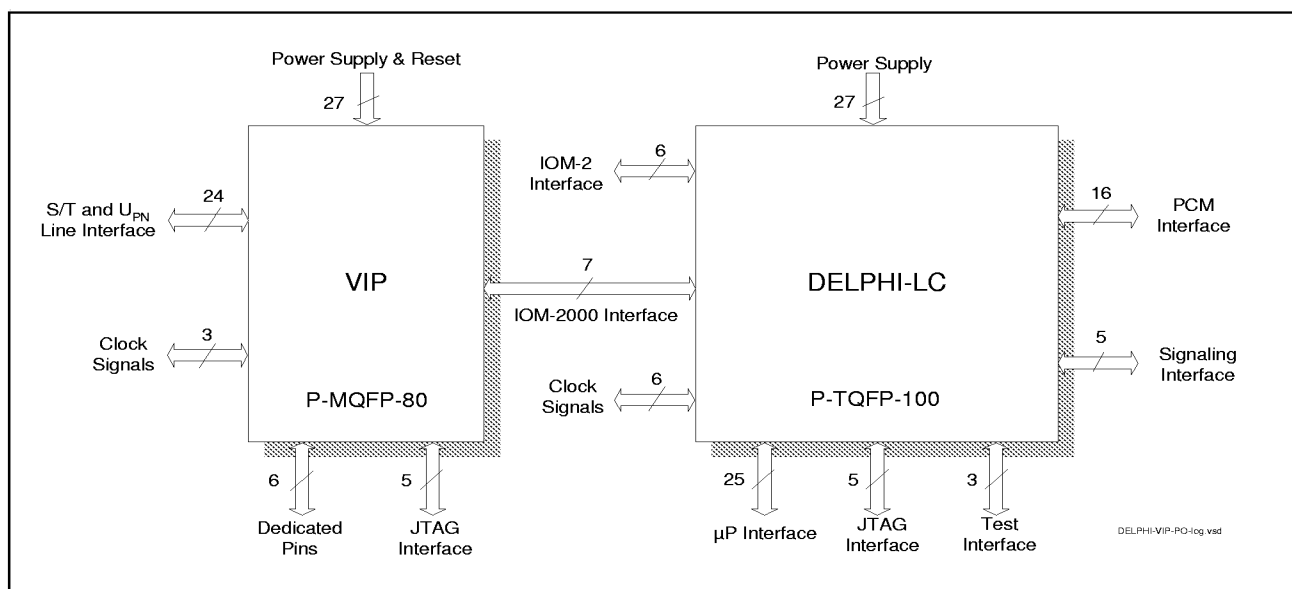

Figure 6   Logic Symbols DELPHI-LC and VIP

2.2 DELPHI Functional Blocks Overview

The next figure compares the block diagrams of DELPHI-LC and DELPHI-PB.
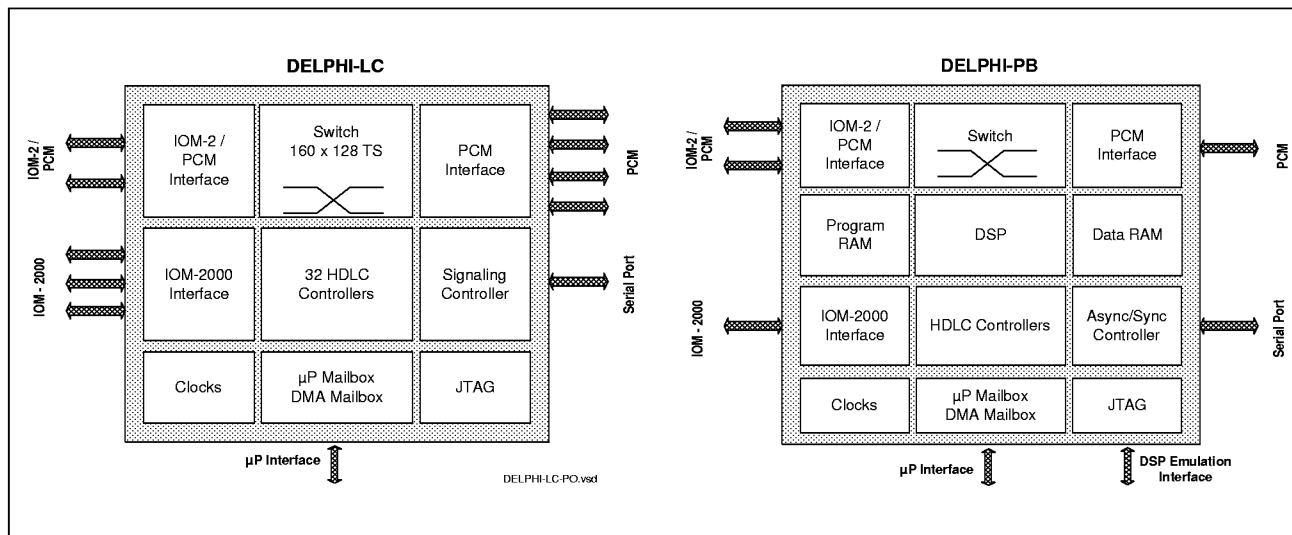

Figure 7   DELPHI-LC and DELPHI-PB Functional Block Diagram

2.3 IOM®-2 Interface

• Two ports providing 16 IOM-2 channels (up to 16 ISDN or 32 analog channels)
• Data rates: 1x 4.096 Mbit/s, 2x 2.048 Mbit/s, 1x 768 kbit/s or 1x 384 kbit/s
• Programmable tri-state control (resolution depending on data rate)
• Support of QUAT-S PEB 2084 D-channel blocking in trunk mode

2.4 IOM-2000 Interface

• Connection of up to 3 VIPs (each providing 8 channels) to the DELPHI:
  – Up to 24 layer-1 U_{PN} channels, of which 12 channels are also programmable to S/T
• Data handling:
  – B-channel data scrambling/descrambling for U_{PN} interface
  – D-channel data collision handling
  – Multiframe handling
• Maintenance channel handling
• Control of Command and Status exchange with VIP(s)

2.5 PCM Interface

• Four ports providing 32 time slots (8-bit) each
• Data rates: 4x 2.048 Mbit/s, 2x 4.096 Mbit/s, 1x 8.192 Mbit/s
• Connection of several DELPHIs via PCM highway (Master and Slave clock capable)
• Tri-state control lines

2.6 Switching Matrix

• Matrix of 160 x 128 8-bit time slots
• Connections between any time slot on IOM-2, IOM-2000 or PCM interface
• Switching with constant delay of two 8 kHz frames for any connection
• Sub-channel switching using 4-bit, 2-bit or 1-bit resolution

2.7 HDLC Controllers

Up to 32 independent HDLC controllers are assignable to any D-channel on IOM-2 interface or IOM-2000 interface (16 kbit/s) or to any B-channel on IOM-2 interface, IOM-2000 interface or PCM interface (64 kbit/s).

HDLC Protocol Support

• Bit stuffing
• Flag/Idle/Abort generation and recognition
• CRC-16 check and generation
• Inter-frame flags or '1s'
• Abort transmission upon collision

2.8 General Purpose Signaling Controller

The general purpose HDLC controller provides a serial communication channel with a data rate of up to 16.384 Mbit/s.

Overview of Features

- 64-byte buffer for receive and 64-byte for transmit direction
- Collision detection/resolution mechanism
- $\overline{\text{CTS}}$ and $\overline{\text{RTS}}$ Handshake lines
- Three operational modes:
  a) Automatic response generation for RR- and I-frames like in ELIC PEB 20550
  b) Extended transparent mode without any HDLC framing
  c) Async mode (software protocol, DELPHI-PB only)

HDLC Protocol Support

- Bit stuffing
- Flag/Idle/Abort generation and recognition
- Inter-frame 'flags' or '1s'
- CRC-16/32 check and generation

2.9 DSP Core OAK+

The DELPHI-PB integrates a user programmable DSP core OAK$^+$ providing up to 60 MIPS. For example, the user can implement dedicated PBX software such as DTMF/tone generation and recognition, conferencing and modem emulation.

The architecture, optimized for high performance and low dissipation, includes:

- Seven instruction groups providing 72 instructions (including bit manipulation)
- Two data busses (X and Y) each with de-multiplexed 16-bit address and data bus
- Computation Unit (CU), Bit Manipulation Unit (BMU), Data Addressing Arithmetic Unit (DAAU), Program Control Unit (PCU)

2.10 µP Interface and Mailbox

The microprocessor interface provides the following modes (compatible to standard processors like Siemens C16x, Motorola 68xxx, Intel 80x86):

- Multiplexed and de-multiplexed bus mode
- DMA support for a dedicated DMA mailbox

The communication with external devices is done via two bi-directional mailboxes:

- General mailbox, accessed by the µP and by the DSP
- DMA mailbox, accessed by a DMA controller and by the DSP

Both mailboxes may also be combined into one double-sized general mailbox. Note that the mailbox protocol syntax is determined by the user.

2.11   Clock Generator

The Master/Slave clock generator provides all clocks for the DELPHI and connected devices.
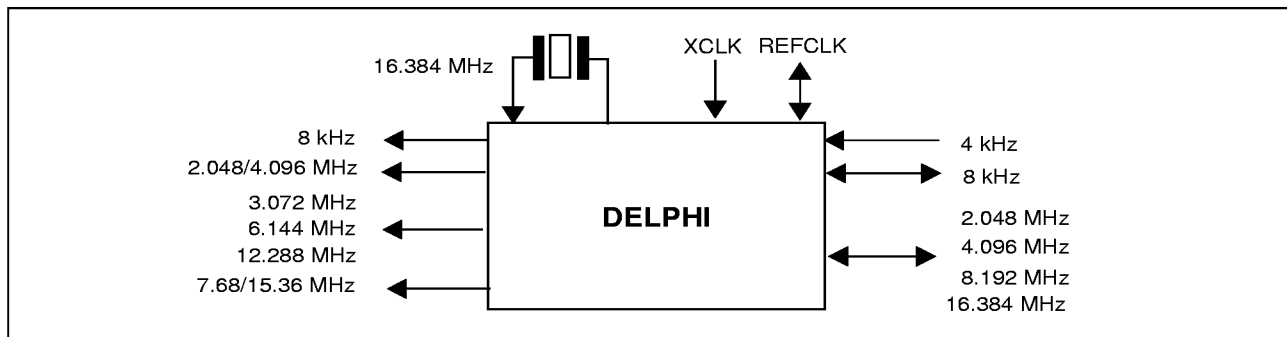

Figure 8   DELPHI System Clocks

All clocks are generated by two on-chip PLLs from a 16.384 MHz external crystal clock.

3   DSP Tool Support for DELPHI

The DELPHI-PB provides a freely programmable OAK$^+$ DSP core. The user can incorporate in his software design the complete set of DSP tools as described below.

3.1   On-chip Emulation

The DELPHI-PB is equipped with an on-chip emulation module (OCEM). It allows to detect bugs in the application software in early design stage. It interprets functions such as Start, Abort, Reset, Step, Read, Write, and also performs instruction and data break points, program flow trace buffering and breakpoint-on-event at operation cycle speed without additional off-chip hardware.

3.2   DELPHI-PB Development / Evaluation Board

Siemens provides evaluation boards to allow quick design start with the DELPHI-PB, supporting software design and testing the interfaces. PBX demo software (DTMF/tone generation and recognition, conferencing, etc.) is included in the package. All µP and DSP registers are accessible for debugging via serial interfaces on the DELPHI board.

DELPHI-PB is DSP software compatible to Siemens' DOC PBX controller (PEB 20560).

3.3   DELPHI Software Configurator

The DELPHI software configurator is a MS-Windows system to develop DSP software. It generates application specific DSP code based on a library of optimized DSP software modules. It helps the user to include only the desired functionality in the DSP code, thus optimizing MIPS and memory usage. No knowledge on DSP programming is required to efficiently create application software. An executable DSP program is directly obtained.

3.4 DSP Macro Assembler

The macro assembler translates DSP assembly language source files into DSP machine language object files. It consists of a macro preprocessor which checks DSP programming restrictions and prepares the object for full symbolic debugging. It contains C-like operators and conventions for an easy design of code and data structures.

The object files generated are compatible to the Common Object File Format (COFF). The Object Format Converter translates the COFF file into an Intel hex file format, which can be downloaded to any EPROM programming tool.

3.5 Linker/Locator

The very flexible and modular linker/locator combines object files generated by the COFF macro assembler into a single executable COFF object file. It performs relocation by mapping to the target systems memory map. It supports user defined memory classes and enables locating segments to absolute or relative locations (also overlaying).

3.6 C Compiler

The C cross compiler is a state-of-the-art compiler providing 2 options for generating efficient DSP object code:

1. to mix object files generated by the compiler with those generated by the assembler directly from efficient hand coded assembly instructions,
2. to use DSP specific C language extensions.

3.7 Simulator

The simulator simulates the operation of the DSP for program verification and debugging purposes. It simulates the entire DSP instruction set and accepts executable COFF object code generated from the linker/locator. The simulator allows verification and monitoring of the DSP states without the requirement of the DSP hardware. To simulate external signals or hardware logic, it is possible to connect DOS files and integrate C functions using the Dynamic Link Library (DLL) mechanism of MS-Windows. During program execution, the internal registers and memory of the simulated DSP are modified as each instruction is interpreted by the host. Execution is suspended when a breakpoint is encountered or when the user halts execution. Then the DSP internal registers and both program and data memory can be looked at and modified.

3.8 Emulator

The emulator is based on the same surface and features as the simulator, but is connected over a PC plug-in card to the JTAG port of the DELPHI-PB. This allows to test the COFF file in real time on the target hardware environment. This tool also enables testing and debugging in the field.