USB97C210

USB 2.0 Flash Media Controller

Datasheet

Product Features

- Complete USB Specification 2.0 Compatibility
  - Includes USB 2.0 Transceiver
  - A Bi-directional Control and a Bi-directional Bulk Endpoint are provided.
- Complete System Solution for interfacing CompactFlash™ (CF), SmartMedia™ (SM), Memory Stick™ (MS), and Secure Digital (SD) and MultiMediaCard™ (MMC) devices to USB 2.0 bus*
  - Supports USB Bulk Only Mass Storage Compliant Bootable BIOS
  - Support for the following devices:
  - CompactFlash
  - SmartMedia
  - XD Card
  - Memory Stick, Memory Stick Pro, HS Memory Stick
  - Secure Digital
  - MultiMediaCard
  - NAND Flash drive
  - CF form factor ATA hard drives
  - Support for simultaneous operation of all above devices. (only one at a time of each of the following groups supported: CF or ATA drive, SM or XD or NAND, SD or MMC)
  - Enhanced CF support to allow true sequential read operations to improve throughput
- 16 GPIOs for special function use: LED indicators, button inputs, power control to memory devices, etc.
  - Inputs capable of generating interrupts with either edge sensitivity
  - One GPIO has automatic 1 sec toggle capability for flashing an LED indicator.
- 8051 8 bit microprocessor
  - Provides low speed control functions
  - 30 Mhz execution speed at 4 cycles per instruction average
  - 12K Bytes of internal SRAM for general purpose scratchpad
  - 768 Bytes of internal SRAM for general purpose scratchpad or program execution while re-flashing external ROM
- Double Buffered Bulk Endpoint
  - Bi-directional 512 Byte Buffer for Bulk Endpoint
  - 64 Byte RX Control Endpoint Buffer
  - 64 Byte TX Control Endpoint Buffer
- External Program Memory Interface
  - 64K Byte Code Space
  - Flash, SRAM, or EPROM Memory
- On Board 12Mhz Crystal Driver Circuit
- Internal PLL for 480Mhz USB2.0 Sampling, 30Mhz MCU clock
- Supports firmware upgrade via USB bus if “boot block” Flash program memory is used
- 2.5 Volt, Low Power Core Operation
- 3.3 Volt I/O with 5V input tolerance
- 128 Pin TQFP (1.0 mm height package) or QFP Package

ORDERING INFORMATION

Order Number(s):

USB97C210-NE for 128 pin TQFP package

USB97C210-NC for 128 pin QFP package

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USB97C210 Datasheet Revision History

REV LEVEL AND DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.5 11/05/03	Table 6.1 - DC Electrical Characteristics, pg. 19	Updated High Input Leakage units.
Rev. 1.4 06/02/03	Chapter 1 - General Description, pg. 5	Updated disclaimer.
Rev. 1.3 03/28/03	Features, pg. 1	Revised features under sub bullet “Support for the following devices”
Rev. 1.3 03/28/03	Chapter 1 - General Description, pg. 5	Revised first, second and fourth paragraph.
Rev. 1.2 07/09/02	Table 5.1 - Pin Descriptions, pg. 13	Changed values of RBIAS and FS-/+ resistors
Rev. 1.2 07/09/02	Table 6.1 - DC Electrical Characteristics, pg. 19	Updated power supply currents to reflect actual performance
Rev. 1.2 07/09/02	Chapter 8 - Typical Application, pg. 24	Updated figure to minimize standby current

References

1. SmartMedia Electrical Specification Version 1.30
2. SmartMedia Physical Format Specifications Version 1.30
3. SmartMedia Logical Format Specifications Version 1.20
4. SMIL (SmartMedia Interface Library) Software Edition Version 1.00, Toshiba Corporation, 01, July, 2000
5. SMIL (SmartMedia Interface Library) Hardware Edition Version 1.00, Toshiba Corporation, 01, July, 2000
6. MultiMediaCard System Specification Version 2.2
7. SD Memory Card Specifications, Part 1, Physical Layer Specification Version 1.0, March 2000, SD Group
8. Memory Stick Standard Excerption from Format Specification v1.3, July, 2000, Sony Corporation.
9. CompactFlash Specification Rev 1.4
10. CF+ & CF Specification Rev. ATA-5 Draft 0.2
11. Universal Serial Bus Specification Rev 2.0

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List of Tables

Chapter 1 General Description

The USB97C210 is a USB2.0 Bulk Only Mass Storage Class Peripheral Controller intended for supporting CompactFlash (CF) in True IDE Mode only, SmartMedia (SM/XD), Memory Stick (MS/MSPro), Secure Digital (SD) and MultiMediaCard (MMC) flash memory devices. It provides a single chip solution for the most popular flash memory cards in the market.*

The device consists of a USB 2.0 PHY and SIE, buffers, Fast 8051 microprocessor with expanded scratchpad, and program SRAM, and CF, MS, SM and SD controllers. The SD controller supports both SD and MMC devices. The Memory Stick controller supports MS, HS MS and MSPro. The CF controller supports CF and CF form factor ATA drives. The Smart Media controller supports SM, XD, and single NAND flash devices.*

- Provisions for external Flash Memory up to 64K bytes for program storage is provided.
- 12K bytes of scratchpad SRAM and 768Bytes of program SRAM are also provided.

Sixteen GPIO pins are for the 128-pin device. Provisions are made to allow hot swap of flash media to be implemented.

The USB97C210 supports the insertion one each of all 4 major types of cards (CF, SM/XD/Nand, MS/MSPro, MMC/SD) simultaneously.

SMSC provides the following object code software free of charge with purchase of the USB97C210**:

- Multiple LUN Mass Storage Class compliant firmware to support all media types in a single code image, with option for firmware download via USB if a sector erasable program memory is used.
- Windows application for programming VID/PID/OEM strings, and unique serial number into serial EEPROM via USB. Serial EEPROM may be eliminated entirely if appropriate firmware and specific Flash device is used for program code.
- Firmware with field upgrade capability via USB (requires specific 128KB Flash for firmware storage).

Source code licenses are also available for USB97C210 customers.**

SMSC may make complete internal specifications available for those customers requiring programming information, subject to SMSC's applicable Proprietary Information Agreement (nondisclosure agreement). Contact your SMSC sales representative for more information.

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Chapter 2 Pin Table

2.1 By Interface

CompactFlash Interface (28 Pins)			
CF_D0	CF_D1	CF_D2	CF_D3
CF_D4	CF_D5	CF_D6	CF_D7
CF_D8	CF_D9	CF_D10	CF_D11
CF_D12	CF_D13	CF_D14	CF_D15
CF_nIOR	CF_nIOW	CF_IRQ	CF_nRESET
CF_IORDY	CF_nCS0	CF_nCS1	CF_SA0
CF_SA1	CF_SA2	CF_nCD1	CF_nCD2
SmartMedia Interface (17 Pins)			
SM_D0	SM_D1	SM_D2	SM_D3
SM_D4	SM_D5	SM_D6	SM_D7
SM_ALE	SM_CLE	SM_nRE	SM_nWE
SM_nWP	SM_nB/R	SM_nCE	SM_nCD
SM_nWPS			
Memory Stick Interface (4 Pins)			
MS_BS	MS_SDIO	MS_SCLK	MS_INS
SD Interface (7 Pins)			
SD_CMD	SD_CLK	SD_DAT0	SD_DAT1
SD_DAT2	SD_DAT3	SD_nWP	
USB Interface (7 Pins)			
USB+	USB-	LOOPFLTR	RBIAS
RTERM	FS+	FS-	
Memory/IO Interface (29 Pins)			
MA0	MA1	MA2	MA3
MA4	MA5	MA6	MA7
MA8	MA9	MA10	MA11
MA12	MA13	MA14	MA15
MD0	MD1	MD2	MD3
MD4	MD5	MD6	MD7
nMRD	nMWR	nMCE	
nIOW	nIOR		
Misc (21 Pins)			
GPIO0/RXD	GPIO1/TXD	GPIO2/T0	GPIO3/nWE
GPIO4	GPIO5	GPIO6	GPIO7
XTAL1/CLKIN	XTAL2	nRESET	
GPIO8	GPIO9	GPIO10	GPIO11
GPIO12	GPIO13	GPIO14	GPIO15
nTEST0	nTEST1		
Power, Grounds (15 Pins)			
Total 128			

2.2 Pin Numbers

Table 2.1 - 128 Pin VTQFP

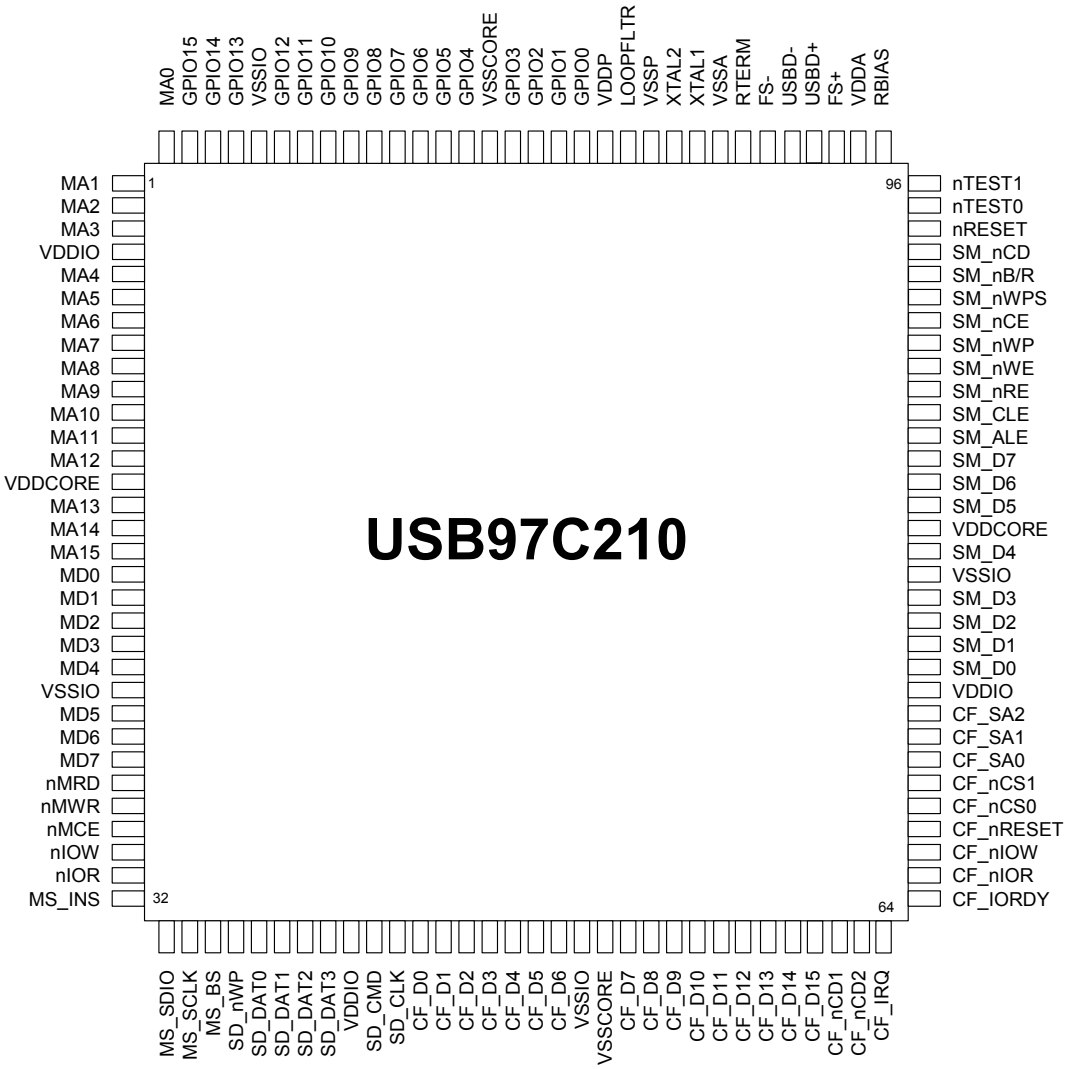
PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
1	MA1	8	33	MS_SDIO	8	65	CF_IORDY	-	97	RBIAS	
2	MA2	8	34	MS_SCLK	8	66	CF_nIOR	8	98	*VDDA*	
3	MA3	8	35	MS_BS	8	67	CF_nIOW	8	99	FS+	
4	*VDDIO*		36	SD_nWP	8	68	CF_nRESET	8	100	USB+	
5	MA4	8	37	SD_DAT0	8	69	CF_nCS0	8	101	USB-	
6	MA5	8	38	SD_DAT1	8	70	CF_nCS1	8	102	FS-	
7	MA6	8	39	SD_DAT2	8	71	CF_SA0	8	103	RTERM	
8	MA7	8	40	SD_DAT3	8	72	CF_SA1	8	104	VSSA	
9	MA8	8	41	*VDDIO*		73	CF_SA2	8	105	XTAL1	
10	MA9	8	42	SD_CMD	8	74	*VDDIO*		106	XTAL2	
11	MA10	8	43	SD_CLK	8	75	SM_D0	8	107	VSSP	
12	MA11	8	44	CF_D0	8	76	SM_D1	8	108	LOOPFLTR	
13	MA12	8	45	CF_D1	8	77	SM_D2	8	109	VDDP	
14	*VDDCORE*		46	CF_D2	8	78	SM_D3	8	110	GPIO0	8
15	MA13	8	47	CF_D3	8	79	*VSSIO*		111	GPIO1	8
16	MA14	8	48	CF_D4	8	80	SM_D4	8	112	GPIO2	8
17	MA15	8	49	CF_D5	8	81	*VDDCORE*	8	113	GPIO3	8
18	MD0	8	50	CF_D6	8	82	SM_D5	8	114	*VSSCORE*	
19	MD1	8	51	*VSSIO*		83	SM_D6		115	GPIO4	8
20	MD2	8	52	*VSSCORE*		84	SM_D7	8	116	GPIO5	8
21	MD3	8	53	CF_D7	8	85	SM_ALE	8	117	GPIO6	8
22	MD4	8	54	CF_D8	8	86	SM_CLE	8	118	GPIO7	8
23	*VSSIO*		55	CF_D9	8	87	SM_nRE	8	119	GPIO8	8
24	MD5	8	56	CF_D10	8	88	SM_nWE	8	120	GPIO9	8
25	MD6	8	57	CF_D11	8	89	SM_nWP	8	121	GPIO10	8
26	MD7	8	58	CF_D12	8	90	SM_nCE	8	122	GPIO11	8
27	nMRD	8	59	CF_D13	8	91	SM_nWPS	-	123	GPIO12	8
28	nMWR	8	60	CF_D14	8	92	SM_nB/R	-	124	*VSSIO*	
29	nMCE	8	61	CF_D15	8	93	SM_nCD	-	125	GPIO13	8
30	nIOW	8	62	CF_nCD1	-	94	nRESET	-	126	GPIO14	8
31	nIOR	8	63	CF_nCD2	-	95	nTEST0	-	127	GPIO15	8
32	MS_INS	-	64	CF_IRQ	-	96	nTEST1	-	128	MA0	8

Table 2.2 - 128 Pin QFP

PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA	PIN #	NAME	MA
4	MA1	8	36	MS_SDIO	8	68	CF_IORDY	-	100	RBIAS	
5	MA2	8	37	MS_SCLK	8	69	CF_nIOR	8	101	*VDDA*	
6	MA3	8	38	MS_BS	8	70	CF_nIOW	8	102	FS+	
7	*VDDIO*		39	SD_nWP	8	71	CF_nRESET	8	103	USB+	
8	MA4	8	40	SD_DAT0	8	72	CF_nCS0	8	104	USB-	
9	MA5	8	41	SD_DAT1	8	73	CF_nCS1	8	105	FS-	
10	MA6	8	42	SD_DAT2	8	74	CF_SA0	8	106	RTERM	
11	MA7	8	43	SD_DAT3	8	75	CF_SA1	8	107	VSSA	
12	MA8	8	44	*VDDIO*		76	CF_SA2	8	108	XTAL1	
13	MA9	8	45	SD_CMD	8	77	*VDDIO*		109	XTAL2	
14	MA10	8	46	SD_CLK	8	78	SM_D0	8	110	VSSP	
15	MA11	8	47	CF_D0	8	79	SM_D1	8	111	LOOPFLTR	
16	MA12	8	48	CF_D1	8	80	SM_D2	8	112	VDDP	
17	*VDDCORE*		49	CF_D2	8	81	SM_D3	8	113	GPIO0	8
18	MA13	8	50	CF_D3	8	82	*VSSIO*		114	GPIO1	8
19	MA14	8	51	CF_D4	8	83	SM_D4	8	115	GPIO2	8
20	MA15	8	52	CF_D5	8	84	*VDDCORE*		116	GPIO3	8
21	MD0	8	53	CF_D6	8	85	SM_D5	8	117	*VSSCORE*	
22	MD1	8	54	*VSSIO*		86	SM_D6	8	118	GPIO4	8
23	MD2	8	55	*VSSCORE*		87	SM_D7	8	119	GPIO5	8
24	MD3	8	56	CF_D7	8	88	SM_ALE	8	120	GPIO6	8
25	MD4	8	57	CF_D8	8	89	SM_CLE	8	121	GPIO7	8
26	*VSSIO*		58	CF_D9	8	90	SM_nRE	8	122	GPIO8	8
27	MD5	8	59	CF_D10	8	91	SM_nWE	8	123	GPIO9	8
28	MD6	8	60	CF_D11	8	92	SM_nWP	8	124	GPIO10	8
29	MD7	8	61	CF_D12	8	93	SM_nCE	8	125	GPIO11	8
30	nMRD	8	62	CF_D13	8	94	SM_nWPS	-	126	GPIO12	8
31	nMWR	8	63	CF_D14	8	95	SM_nB/R	-	127	*VSSIO*	
32	nMCE	8	64	CF_D15	8	96	SM_nCD	-	128	GPIO13	8
33	nIOW	8	65	CF_nCD1	-	97	nRESET	-	1	GPIO14	8
34	nIOR	8	66	CF_nCD2	-	98	nTEST0	-	2	GPIO15	8
35	MS_INS	-	67	CF_IRQ	-	99	nTEST1	-	3	MA0	8

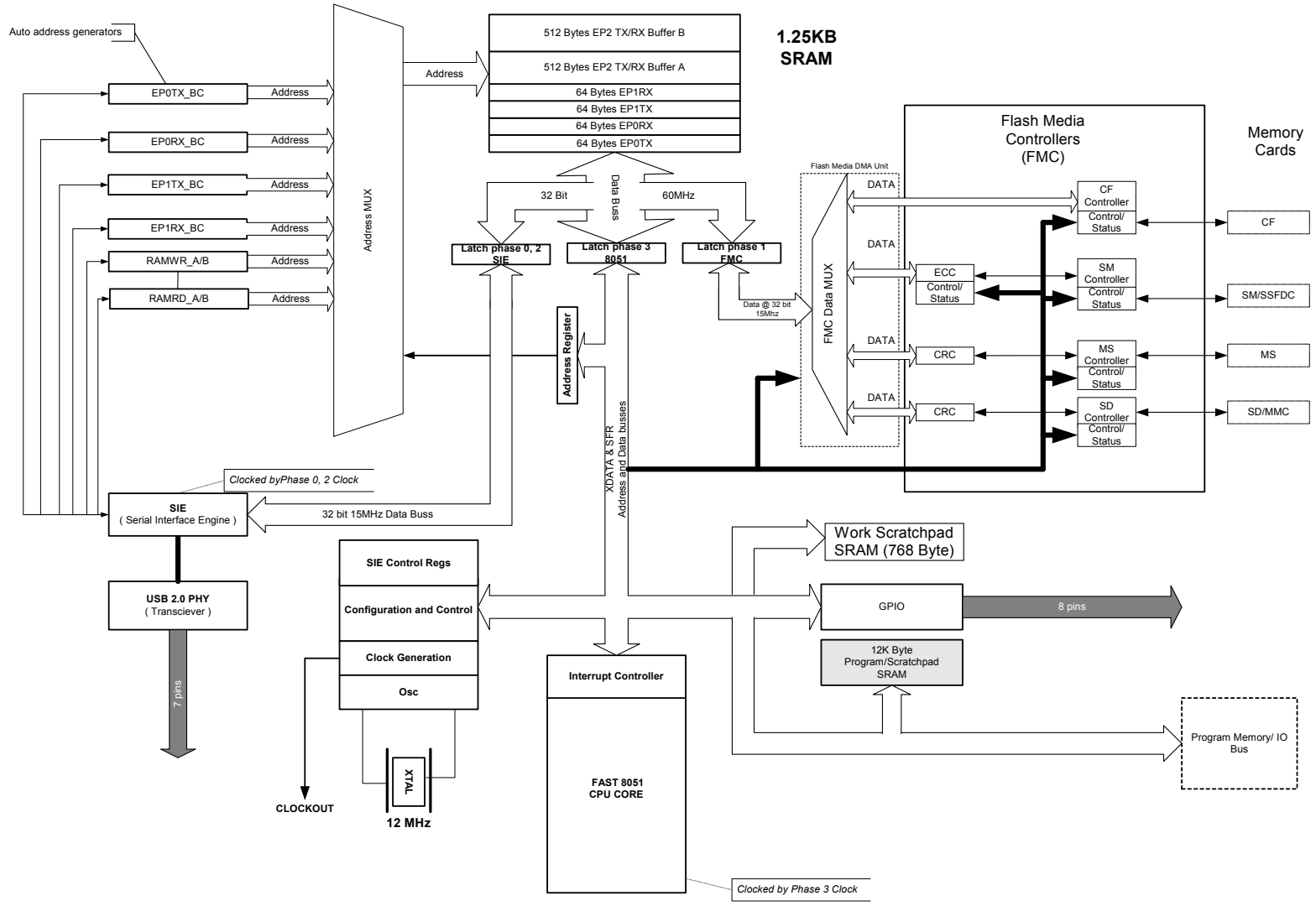
Chapter 3 Pin Configurations

3.1 128 Pin VTQFP



3.2 128 Pin QFP

Chapter 4 Block Diagram



Chapter 5 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The “n” symbol in the signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When “n” is not present before the signal name, the signal is asserted when at the high voltage level.

The terms assertion and negation are used exclusively. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term assert, or assertion indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term negate, or negation indicates that a signal is inactive.

Table 5.1 - Pin Descriptions

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
CompactFlash (In True IDE mode) Interface			
CF Chip Select 1	CF_nCS1	O8	This pin is the active low chip select 1 signal for the CF ATA device
CF Chip Select 0	CF_nCS0	O8	This pin is the active low chip select 0 signal for the task file registers of CF ATA device in the True IDE mode.
CF Register Address 2	CF_SA2	O8	This pin is the register select address bit 2 for the CF ATA device.
CF Register Address 1	CF_SA1	O8	Address signal 1 for the task file registers, when the CFC is enabled in True IDE mode
CF Register Address 0	CF_SA0	O8	Address signal 0 for the task file registers, when the CFC is enabled in True IDE mode.
CF Interrupt	CF_IRQ	IPD	This is the active high interrupt request signal from the CF device. This pin *has* an internal weak pull-down resistor.
CF Data 15-8	CF_D[15:8]	IO8	The bi-directional data signals CF_D15-CF_D8 in True IDE mode data transfer, when the CFC is enabled. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. *These pins have an internal weak pull-down resistor.*
CF Data7-0	CF_D[7:0]	IO8	The bi-directional data signals CF_D7-CF_D0 in the True IDE mode data transfer. In the True IDE Mode, all of task file register operation occur on the CF_D[7:0], while the data transfer is on CF_D[15:0]. *These pins have an internal weak pull-down resistor.*
IO Ready	CF_IORDY	IPU	This pin is active high input signal with an internal weak pull-up resistor.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
CF Card Detection2	CF_nCD2	IPU	This card detection pin is connected to the ground on the CF device, when the CF device is inserted. This pin has an internal weak pull-up resistor.
CF Card Detection1	CF_nCD1	IPU	This card detection pin is connected to ground on the CF device, when the CF device is inserted. This pin has an internal weak pull-up resistor.
CF Hardware Reset	CF_nRESET	O8	This pin is an active low hardware reset signal to CF device.
CF IO Read	CF_nIOR	O8	This pin is an active low read strobe signal for CF device, when the CFC is enabled.
CF IO Write Strobe	CF_nIOW	O8	This pin is an active low write strobe signal for CF device, when the CFC is enabled.
SmartMedia Interface			
SM Write Protect	SM_nWP	O8	This pin is an active low write protect signal for the SM device, when the SMC is enabled.
SM Address Strobe	SM_ALE	O8	This pin is an active high Address Latch Enable signal for the SM device, when the SMC is enabled
SM Command Strobe	SM_CLE	O8	This pin is an active high Command Latch Enable signal for the SM device, when the SMC is enabled.
SM Data7-0	SM_D[7:0]	IO8	These pins are the bi-directional data signal SM_D7-SM_D0, when the SMC is enabled. The bi-directional input signal should have an internal weak pull-up resister on the input.
SM Read Enable	SM_nRE	O8	This pin is an active low read strobe signal for SM device, when SMC is enabled.
SM Write Enable	SM_nWE	O8	This pin is an active low write strobe signal for SM device, when SMC is enabled.
SM Write Protect Switch	SM_nWPS	IPU	A write-protect seal is detected, when this pin is low. This pin has an internal weak pull-up resistor.
SM Busy or Data Reday	SM_nB/R	IPU	This pin is connected to the BSY/RDY pin of the SM device. This pin has an internal weak pull-up resistor.
SM Chip Enable	SM_nCE	O8	This pin is the active low chip enable signal to the SM device. This pin has an internal weak pull-up resistor.
SM Card Detection	SM_nCD	IPU	This is the card detection signal from SM device to indicate if the device is inserted. This pin has internal weak pull-up resistor.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
Memory Stick Interface			
MS Bus State	MS_BS	O8	For detailed information on the function of these pins, please consult the Sony Memory Stick specifications.
MS System Data In/Out	MS_SDIO	IO8	
MS Card Insertion	MS_INS	IPU	
MS System CLK	MS_SCLK	O8	

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
SD Interface			
SD Data3-0	SD_DAT[3:0]	IO8	For detailed information on the function of these pins, please consult the SD Memory Card Specifications.
SD Clock	SD_CLK	O8	
SD Command	SD_CMD	IO8	
SD Write Protected	SD_nWP	IPU	
USB Interface			
USB Bus Data	USB- USB+	IO-U	These pins connect to the USB bus data signals.
USB Transceiver Filter	LOOPFLTR		This pin provides the ability to supplement the internal filtering of the transceiver with an external network, if required. This pin is normally not connected.
USB Transceiver Bias	RBIAS		A precision 10.0K resistor is attached from ground to this pin to set the transceiver's internal bias currents.
Termination Resistor	RTERM		A precision 1.5K resistor is attached to this pin from a 3.3V supply.
Full Speed USB Data	FS- FS+	IO-U	These pins connect to the USB- and USB+ pins through 39.2 ohm series resistors.
Memory/IO Interface			
Memory Data Bus	MD[7:0]	IO8	These signals are used to transfer data between the internal CPU and the external program memory.
Memory Address Bus	MA[15:0]	O8	These signals address memory locations within the external memory. *Memory access time should be 80 ns or less.*
Memory *Write* Strobe	nMWR	O8	Program Memory Write; active low
Memory Read Strobe	nMRD	O8	Program Memory Read; active low. *Memory output enable time (assuming this signal is used for this memory function) must be 80 ns or less.*
Memory Chip Enable	nMCE	O8	Program Memory Chip Enable; active low. This signal shall be deasserted, when the USB97C210 is in power down mode (USB SUSPEND).
I/O Read Strobe	nIOR	O8	This is an active low I/O Read strobe signal of MD bus.
I/O Write Strobe	nIOW.	O8	This is an active low I/O Write strobe signal of MD bus.
Misc			
Crystal Input/External Clock Input	XTAL1/ CLKIN	ICLKx	12Mhz Crystal or external clock input. This pin can be connected to one terminal of the crystal or can be connected to an external 12Mhz clock when a crystal is not used.
Crystal Output	XTAL2	OCLKx	12Mhz Crystal This is the other terminal of the crystal, or left open when an external clock source is used to drive XTAL1/CLKIN. It may not be used to drive any external circuitry other than the crystal circuit.

NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
General Purpose I/O	GPIO0 /RXD	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output. In addition to the above, this port has the capability of auto-toggling at a 1 Hz rate when used as an output. As an input, the GPIO0 can also be used as input to the RXD of a UART in the device for firmware debug purposes. *Note: This pin defaults as an input and should be terminated to a supply via a high value resistor to avoid a floating input condition.*
General Purpose I/O	GPIO1 /TXD	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output. In addition, as an output, the GPIO1 can also be used as an output TXD of a UART in the device for firmware debug purposes. *Note: This pin defaults as an input and should be terminated to a supply via a high value resistor to avoid a floating input condition.*
General Purpose I/O	GPIO2 /T0	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output. In addition, the pin can be used as the internal 8051 “T0 timer P3.4” output. *Note: This pin defaults as an input and should be terminated to a supply via a high value resistor to avoid a floating input condition.*
General Purpose I/O	GPIO3 /nWE	I/O8	This pin may be used either as input, edge sensitive interrupt input, or output. In addition, the output can be nWE, for use with PCMCIA form factor flash cards with “true IDE” capability. *Note: This pin defaults as an input and should be terminated to a supply via a high value resistor to avoid a floating input condition.*
General Purpose I/O	GPIO[7:4]	I/O8	This pin may be used either as input, edge sensitive interrupt output, or output.
General Purpose I/O	GPIO[15:8]	I/O8	These pins may be used either as input, or output.
RESET input	nRESET	IS	This active low signal is used by the system to reset the chip. The active low pulse must be at least 100ns wide.
TEST Input	nTEST[0:1]	I	These signals are used for testing the chip. User should normally leave them unconnected.

POWER, GROUNDS, and NO CONNECTS			
	VDD		+2.5V Core power
	VDDIO		+3.3V I/O power
	VDDP		+2.5 Analog power
	VSSP		Analog Ground Reference
	VDDA		+3.3V Analog power
	VSSA		Analog Ground Reference
	GND		Ground Reference

5.1 Buffer Type Descriptions

Table 5.2 - USB97C210 Buffer Type Descriptions

BUFFER	DESCRIPTION
I	Input
IPU	Input with internal weak pull-up resistor.
IPD	Input with internal weak pull-down resistor.
IS	Input with Schmitt trigger
I/O4	Input/Output with 4mA drive
I/OD4	Input/Open drain output … 4mA sink
I/O8	Input/Output with 8mA drive
I/OD8	Input/Open drain output … 8mA sink
O4	Output with 4mA drive
O8	Output with 8mA drive
I/O12	Output with 12mA drive
O12	Output with 12mA drive
OD12	Open drain….12mA sink
ICLKx	XTAL clock input
OCLKx	XTAL clock output
I/O-U	Defined in USB specification

Chapter 6 DC Parameters

6.1 Maximum Guaranteed Ratings

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin, with respect to Ground 5.5V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum $V_{DD,}$ V_{DDP} ..... +3.0V
Maximum $V_{DDIO,}$ V_{DDA} ..... +4.0V

*Stresses above the specified parameters could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. When this possibility exists, it is suggested that a clamp circuit be used.

Table 6.1 - DC Electrical Characteristics

(T_A = 0°C - 70°C, $V_{DDIO,}V_{DA}$ = *+3.3 V* ± 10%, $V_{DD,}$ V_{DDP} = *+2.5 V* ± 10%,)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
ICLK Input Buffer						
Low Input Level	V_{ILCK}			0.4	V	
High Input Level	V_{IHCK}	2.2			V	
Input Leakage (All I and IS buffers)						
Low Input Leakage	I_{IL}	-10		+10	uA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	uA	V_{IN} = V_{DDIO}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	uA	V_{IN} = 0 to V_{DDIO} (**Note 1**)
I/O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8 mA @ V_{DDIO} = 3.3V
HIGH OUTPUT LEVEL	V_{OH}	2.4			V	I_{OH} = -4 mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (**Note 1**)
I/O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (**Note 1**)
I/O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA @ V_{DDIO} = 3.3V
High Output Level	V_{OH}	2.4			V	I_{OH} = -12 mA @ V_{DDIO} = 3.3V
Output Leakage	I_{OL}	-10		+10	µA	V_{IN} = 0 to V_{DDIO} (**Note 1**)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
IO-U (**Note 2**)						
Supply Current Unconfigured	I_{CCINIT}		80 60		mA	V_{DD}, V_{DDP} = 2.5V V_{DDA}, V_{DDIO} = 3.3V
Supply Current Active	I_{CC}		80 60	100 70	mA	V_{DD}, V_{DDP} = 2.5V V_{DDA}, V_{DDIO} = 3.3V
Supply Current Standby	I_{CSBY}		4 2	170 130	µA	V_{DD}, V_{DDP} = 2.5V V_{DDA}, V_{DDIO} = 3.3V

Note 1: Output leakage is measured with the current pins in high impedance.

Note 2: See Appendix A for USB DC electrical characteristics.

Note 3: Unconfigured and Operating Supply currents are measured in HS mode.

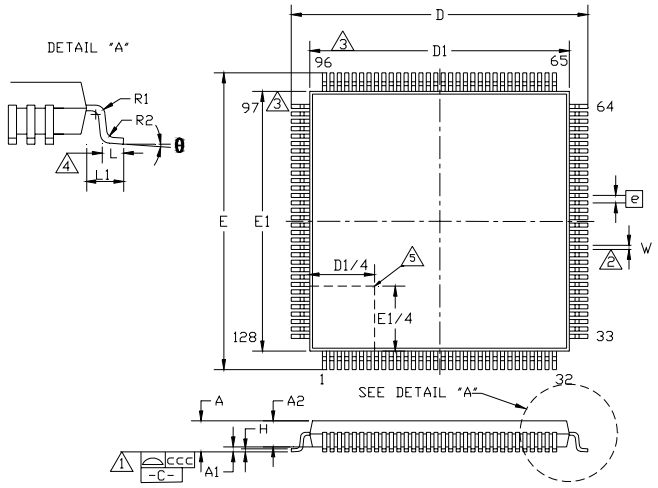
Note 4: Standby currents are measured in optimum board configuration and vary depending on system configuration.

Table 6.2 - Capacitance T_A = 25°C; fc = 1MHz; V_{DD} = 2.5V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except USB pins (and pins under test tied to AC ground)
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

Chapter 7 Package Outlines

7.1 128 Pin VTQFP Package Outline, 14X14X1.0 Body, 2 MM Footprint

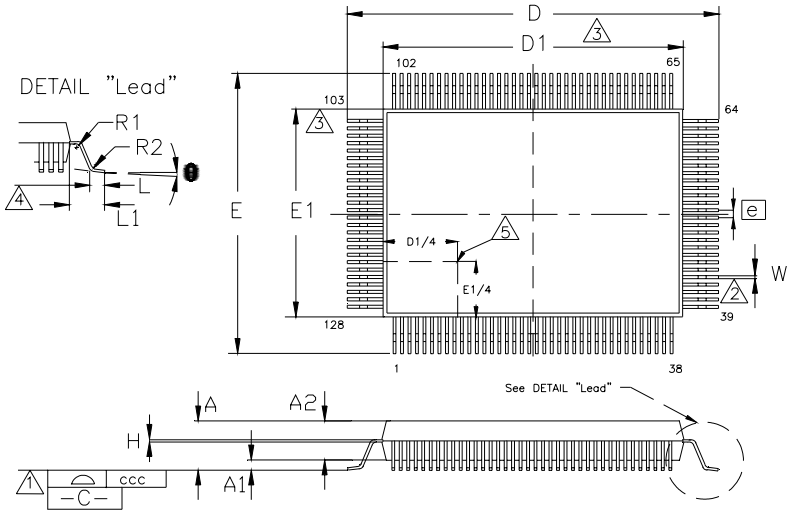


	MIN	NOMINAL	MAX	REMARKS
A	~	~	1.20	Overall Package Height
A1	0.05	~	0.15	Standoff
A2	0.95	~	1.05	Body Thickness
D	15.80	~	16.20	X Span
D1	13.80	~	14.20	X body Size
E	15.80	~	16.20	Y Span
E1	13.80	~	14.20	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length
L1	~	1.00	~	Lead Length
e	0.40 Basic			Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.13	0.18	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

[1] Controlling Unit: millimeter.
[2] Tolerance on the true position of the leads is ± 0.035 mm maximum.
[3] Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.
[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

7.2 128 Pin QFP Package Outline, 14X20X2.7 Body, 3.9 MM Footprint



	MIN	NOMINAL	MAX	REMARKS
A	~	~	3.4	Overall Package Height
A1	0.05	~	0.5	Standoff
A2	2.55	~	3.05	Body Thickness
D	23.70	~	24.10	X Span
D1	19.90	~	20.10	X body Size
E	17.70	~	18.10	Y Span
E1	13.90	~	14.10	Y body Size
H	0.09	~	0.20	Lead Frame Thickness
L	0.73	0.88	1.03	Lead Foot Length
L1	~	1.95	~	Lead Length
e	0.50 Basic			Lead Pitch
θ	0^o	~	7^o	Lead Foot Angle
W	0.10	~	0.30	Lead Width
R1	0.13	~	~	Lead Shoulder Radius
R2	0.13	~	0.30	Lead Foot Radius
ccc	~	~	0.08	Coplanarity

Notes:

[1] Controlling Unit: millimeter.
[2] Tolerance on the position of the leads is ± 0.04 mm maximum.
[3] Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.
[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.
[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

Chapter 8 Typical Application