MOTOROLA

Military 54F192

Advance Information

Synchronous 4-Bit Up/Down Decade Counter (Asynchronous Master Reset)

ELECTRICALLY TESTED PER:
MIL-M-38510/34404

The 54F192 is an up/down BCD decade (8241) counter. The 54F193 is an up/down modulo-16 binary counter. Separate Count Up and Count Down Clocks are used, and in either counting mode the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs.

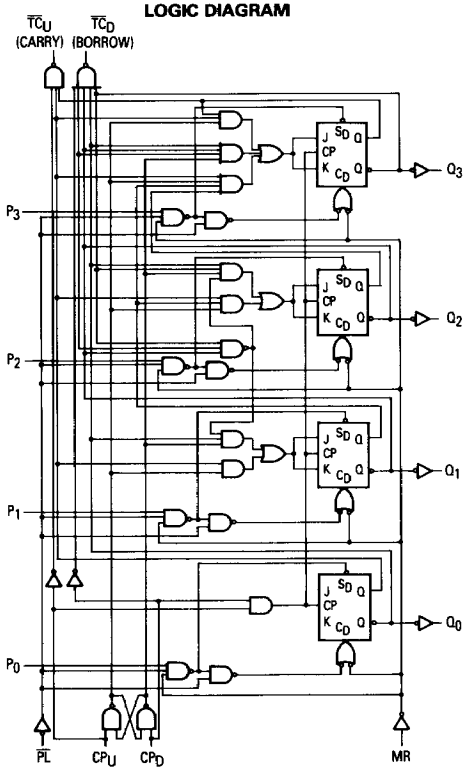
Separate Terminal Count Up and Terminal Count Down outputs are provided that are used as the clocks for a subsequent stage without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

AVAILABLE AS:

1) JAN: *
2) SMD: *
3) 883C: *

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2
***Call Factory for latest update**

LOGIC DIAGRAM



PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
P_1	1	1	2	V_{CC}
Q_1	2	2	3	OPEN
Q_0	3	3	4	OPEN
CP_D	4	4	5	V_{CC}
CP_U	5	5	7	V_{CC}
Q_2	6	6	8	OPEN
Q_3	7	7	9	OPEN
GND	8	8	10	GND
P_3	9	9	12	V_{CC}
P_2	10	10	13	V_{CC}
$\overline{PL}$	11	11	14	GND
$\overline{TC}_U$	12	12	15	OPEN
$\overline{TC}_D$	13	13	17	V_{CC}
MR	14	14	18	GND
P_0	15	15	19	V_{CC}
V_{CC}	16	16	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

FUNCTION TABLE

MR	$\overline{PL}$	CP_U	CP_D	MODE
H	X	X	X	Reset (Asyn.)
L	L	X	X	Preset (Asyn.)
L	H	H	H	No Change
L	H	⎍	H	Count Up
L	H	H	⎍	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

This document contains information on a new product. Specifications and information herein are subject to change without notice.

FUNCTIONAL DESCRIPTION

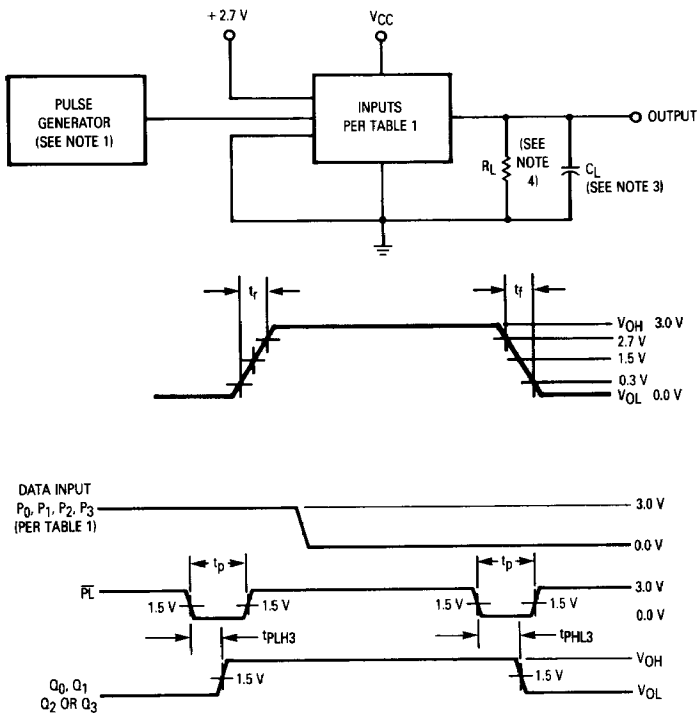
The 'F192, '193 are asynchronously presettable counters. The 'F192 is a decade counter while the 'F193 is organized for 4-bit binary operation. They both contain four edge triggered flip-flops, with internal gating and steering logic to provide master reset, individual preset, count up and count down operations.

A LOW-to-HIGH transition on the CP input to each flip-flop causes the output to change state. Synchronous switching, as opposed to ripple counting, is achieved by driving the steering gates of all stages from a common Count Up line and a common Count Down line, thereby causing all state changes to be initiated simultaneously. A LOW-to-HIGH transition on the Count Up input will advance the count by one; a similar transition on the Count Down input will decrease the count by one. While counting with one clock input, the other should be held HIGH, as indicated in the Function Table. Otherwise, the circuit will either count by twos or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW.

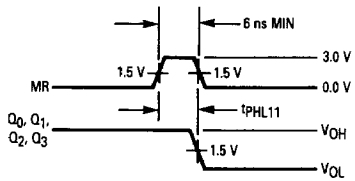
The Terminal Count Up ($\overline{TC}_U$) and Terminal Count Down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state; 9 ('F192) or 16 ('F193), the reset HIGH-to-LOW transition of the Count Up Clock will cause $\overline{TC}_U$ to go LOW. $\overline{TC}_U$ will stay LOW until $\overline{CP}_U$ goes HIGH again, thus effectively repeating the Count Up Clock, but delayed by two gate delays. Similarly, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the Count Down Clock goes LOW. Since the $\overline{TC}$ outputs repeat the clock waveforms, they can be used as the clock input signals to the next higher order circuit in a multistage counter.

Both the 'F192 and the 'F193 have an asynchronous parallel load capability permitting the counter to be preset. When the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs are LOW, information present on the Parallel Data input (P_0–P_3) is loaded into the counter and appears on the outputs regardless of the conditions of the clock inputs. A HIGH signal on the Master Reset input will disable the preset gates, override both clock inputs, and latch each Q output in the LOW state. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

TEST CIRCUIT AND WAVEFORMS



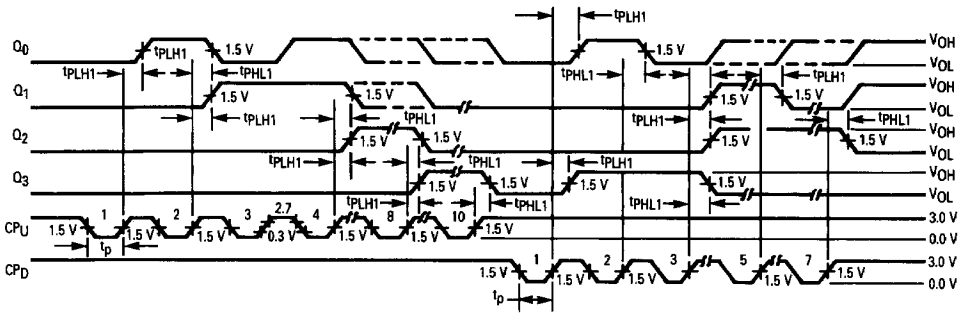
Parallel Loaded Voltage Waveforms



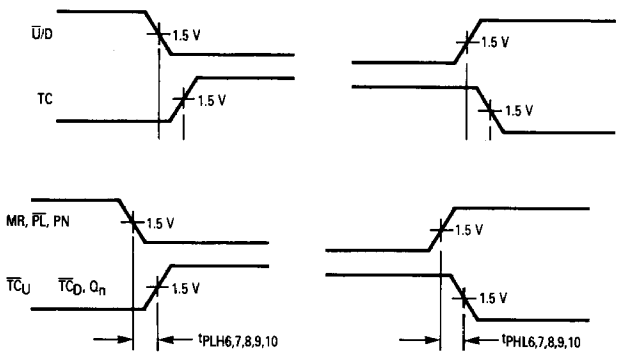
NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR $\leq$ 1.0 MHz, $Z_{out} \approx 50\ \Omega$.
2. Terminal conditions (pins not designated may be high $\geq$ 2.0 V, low $\leq$ 0.8 V, or open).
3. C_L = 50 pF ± 10%, including scope probe, wiring, and stray capacitance without package in test fixture.
4. R_L = 499 Ω ± 5.0%.
5. Voltage measurements are to be made with respect to network terminal ground.

Clear Switching Voltage Waveform

WAVEFORMS

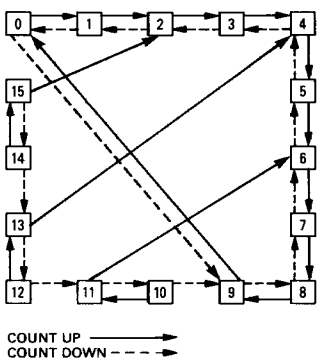


Serial Loaded Voltage Waveforms



Switching Time Waveforms

STATE DIAGRAM



Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = −1.0 mA, V_{IH} = 2.0 V, or 0 V, MR = 0 V or 0.8 V, $\overline{PL}$ = 0 V or 0.8 V, CP_n = 2.0 V or 5.5 V.
V_{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V_{CC} = 4.5 V, I_{OL} = 20 mA, V_{IL} = 0.8 V or 0 V, MR = 0 V, $\overline{PL}$ = 0.8 V or 0 V, CP_n = 5.5 V or 0.8 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	μA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	μA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{IL}	Logical "0" Input Current	−0.03	−0.6	−0.03	−0.6	−0.03	−0.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, $\overline{PL}$ & MR = 0 V or (0.5 V), other inputs are open.
$I_{IL(CP_n)}$	Logical "0" Input Current	−0.75	−1.8	−0.75	−1.8	−0.75	−1.8	mA	V_{CC} = 5.5 V, $V_{IN(CP_n)}$ = 0.5 V, other CP_n input = 5.5 V, other inputs are open.
I_{OS}	Short Circuit Output Current	−60	−150	−60	−150	−60	−150	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V or 0 V, V_{OUT} = 0 V, $\overline{PL}$ & MR = 0 V, CP_n = 5.5 V or open.
I_{CC}	Power Supply Current Off		55		55		55	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V (all inputs), $\overline{PL}$ & MR = 0 V.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.
		Subgroup 7		Subgroup 8A		Subgroup 8B			
	Functional Tests								per Truth Table with V_{CC} = 4.5 V **(Repeat at)** V_{CC} = 5.5 V, V_{INL} = 0.5 V, and V_{INH} = 2.5 V.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+25°C		+125°C		−55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output CP_n to Q_n	5.5	12.5	5.5	12.5	5.5	12.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH1}	Propagation Delay /Data-Output CP_n to Q_n	4.0	8.5	4.0	8.5	4.0	8.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL2}	Propagation Delay /Data-Output CP_U to $\overline{TC}_U$	3.5	8.0	3.5	8.0	3.5	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH2}	Propagation Delay /Data-Output CP_U to $\overline{TC}_U$	4.0	9.0	4.0	9.0	4.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL3}	Propagation Delay /Data-Output $\overline{PL}$ to Q_n	5.0	13	5.0	13	5.0	13	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH3}	Propagation Delay /Data-Output $\overline{PL}$ to Q_n	5.0	11	5.0	11	5.0	11	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL4}	Propagation Delay /Data-Output CP_D to $\overline{TC}_D$	3.5	8.0	3.5	8.0	3.5	8.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH4}	Propagation Delay /Data-Output CP_D to $\overline{TC}_D$	4.0	9.0	4.0	9.0	4.0	9.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL5}	Propagation Delay /Data-Output P_n to Q_n	6.0	14.5	6.0	14.5	6.0	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH5}	Propagation Delay /Data-Output P_n to Q_n	3.0	7.0	3.0	7.0	3.0	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL6}	Propagation Delay /Data-Output MR to $\overline{TC}_D$	7.0	14.5	7.0	14.5	5.5	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH6}	Propagation Delay /Data-Output MR to $\overline{TC}_U$	6.0	13.5	6.0	13.5	6.0	13.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL7}	Propagation Delay /Data-Output $\overline{PL}$ to $\overline{TC}_D$	7.0	14.5	5.5	14.5	5.5	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH7}	Propagation Delay /Data-Output $\overline{PL}$ to $\overline{TC}_U$	7.0	15.5	7.0	15.5	7.0	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

5

Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		−55°C			
	Static Parameters:	Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL8}	Propagation Delay /Data-Output $\overline{PL}$ to $\overline{TC}_D$	7.0	14.5	4.0	14.5	4.0	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH8}	Propagation Delay /Data-Output $\overline{PL}$ to $\overline{TC}_D$	7.0	15.5	4.0	15.5	4.0	15.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
f_{MAX}	Maximum Clock Frequency	90		90		90		MHz	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL9}	Propagation Delay /Data-Output P_n to $\overline{TC}_U$	6.5	14	6.5	14	6.5	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH9}	Propagation Delay /Data-Output P_n to $\overline{TC}_U$	7.0	14.5	7.0	14.5	7.0	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL10}	Propagation Delay /Data-Output P_n to $\overline{TC}_D$	6.5	14	6.5	14	6.5	14	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PLH10}	Propagation Delay /Data-Output P_n to $\overline{TC}_D$	7.0	14.5	7.0	14.5	7.0	14.5	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.
t_{PHL11}	Propagation Delay /Data-Output MR to Q_n	6.5	14.5	14.5	7.0	14.5	7.0	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 499 Ω.

5