DATA SHEET

54F373/4
Latches/flip-flops

Product specification

1995 Jun 08

Military and Special Products Data Handbook

Philips
Semiconductors

PHILIPS

54F373 Octal transparent latch (3-State)
54F374 Octal D-type flip-flop (3-State)

FEATURES

- 8-bit transparent latch — 54F373
- 8-bit positive, edge-triggered register — 54F374
- 3-State output buffers
- Common 3-State output enable
- Independent register and 3-State buffer operation
- See 54F573 for broadside pinout version of the 54F373
- See 54F574 for broadside pinout version of the 54F374

DESCRIPTION

The 54F373 is an octal transparent latch coupled to eight 3-State output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
20-Pin Ceramic DIP	54F373/BRA, 54F374/BRA	GDIP1-T20
20-Pin Ceramic Flat Pack	54F373/BSA, 54F374/BSA	GDFP2-F20
20-Pin Ceramic LLCC	54F373/B2A, 54F374/B2A	CQCC2-N20

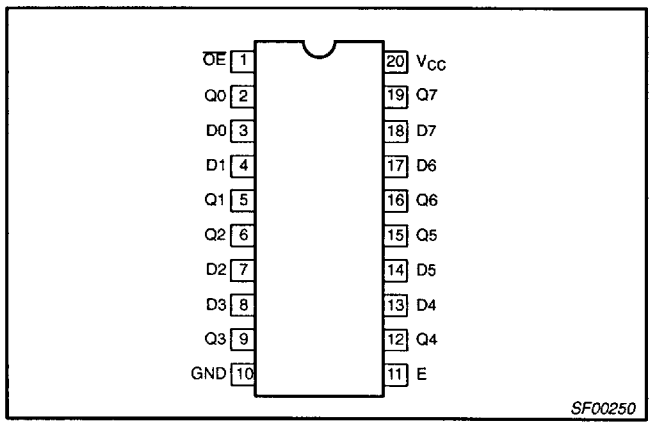
* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

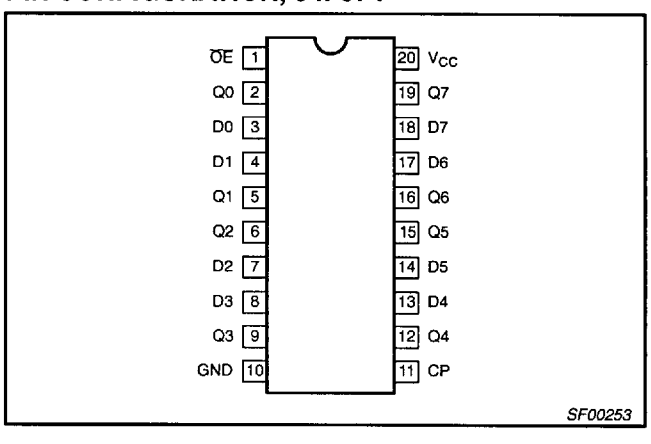
PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D7	Data inputs	1.0/1.0	20μA/0.6mA
E (54F373)	Latch enable input (active High)	1.0/1.0	20μA/0.6mA
$\overline{OE}$	Output enable input (active Low)	1.0/1.0	20μA/0.6mA
CP (54F374)	Clock pulse input (active rising edge)	1.0/1.0	20μA/0.6mA
Q0 - Q7	3-State outputs	150/33	3mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

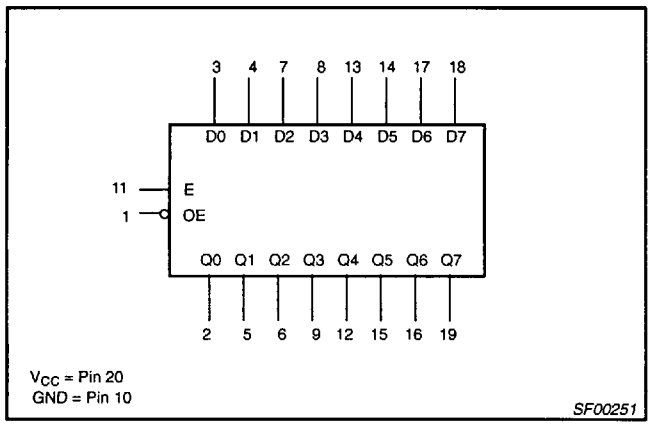
PIN CONFIGURATION, 54F373



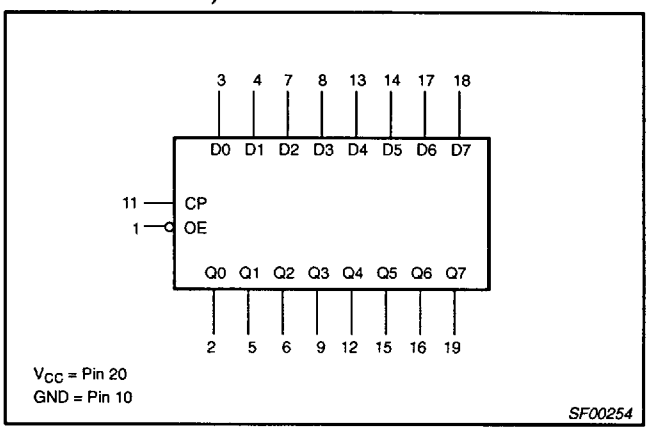
PIN CONFIGURATION, 54F374



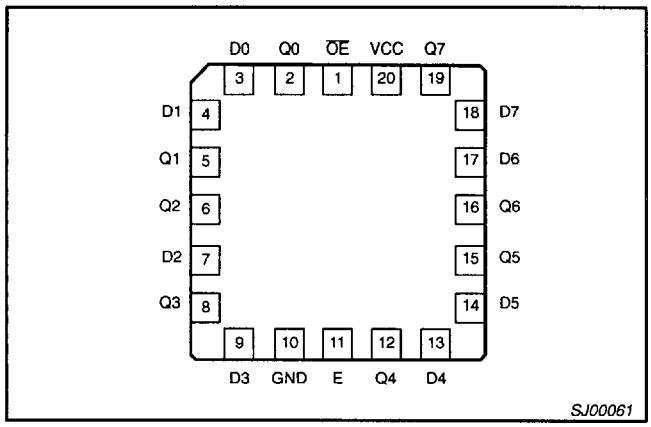
LOGIC SYMBOL, 54F373



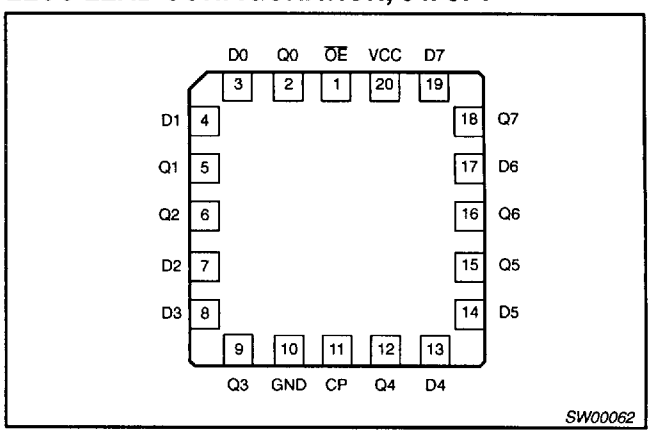
LOGIC SYMBOL, 54F374



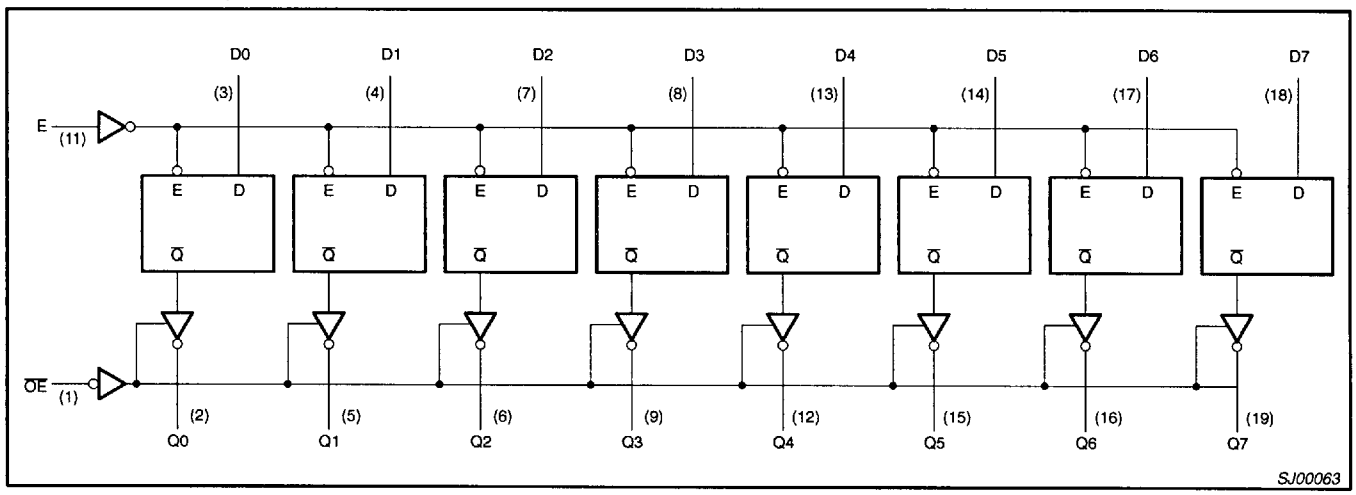
LLCC LEAD CONFIGURATION, 54F373



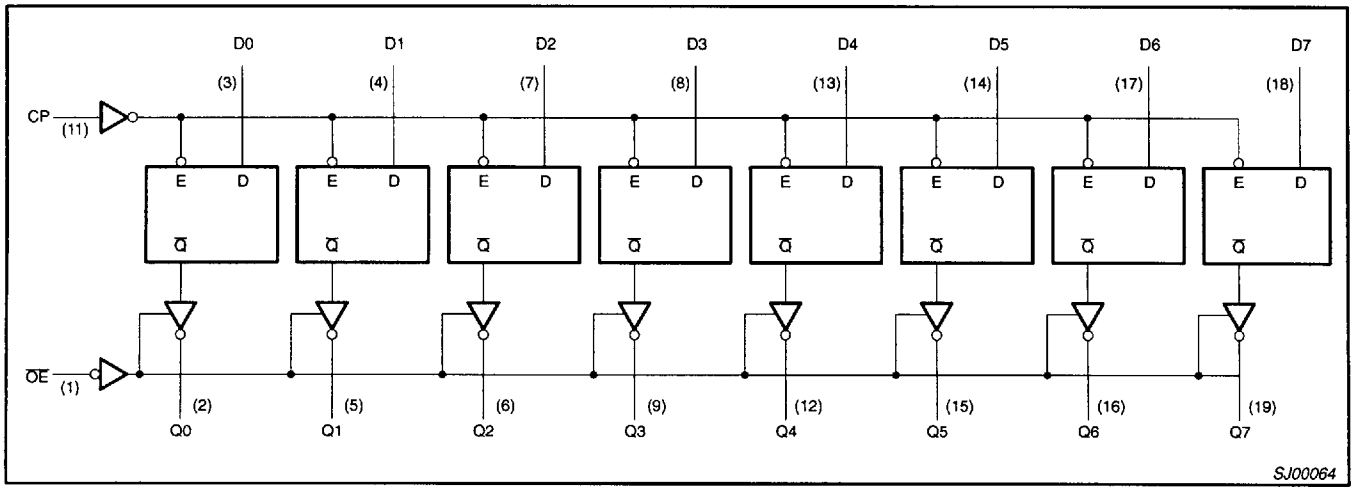
LLCC LEAD CONFIGURATION, 54F374



LOGIC DIAGRAM, 54F373



LOGIC DIAGRAM, 54F374



When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

The 54F374 is an 8-bit, edge-triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the Clock (CP) and Output Enable ($\overline{OE}$) control gates. The register is fully edge triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High impedance "off" state, which means they will neither drive nor load the bus.

FUNCTION TABLE, 54F373

INPUTS			INTERNAL REGISTER	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	Dn		Q0 - Q7	
L	H	L	L	L	Enable and read register
L	H	H	H	H	
L	↓	l	L	L	Latch and read register
L	↓	h	H	H	
L	L	X	NC	NC	Hold
H	L	X	NC	Z	Disable outputs
H	H	Dn	Dn	Z	

NOTES:
H = High-voltage level
h = High state must be present one setup time before the high-to-low enable transition
L = Low-voltage level
l = Low state must be present one setup time before the high-to-low enable transition
NC= No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-low enable transition

FUNCTION TABLE, 54F374

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	Dn	REGISTER	Q0 - Q7	
L	↑	l	L	L	Load and read register
L	↑	h	H	H	
L	↕	X	NC	NC	Hold
H	↕	X	NC	Z	Disable outputs
H	↑	Dn	Dn	Z	

NOTES:
H = High-voltage level
h = High state must be present one setup time before the low-to-high clock transition
L = Low-voltage level
l = Low state must be present one setup time before the low-to-high clock transition
NC= No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-high clock transition
↕ = Not low-to-high clock transition

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +5.5	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH1}	High-level output current			-1	mA
I_{OH2}	High-level output current			-3	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = Min, V_{IH} = Min,	I_{OH1} = -1mA	2.5			V
			V_{IL} = Max	I_{OH2} = -3mA	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = Min, I_I = I_{IK}			-0.73	-1.2	V
I_{OZH}	Off-state output current, High-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 2.7V				50	µA
I_{OZL}	Off-state output current, Low-level voltage applied		V_{CC} = Max, V_{IH} = Min, V_O = 0.5V				-50	µA
I_{IH2}	Input current at maximum input voltage		V_{CC} = Max, V_I = 7.0V				100	µA
I_{IH1}	High-level input current		V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low-level input current		V_{CC} = Max, V_I = 0.5V				-0.6	mA
I_{OS}	Short-circuit output current[3]		V_{CC} = Max, V_O = 0.0V		-60		-150	mA
I_{CC}	Supply current (total)	54F373	V_{CC} = Max	I_{CCZ} $\overline{OE} \geq$ 4.0V, D inputs = E = GND		35	55	mA
		54F374		I_{CCZ} CP ≥ 4.0V, D inputs = GND		57	86	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55°C to +125°C, V_{CC} = +5.0V ± 10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	54F374	Waveform 6	100			60		MHz
t_{PLH} t_{PHL}	Propagation delay E to Qn	54F373	Waveform 1	3.0 1.0	9.0 4.0	11.5 7.0	3.0 2.0	15.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dn to Qn	54F373	Waveform 4	3.0 2.0	5.3 3.7	7.0 5.0	3.0 1.7	8.5 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay CP to Qn	54F374	Waveform 6	4.0 4.0	6.5 6.5	8.5 8.5	4.0 4.0	10.5 11.5	ns ns
t_{PZH}	Output enable time to High level	54F373 54F374	Waveform 2	2.0 2.0	5.0 9.0	11.0 11.5	2.0 2.0	13.5 14.0	ns ns
t_{PZL}	Output enable time to Low level	54F373 54F374	Waveform 3	2.0 2.0	5.6 5.3	7.5 7.5	2.0 2.0	10.0 10.0	ns ns
t_{PHZ}	Output disable time from High level	54F373 54F374	Waveform 2	2.0 2.0	4.5 5.3	6.5 7.0	2.0 2.0	10.0 8.0	ns ns
t_{PLZ}	Output disable time from Low level	54F373 54F374	Waveform 3	2.0 2.0	3.8 4.3	5.0 5.5	2.0 2.0	7.0 7.5	ns ns

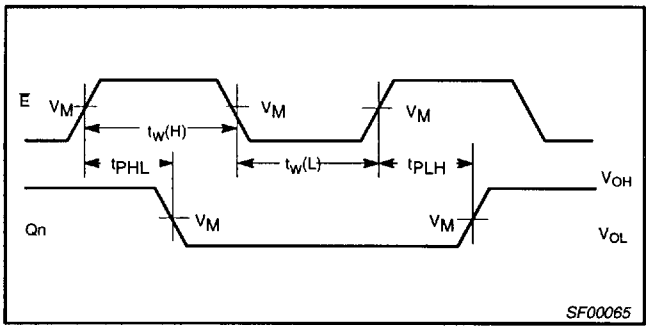
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_A = +25°C V_{CC} = +5.0V C_L = 50pF R_L = 500Ω			T_A = -55°C to +125°C V_{CC} = +5.0V ± 10% C_L = 50pF R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to E	54F373	Waveform 5	2.0 2.0			2.0 2.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to E	54F373	Waveform 5	3.0 3.0			3.0 3.0		ns ns
$t_w(H)$ $t_w(L)$	Clock pulse width	54F374	Waveform 6	7.0 6.0			7.0 6.0		ns ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low Dn to CP	54F374	Waveform 7	2.0 2.0			2.5 2.0		ns ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low Dn to CP	54F374	Waveform 7	2.0 2.0			2.0 2.5		ns ns
$t_w(H)$ $t_w(L)$	Latch enable pulse width	54F373	Waveform 1	6.0 6.0			6.0 6.0		ns ns

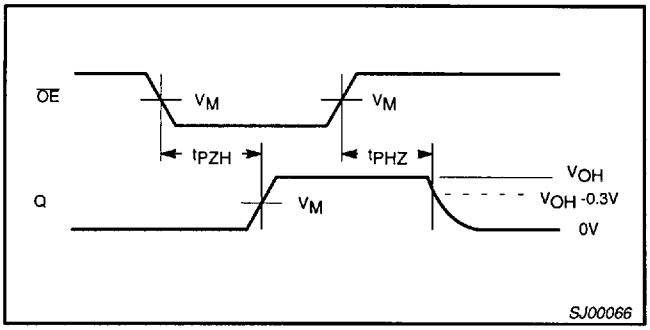
NOTES:

1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

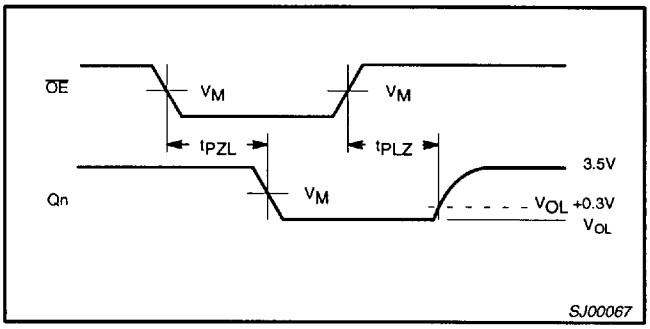
AC WAVEFORMS



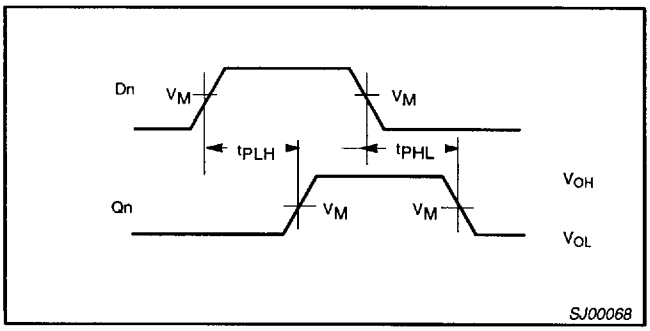
Waveform 1. Latch Enable to Output Delays and Latch Enable Pulse Width



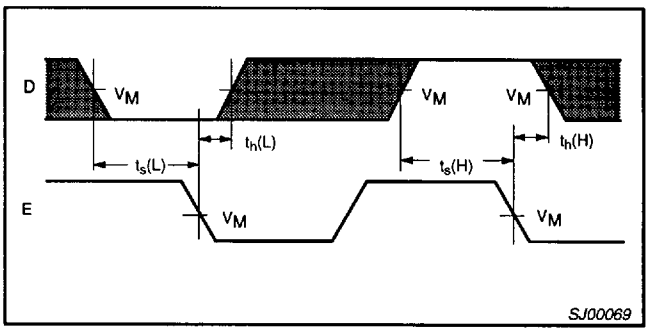
Waveform 2. 3-State Output Enable Time to High Level and Output Disable Time from High Level



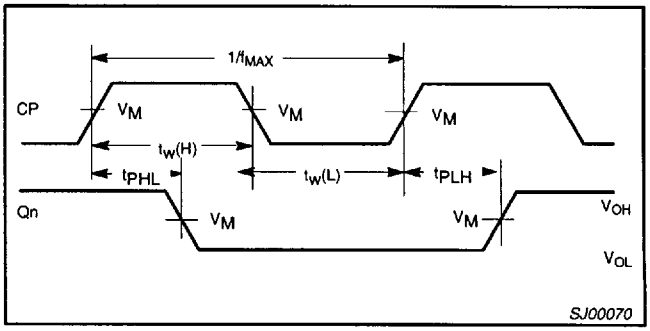
Waveform 3. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level



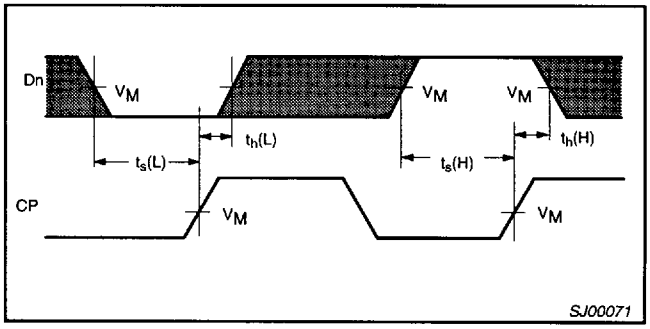
Waveform 4. Propagation Delay Data to Q Outputs



Waveform 5. Data Setup and Hold Times

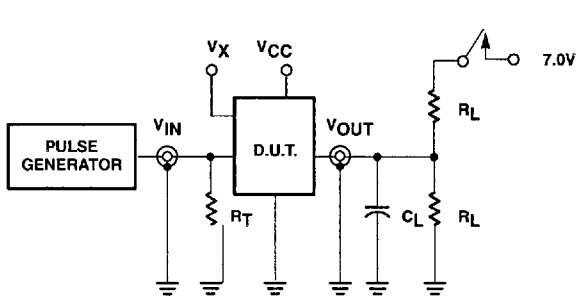


Waveform 6. Clock to Output Delays and Pulse Width

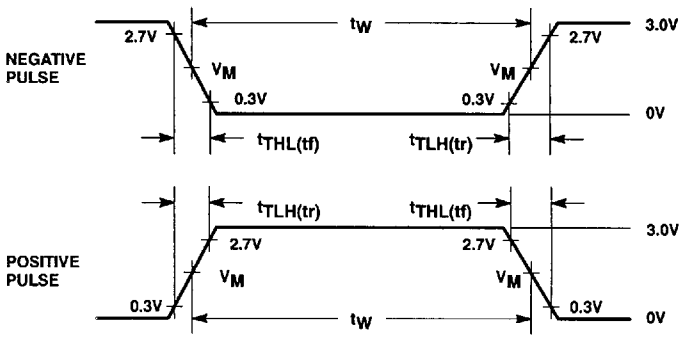


Waveform 7. Data Setup and Hold Times

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



Input Pulse Definitions

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All others	open

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**t_W**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V, ≥2.7V or open per Function Table.

SJ00072