Military 93415

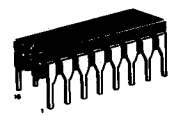
TTL 1024 x 1-Bit Random Access Memory

The 93415 is a 1024-bit Read/Write RAM organized 1024 words by 1 bit.

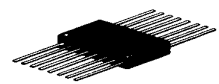
The 93415 is designed for buffer control storage and high performance main memory applications, and has a typical access time of 35 ns.

The 93415 has full decoding on-chip, separate data input and data output lines, and an active low chip select. The device is fully compatible with standard DTL and TTL logic families and features an uncommitted collector output for ease of memory expansion.

- Uncommitted Collector Output
- TTL Inputs and Output
- Non-Inverting Data Output
- High Speed —
  - Access Time — 35 ns Typical
  - Chip Select — 15 ns Typical
- Power Dissipation Decreases with Increasing Temperature
- Power Dissipation 0.5 mW/Bit Typical
- Organized 1024 Words x 1 Bit
- Order as: 93415/BEAJC = Dual-In-Line
  93415/BFAJC = Flat Pack

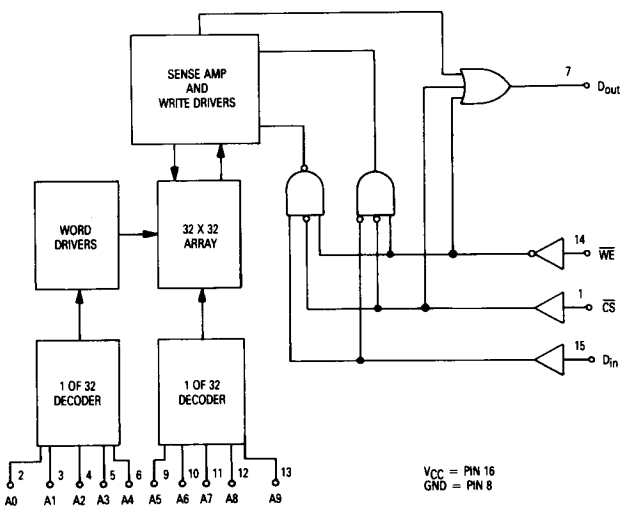


CASE 620-09
CERAMIC DUAL-IN-LINE

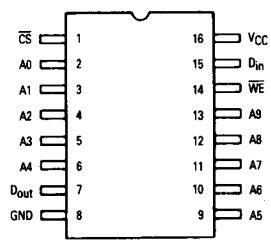


CASE 650-05
FLAT PACK

BLOCK DIAGRAM



PIN ASSIGNMENT



PIN NAMES	
$\overline{CS}$	Chip Select
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{in}	Data Input
D_{out}	Data Output

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FUNCTIONAL DESCRIPTION

The 93415 is a fully decoded 1024-bit Random Access Memory organized 1024 words by one bit. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active low Write Enable ($\overline{WE}$, Pin 14). With $\overline{WE}$ held low and the chip selected, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{out} and is non-inverted.

Uncommitted collector outputs are provided to allow wired-OR applications. In any application an external pull-up resistor of R_L value must be used to provide a high at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC}(Min)}{I_{OL} - FO(1.6)} \leq R_L \leq \frac{V_{CC}(Min) - V_{OH}}{n(I_{CEX}) + FO(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output High Level at Output Node
I_{OL} = Output Low Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA High/1.6 mA Low.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Storage Temperature Ceramic Package (E and F Suffix)	−55°C to +165°C
Operating Junction Temperature, T_J Ceramic Package (E and F Suffix)	<165°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)	−0.5 V to +5.5 V
Voltage Applied to Outputs (Output High)	−0.5 V to +5.5 V
Output Current (dc) (Output Low)	+20 mA
Input Current (dc)	−12 mA to +5.0 mA

NOTE 1: Device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.

TRUTH TABLE

Inputs			Output	
$\overline{CS}$	$\overline{WE}$	D_{in}	Open Collector	Mode
H	X	X	H	Not Selected
L	L	L	H	Write "0"
L	L	H	H	Write "1"
L	H	X	D_{out}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care (High or Low)

GUARANTEED OPERATING RANGES (Note 2)

Supply Voltage (V_{CC})			
Min	Nom	Max	Ambient Temperature (T_A)
4.5 V	5.0 V	5.5 V	−55°C to +125°C

DC OPERATING CONDITIONS AND CHARACTERISTICS (Full operating voltage and temperature range unless otherwise noted)

Symbol	Characteristic	Limits Min	Limits Max	Unit	Conditions	
V_{OL}	Output Low Voltage		0.45	Vdc	V_{CC} = Min, I_{OL} = 16 mA	
V_{IH}	Input High Voltage	2.1		Vdc	Guaranteed Input High Voltage for All Inputs	
V_{IL}	Input Low Voltage		0.8	Vdc	Guaranteed Input Low Voltage for All Inputs	
I_{IL}	Input Low Current		−400	μAdc	V_{CC} = Max, V_{in} = 0.4 V	
I_{IH}	Input High Current		40	μAdc	V_{CC} = Max, V_{in} = 4.5 V	
I_{CEX}	Output Leakage Current		100	μAdc	V_{CC} = Max, V_{out} = 5.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.5	Vdc	V_{CC} = Max, I_{in} = −12 mA	
I_{CC}	Power Supply Current		130	mAdc	T_A = +125°C	V_{CC} = 5.5 V, All Inputs Grounded
			155	mAdc	T_A = 25°C	
			170	mAdc	T_A = −55°C	

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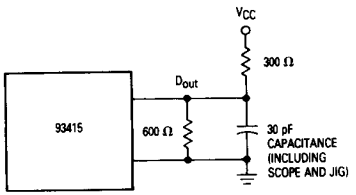
AC OPERATING CONDITIONS AND CHARACTERISTICS

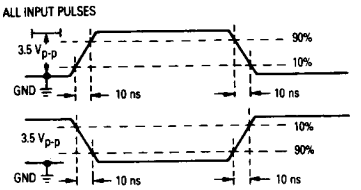
(Full operating voltage and temperature unless otherwise noted)

AC TEST LOAD AND WAVEFORM

LOADING CONDITION



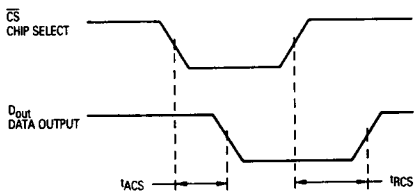
INPUT PULSES



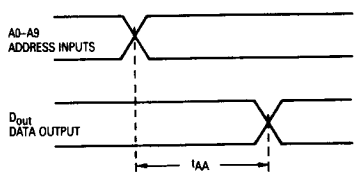
Symbol	Characteristic (Notes 2, 3)	93415/BE/BF Min	93415/BE/BF Max	Unit	Conditions
READ MODE	DELAY TIMES			ns	
t_{ACS}	Chip Select Time		45		See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		50		
t_{AA}	Address Access Time		60		
WRITE MODE	DELAY TIMES			ns	
t_{WS}	Write Disable Time		45		See Test Circuit and Waveforms
t_{WR}	Write Recovery Time		50		
	INPUT TIMING REQUIREMENTS			ns	
t_W	Write Pulse Width (to guarantee write)	40			
t_{WSD}	Data Setup Time Prior to Write	5.0			
t_{WHD}	Data Hold Time After Write	5.0			See Test Circuit and Waveforms
t_{WSA}	Address Setup Time (at t_W = Min)	15			
t_{WHA}	Address Hold Time	10			
t_{WSCS}	Chip Select Setup Time	5.0			
t_{WHCS}	Chip Select Hold Time	5.0			

READ OPERATION TIMING DIAGRAM

PROPAGATION DELAY FROM CHIP SELECT



PROPAGATION DELAY FROM ADDRESS INPUTS



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

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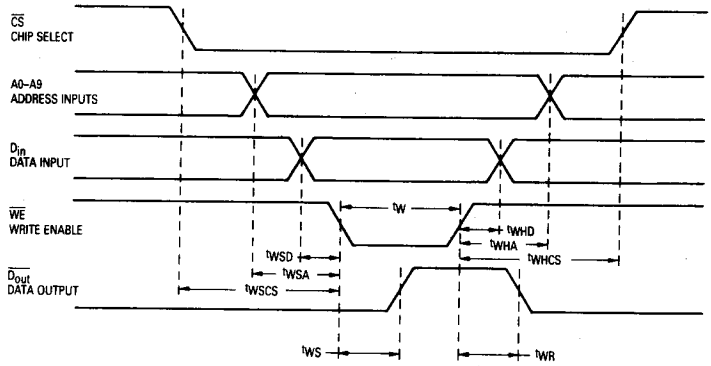
WRITE CYCLE TIMING



(ALL TIME MEASUREMENTS REFERENCED TO 1.5 V)

NOTE 2: DC and AC specifications limits guaranteed with 500 linear feet per minute blown air.

Package	θ_{JA} (Junction to Ambient)		θ_{JC} (Junction to Case)
	Blown	Still	
E Suffix	50°C/W	85°C/W	15°C/W
F Suffix	55°C/W	90°C/W	15°C/W

NOTE 3: The AC limits are guaranteed to be the worst case bit in the memory.

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