AsahiKASEI
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AKD7780

AK7780 Evaluation Board Rev.0

GENERAL DESCRIPTION

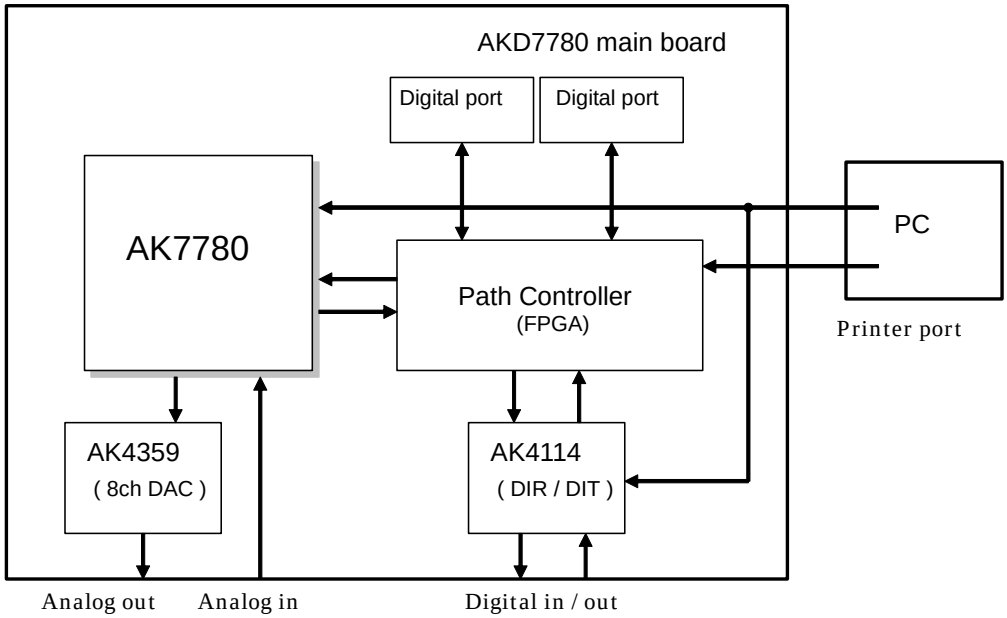
The AKD7780 is an evaluation board for AK7780, which is a highly integrated audio processor including two 24-bit stereo ADC's, a mono ADC and a stereo SRC. This board is composed of a main board and a sub board. AKD7780 has SPDIF input/output port, 2 pairs of stereo analog input ports, 1 mono analog input port, 4 pairs of stereo analog output ports and this helps to the evaluation of AK7780.

■ Ordering guide

AKD7780 --- Evaluation board for AK7780
Cable for connecting with printer port of IBM-AT compatible PC and control software and driver for Windows 2000/XP are packed with this.
This control software does not operate on Window NT.
Windows 2000/XP needs an installation of driver. In case of Windows 95/98/ME, the installation is not needed.

FUNCTION

- **Register setting / Download / Read back function to/from PC**
- **Digital interface by SPDIF I/O**
- **Digital interface by general audio data header(x2)**
- **Analog interface of ADC 5ch / DAC 8ch**
  (Note: There is no DAC within AK7780. 8ch DAC AK4359 is equipped.)



(Note) AK4114 has DIR, DIT and X'tal oscillator.
Figure 1. AKD7780 Block Diagram

Evaluation Board Diagram

■ Board Diagram

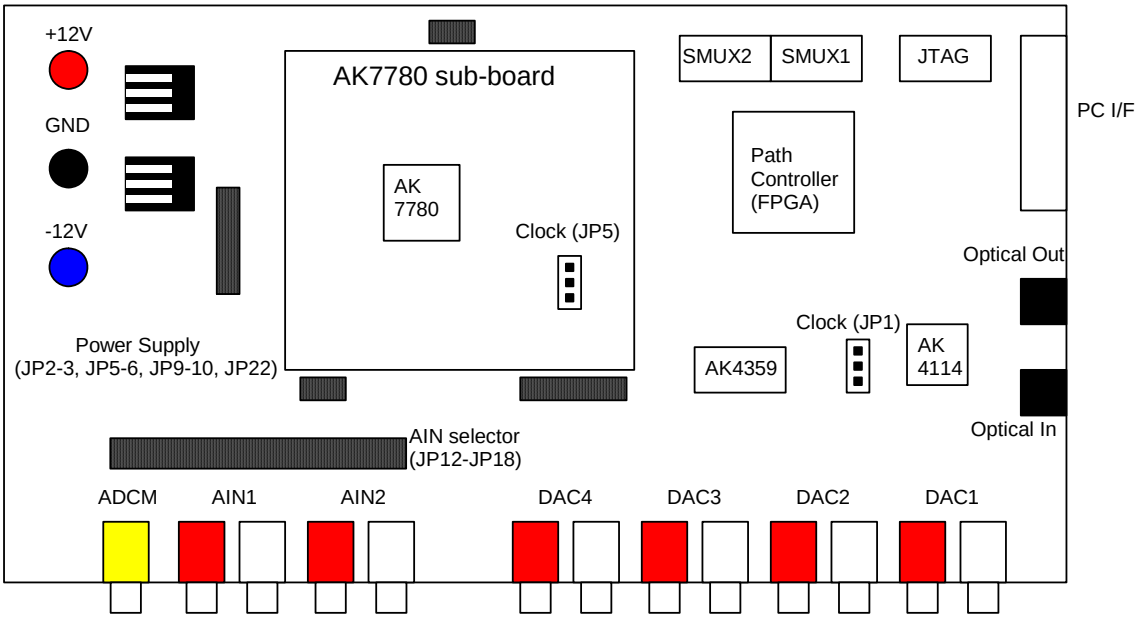


Figure 2. AK7780 Board Diagram

■ Description

(1) AIN/DAC/ADCM
RCA Jack. White is for Lch and Red is for Rch. Yellow one is for mono input.

(2) Optical In
Optical input connector. It supports sampling frequencies from 32Hz to 48Hz. It is used as digital data source for AK7780. When AK7780 is operated in slave mode, this input signal is always necessary.

(3) Optical Out
Optical output connector. It can be selected from SDOUT1-6 or ADOUTA1.

(4) Power Supply
Supply +12V, GND, -12V for each terminal. Current consumption is about 500mA in operation.

(5) Clock (jumper)
Clock source jumper. Select clock source between “EXT” and “XTL” for AK4114 or AK7780.

(6) Other jumper pins’ setting
According to Table 1. / Table 2.

(7) PC/IF
Connect to PC printer port (Parallel port) with attached cable. Input signals are pull-upped with 10k-ohm resistance. Output signals are 0-5V swing.

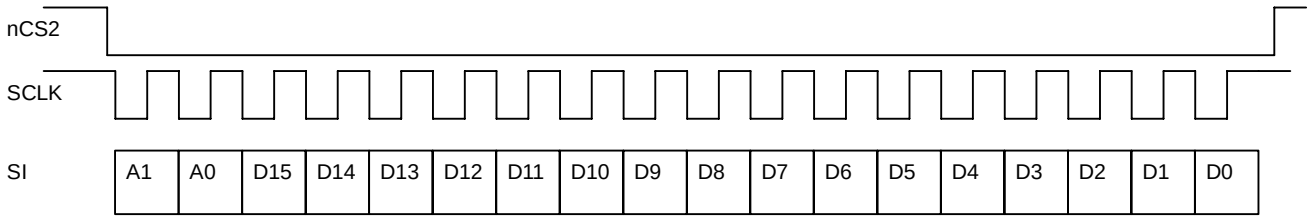
Pin	I/O	Function	Pin	I/O	Function
2	I	nCS3 for AK4114	10	O	(not used)
3	I	INIT_RESET	11	O	(not used)
4	I	(not used)	12	O	RDY
5	I	I2CSEL	13	O	SO
6	I	SCLK	15	O	(not used)
7	I	SI			
8	I	nCS for AK7780			
9	I	nCS2 for FPGA			

(8) Audio digital data port
Two of digital ports (SMUX1/SMUX2) are available.

Pin	I/O	Function	pin	I/O	Function
1	I	MCLK	2	P	GND
3	I	BITCLK	4	P	GND
5	I	LRCLK	6		(NC)
7	I	DI	8		(NC)
9	P	VDD	10	O	DO

■ Path Controller

The Path Controller manages I/O control for audio signal, selector, and AK7780 pin configuration. This controller has 3 words register and each register has 16bit. Access is done by 18bit length as bellow format.



ADDRESS=0		
D[15]	(test)	Set 0.
D[14:12]	SDOUT	Output signal select. 000: SDOUT1 001: SDOUT2 -- 101: SDOUT6 110: SDOUTA1 111:Low
D[11:10]	SRC	Select SRC master device. 00: AK4114 01: SMUX1 10: SMUX2 11: Low
D[9:8]	SDIN5	SDIN5 pin input select 00: AK4114 01: SMUX1 10: SMUX2 11: Low
D[7:6]	SDIN4	SDIN4 pin input select 00: AK4114 01: SMUX1 10: SMUX2 11: Low
D[5:4]	SDIN3	SDIN3 pin input select 00: AK4114 01: SMUX1 10: SMUX2 11: Low
D[3:2]	SDIN2	SDIN2 pin input select 00: AK4114 01: SMUX1 10: SMUX2 11: Low
D[1:0]	SDIN1	SDIN1 pin input select 00: AK4114 01: SMUX1 10: SMUX2 11: Low

ADDRESS=1		
D[6:4]	CKM[2:0]	AK7780 CKM pin setting
D[3:2]	SELSRC[1:0]	AK7780 SELSRC pin setting 00: LRCK 01:BICK 10:TEST 11:TEST
D[1:0]	CAD[1:0]	AK7780 CAD pin setting

ADDRESS=2		
D[15]	TRXPDN	AK4114 PDN pin setting
D[14]	DACPDN	AK4359 reset pin setting
D[13]	SRCRST	AK7780 SRCRST pin setting
D[12]	ADRST	AK7780 ADRST pin setting
D[11]	DSPRST	AK7780 DSPRST pin setting
D[10]	CKRST	AK7780 CKRST pin setting
D[9:8]	MASTER	Select master device for AK7780 00: AK4114 01: SMUX1 10: SMUX2 11: AK7780
D[6]	(not used)	
D[5]	TEST2	AK7780 TEST2I pin setting (Normally 0)
D[4]	TEST1	AK7780 TEST1I pin setting (Normally 0)
D[3]	SRCMUTE	AK7780 SRCMUTE pin setting
D[2]	JX2	AK7780 JX2 pin setting
D[1]	JX1	AK7780 JX1 pin setting
D[0]	JX0	AK7780 JX0 pin setting

Evaluation Board Manual

■ Operation sequence

1. **Set up the power supply lines.**
   [+12V] (red) = +12V
   [-12V] (blue) = -12V
   [GND] (black) = 0V

   Each supply line should be distributed from the power supply unit.

2. **Set up the jumper pins (according to the follows).**

3. **Connect the needed connector (according to the follows).**

4. **Power on.**

5. **Set up the register via PC (according to the follows).**

■ Evaluation Mode

(1) ADC with external DIT

1. Connection of connector
   For analog input, RCA1(AIN1L)/RCA2(AIN1R) or RCA3(AIN2L)/RCA4(AIN2R) or RCA5(AIN MONO) is available.
   For digital output, optical connector PORT2 (TOTX141) is available.

2. Setting of jumper pins for analog output (JP12 – JP18)
   According to Table 3. / Table 4. / Table 5.

3. Set up the FPGA and AK7780 control register via PC.

(2) SRC with external DIR, DIT

1. Connection of connector
   For digital input, optical connector PORT1 (TORX141) is available.
   For digital output optical connector PORT2 (TOTX141) is available.

2. Set up the FPGA and AK7780 control register via PC.

■ Register Control

It is possible to control AKD7780 via printer port (parallel port) of IBM-AT compatible PC. Connect the P1 port on board to PC with the packed cable.

Control software is packed with this board. The software operation sequence is included in the evaluation board manual.

■ Indication for LED

[LED] : U17 When power is supplied , LED is lighted to red. Monitor the PC_RQ_N signal and change the color when the board is communicating with PC.

■ Setting of Jumper Pins

(main board)

Jumper	Setting (Default)	Note
JP01 (AK4114 Clock)	"XTL"	"XTL": XTL "EXT": External Clock
JP02 (AVDD)	Short	AK7780 AVDD
JP03 (AVDD_SRC)	Short	AK7780 AVDD_SRC
JP05 (AVSS)	Short	AK7780 AVSS
JP06 (DVDD18)	Short	AK7780 DVDD18
JP09 (DVSS)	Short	AK7780 DVSS
JP10 (DVDD)	Short	AK7780 DVDD
JP12 (AIN1-Lch)	Short	AINLN
JP13 (AIN1-Rch)	Short	AINRN
JP18 (AIN-Mono)	Short	AINM
JP22 (P DVDD)	Short	Peripheral DVDD

Table 1. Setting of jumper pins on main board

(sub board)

Jumper	Setting (Default)	Note
JP4 (CLKO2)	Short	Short: CLKO1 output
JP5 (AK7780 Clock)	"XTL"	"XTL": XTL "EXT": External Clock
JP6 (CLKO1)	Short	Short: CLKO1 output

Table 2. Setting of jumper pins on sub board

■ Analog Input Circuit

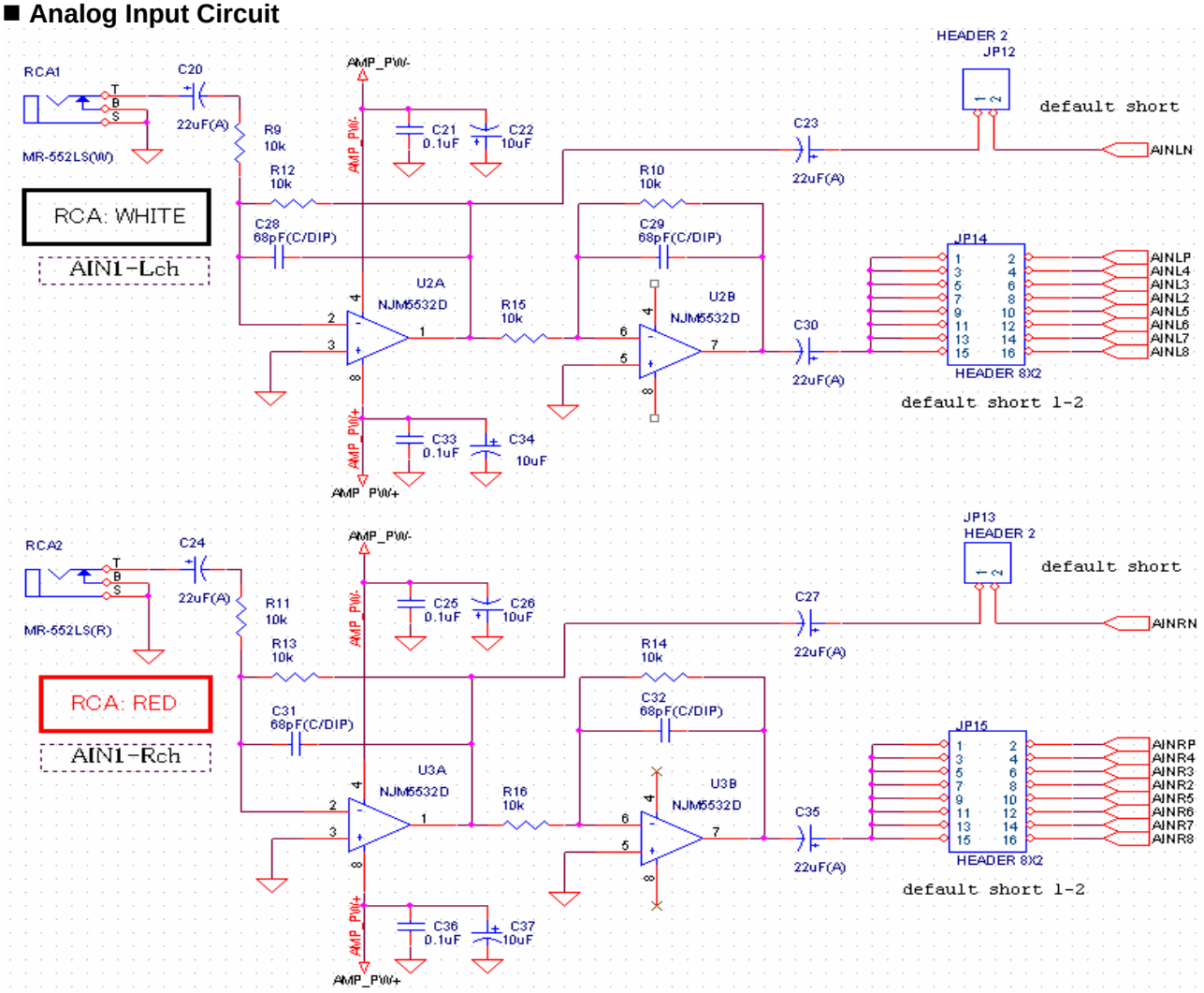


Figure 3. AIN1 Analog Input Circuit

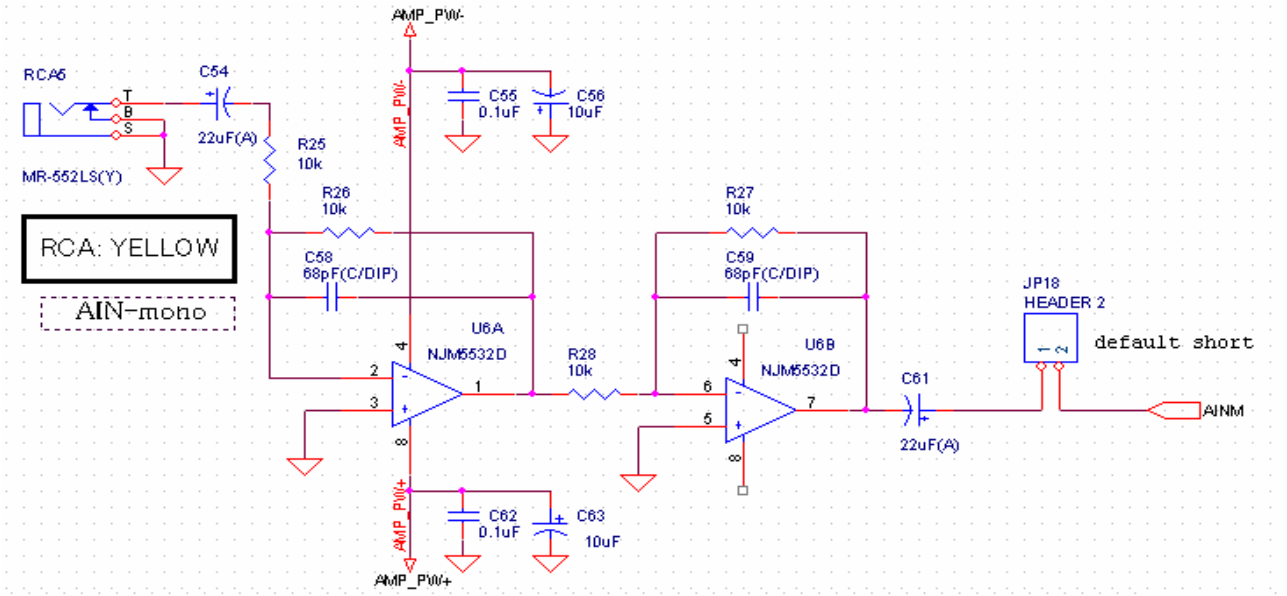


Figure 4. AIN MONO Analog Input Circuit

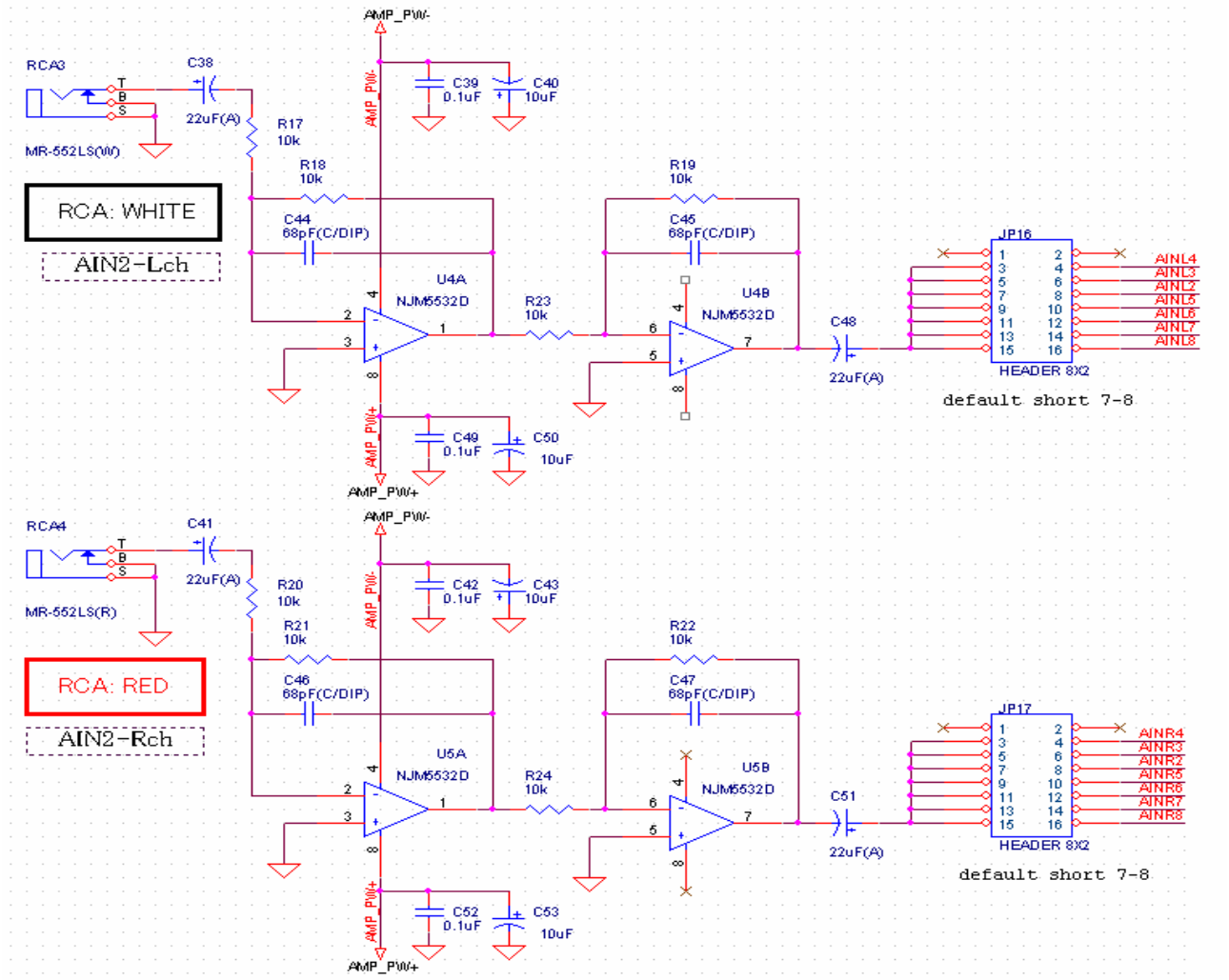


Figure 5. AIN2 Analog Input Circuit

For analog input, RCA1(AIN1L)/ RCA2(AIN1R), RCA3(AIN2L)/RCA4(AIN2R), RCA5(AIN MONO) are available. The AK7780 supports single-ended input mode, monaural single-ended input mode and differential input mode. The input range of AIN is 2.00Vpp@3.3V.

・Setting of jumper pins of analog input circuit

Input Pin	JP12	JP13	JP14	JP15	
AINLN/ AINLP AINRN/AINRP	Short	Short	1-2 pin Short	1-2 pin Short	Default
AINL2/ AINR2	Open	Open	7-8 pin Short	7-8 pin Short	
AINL3/ AINR3	Open	Open	5-6 pin Short	5-6 pin Short	
AINL4/ AINR4	Open	Open	3-4 pin Short	3-4 pin Short	
AINL5/ AINR5	Open	Open	9-10 pin Short	9-10 pin Short	
AINL6/ AINR6	Open	Open	11-12 pin Short	11-12 pin Short	
AINL7/ AINR7	Open	Open	13-14 pin Short	13-14 pin Short	
AINL8/ AINR8	Open	Open	15-16 pin Short	15-16 pin Short	

Table 3. Setting of input when using AIN1L/AIN1R

Input Pin	JP16	JP17	
AINL2/ AINR2	7-8 pin Short	7-8 pin Short	Default
AINL3/ AINR3	5-6 pin Short	5-6 pin Short	
AINL4/ AINR4	3-4 pin Short	3-4 pin Short	
AINL5/ AINR5	9-10 pin Short	9-10 pin Short	
AINL6/ AINR6	11-12 pin Short	11-12 pin Short	
AINL7/ AINR7	13-14 pin Short	13-14 pin Short	
AINL8/ AINR8	15-16 pin Short	15-16 pin Short	

Table 4. Setting of input when using AIN2L/AIN2R

Input Pin	JP18	
AIN MONO	Short	Default

Table 5. Setting of input when using AIN MONO

■ Analog Output Circuit

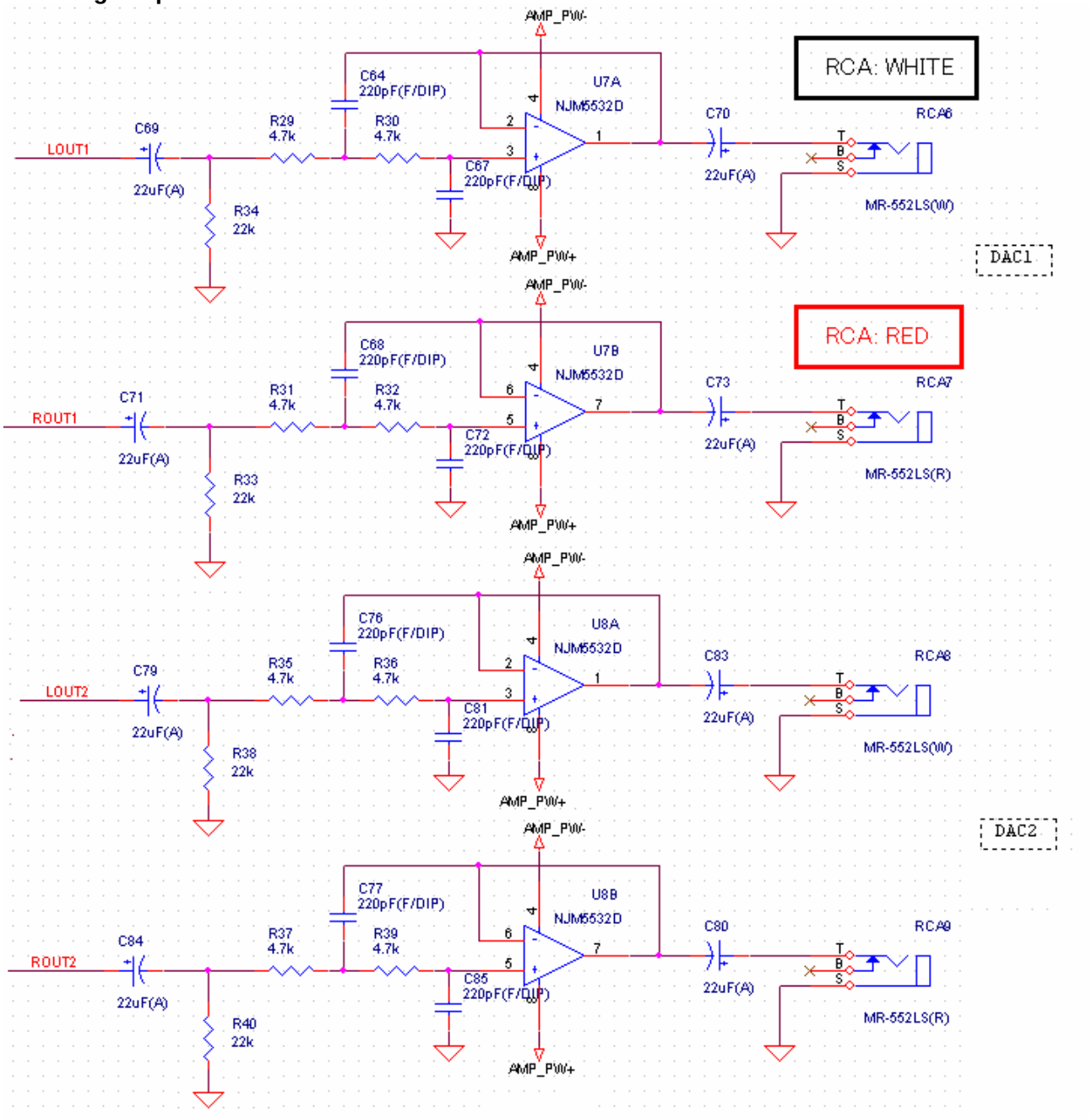


Figure 6. DAC1, DAC2 Analog Output Circuit

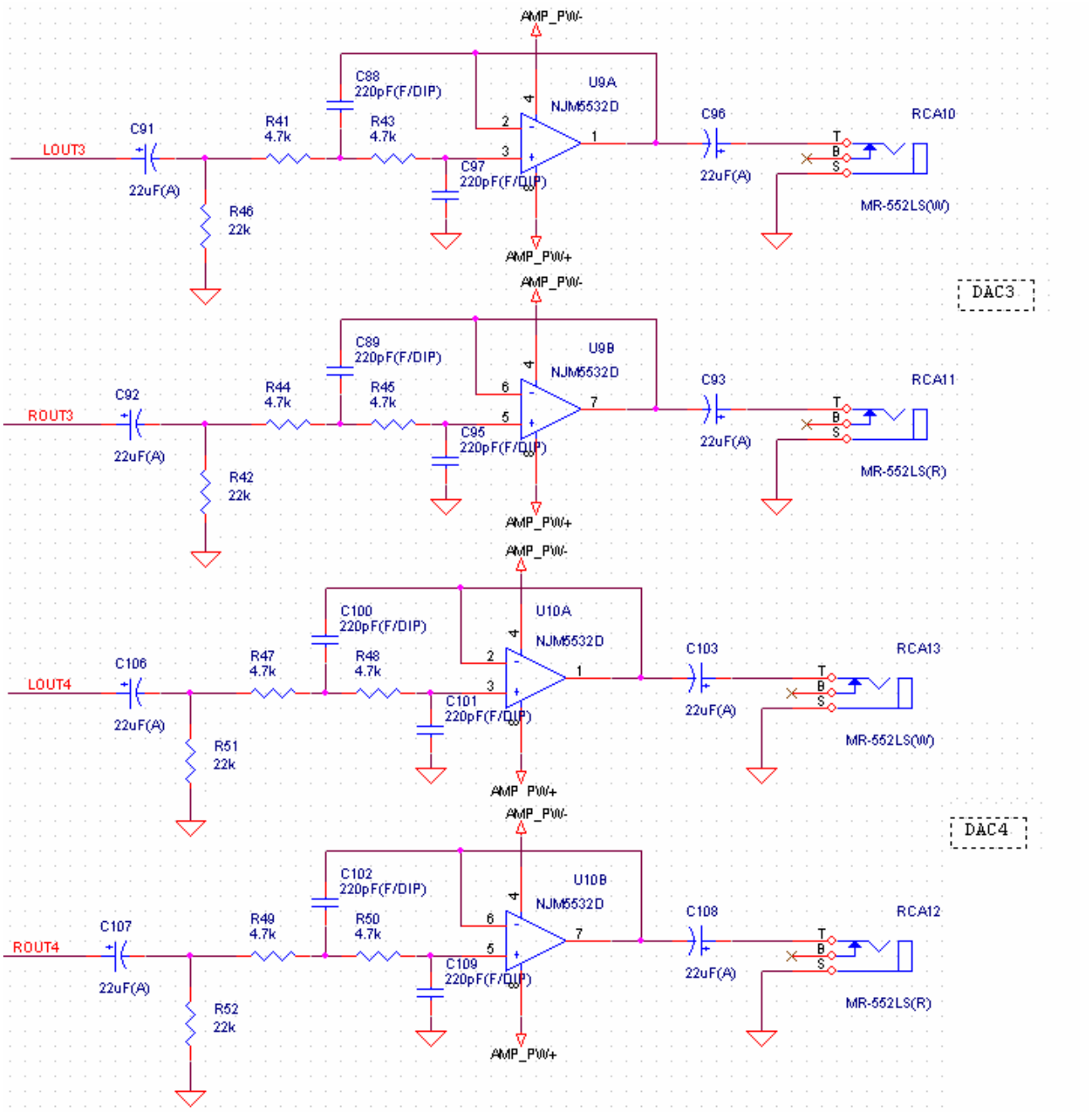


Figure 7. DAC3, DAC4 Analog Output Circuit

There is no DAC within AK7780. So 8ch DAC AK4359 is equipped on board.
For analog output, connector RCA6(DAC1L), RCA7(DAC1R), RCA8(DAC2L), RCA9(DAC2R), RCA10(DAC3L), RCA11(DAC3R), RCA13(DAC4L), RCA12(DAC4R) are available.

■ **Digital Input Circuit (External DIR:PORT1)**

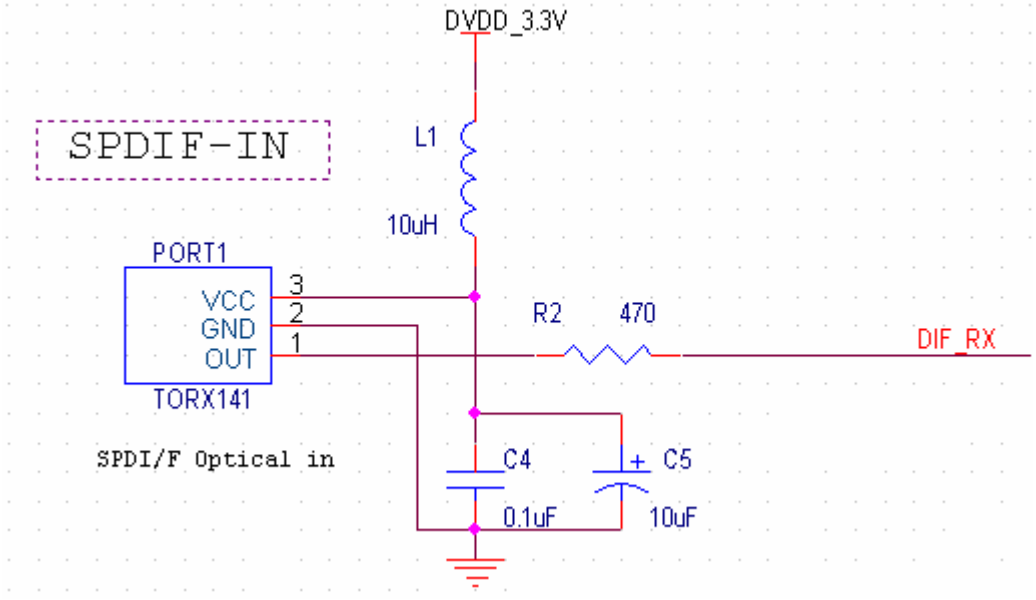


Figure 8. Digital Input Circuit (AK4114)

For digital input, optical connector PORT1 is available.

■ **Digital output circuit (External DIT:PORT2)**

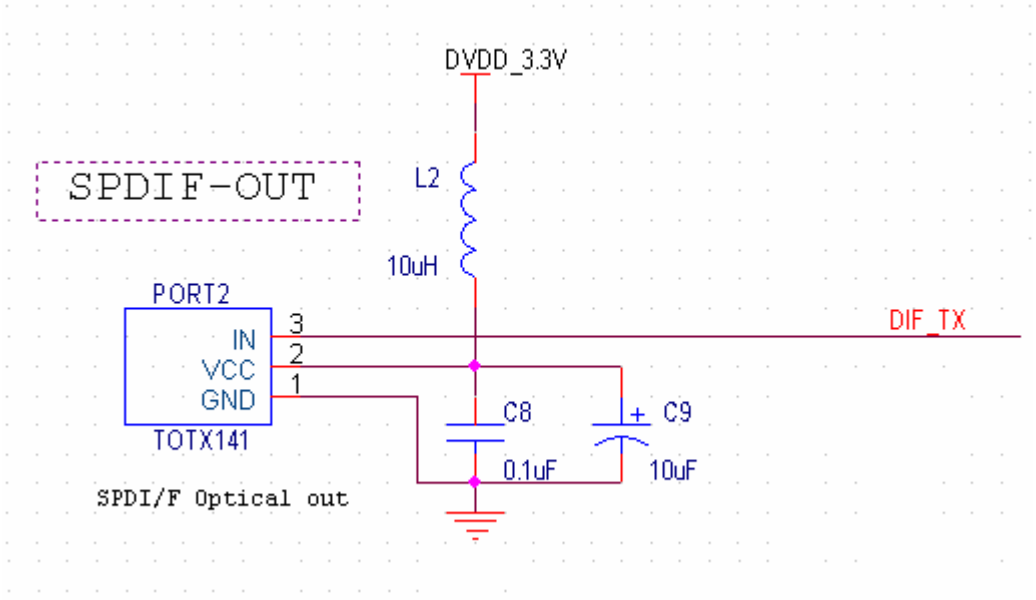


Figure 9. Digital Output Circuit (AK4114)

For digital output, optical connector PORT2 is available.

Control Software Manual

■ Set-up of the evaluation board and control software

1. Set up the AKD7780 according to previous term.

2. Connect IBM-AT compatible PC with AKD7780 by 25 pin printer cable (packed with AKD7780). (Please install the driver in the CD-ROM when software is used on Window 2000/XP. Please refer “Installation Manual of Control Software Driver by AKM device control software”. In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT. And the operation on Windows Vista has not been confirmed.)

3. Insert the CD-ROM labeled “AK7780 Evaluation Kit” into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of “AK7780.exe” to set up the program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow

1. Set up the control program according to the explanation above.
2. Click “Board Init” button to initialize the board.
3. Select the needed dialogue to evaluate by changing the setting.

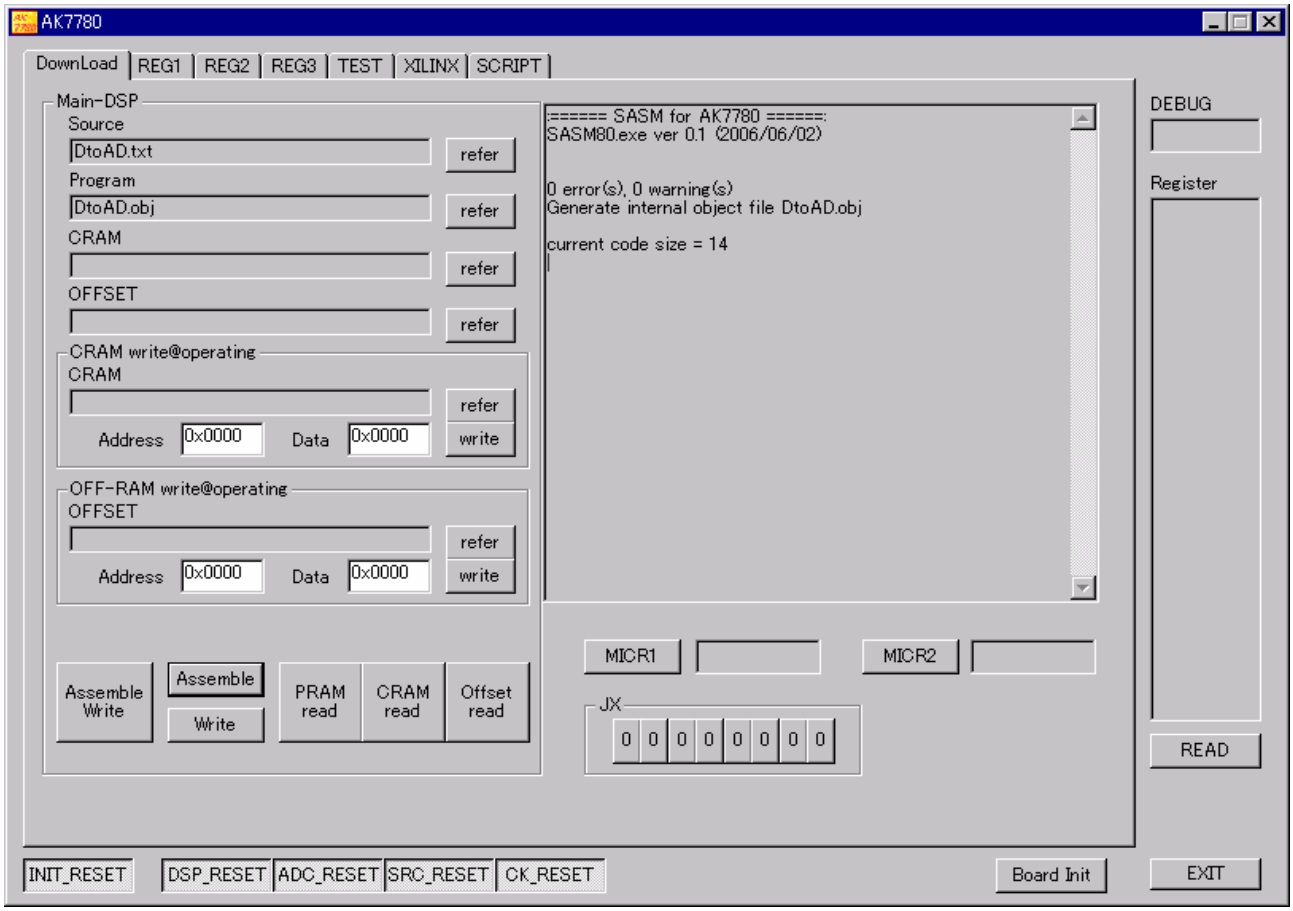


Figure 10. The image of control software

Control software supports program download, register setting, peripheral logic setting and running script. These menus are changing at upper tab. Frequent used function are placed outside of main menu.

(1) Download

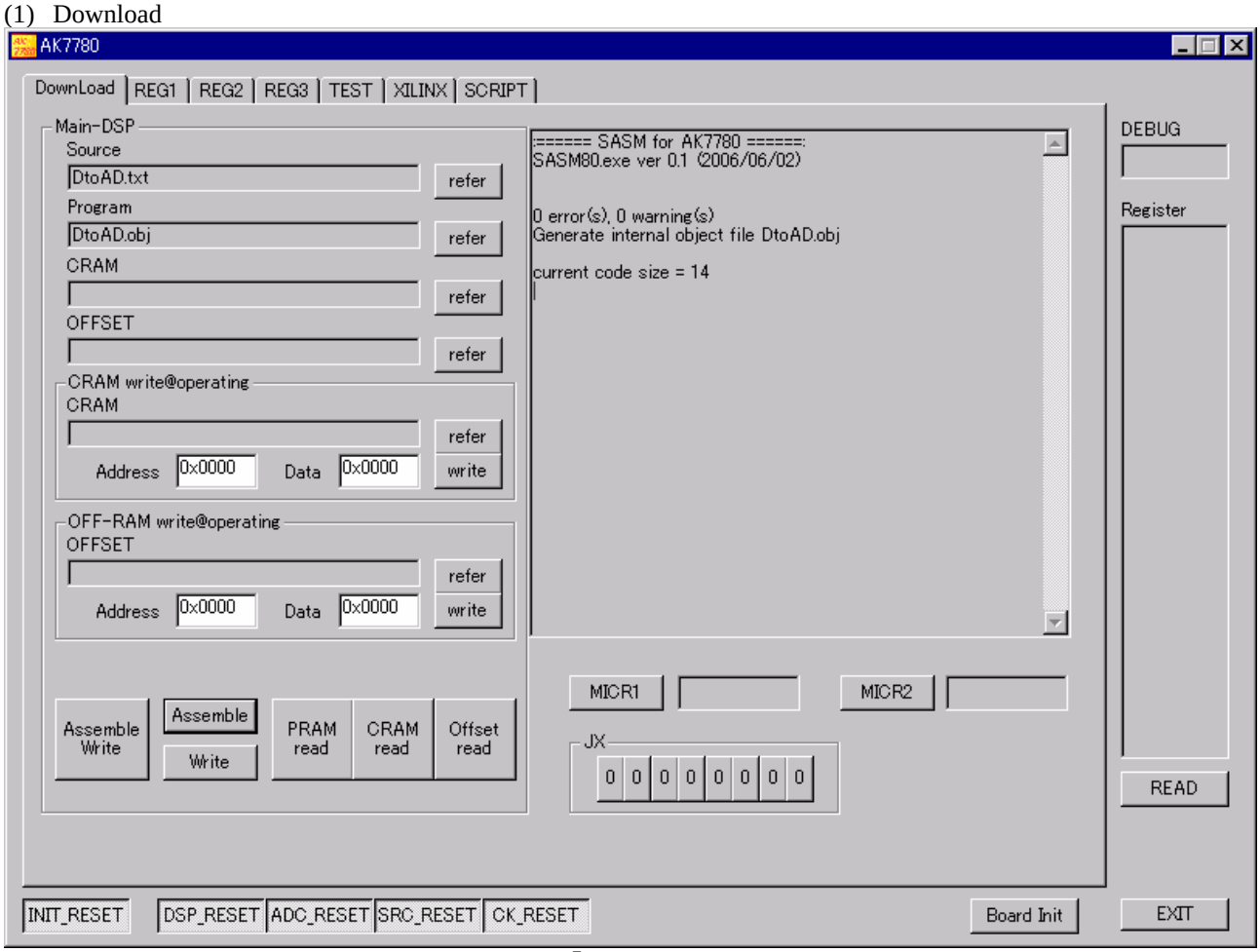


Figure 11. 「Download」 Dialogue

Push “Refer” button at source item and select source file.
And then, push “Assemble” button, Assembler runs and outputs result. Automatically assembled file is selected as a PRAM file. Push “Write” button, download process is done.
“Assemble Write” button do all of this process.

In this menu, read back of download data, SO-read function, JX setting, CRAM/OFRAM writing under operation are supported.

(2) Register Setting

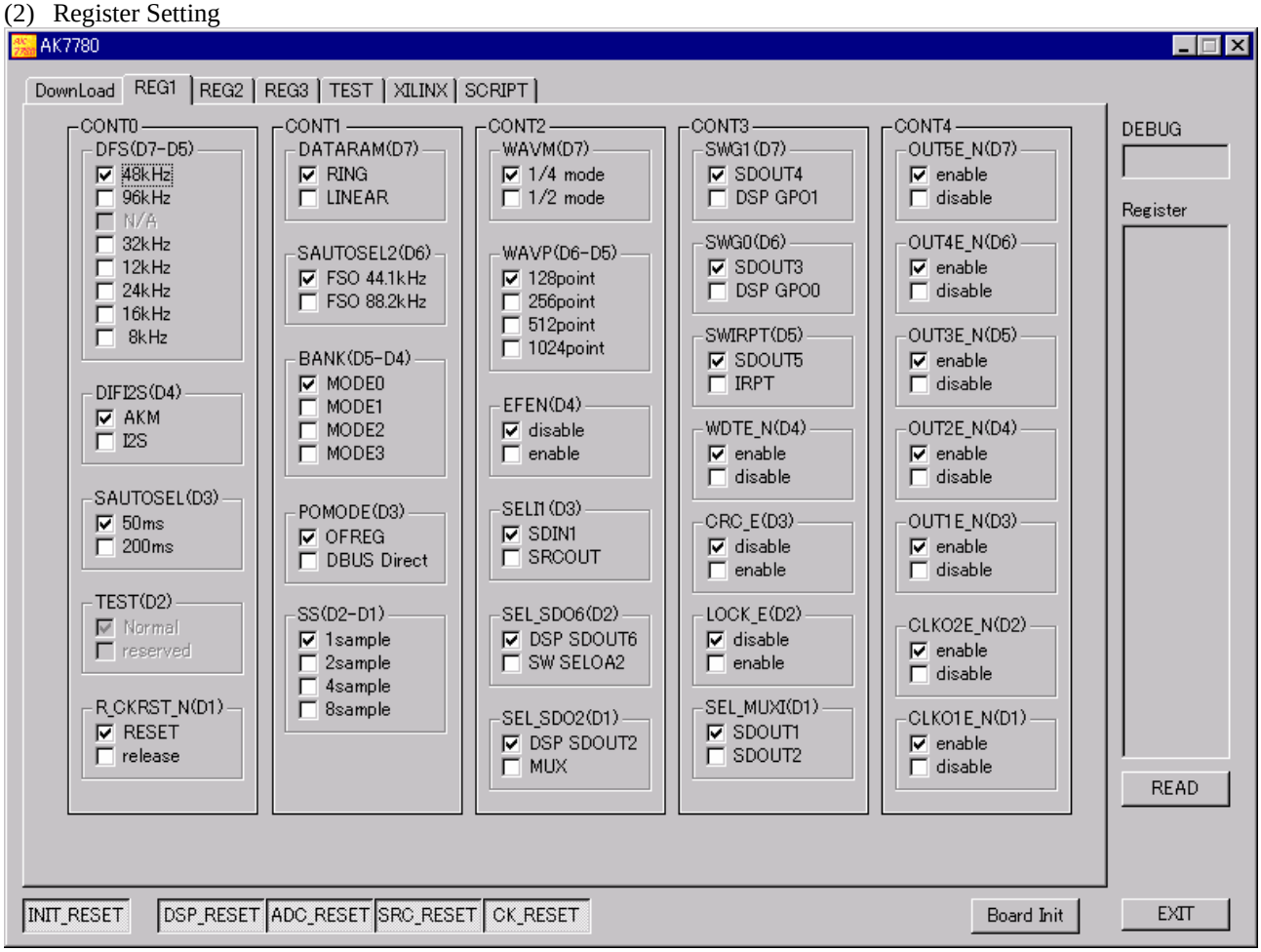


Figure 12. 「REG1」 Dialogue

REG1/REG2/REG3/TEST tabs are register setting window. (Test items are inactivated.)
Check each button and control software will write to each AK7780 register. When accessing to CONT0 register, DSR_RESET will automatically to L.

The reference page of registers in datasheet is as follow:

Register	Reference Page		Register	Reference page
CONT00	31		CONT07	38
CONT01	32		CONT08	39
CONT02	33		CONT09	40
CONT03	34		CONT0A	41
CONT04	35		CONT0B	42
CONT05	36		CONT0C	43
CONT06	37		CONT0D	44

Table 6. Reference page of registers

(3) Peripheral logic setting

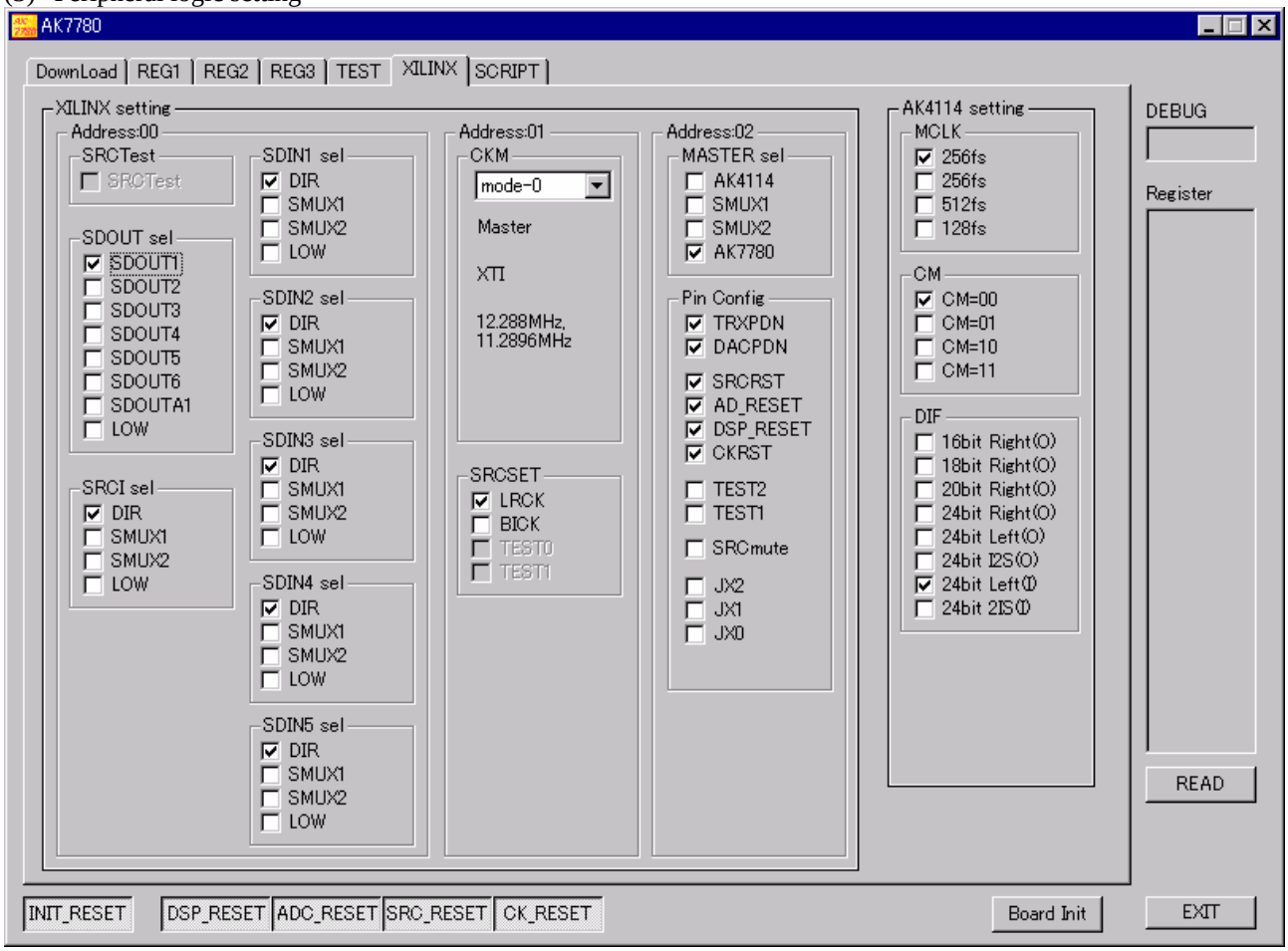


Figure 13. 「XILINX」 Dialogue

In this menu, Path Controller and AK4114 setting are supported. AK7780 is set to master mode and other devices are set to slave mode after start up.

(4) Script

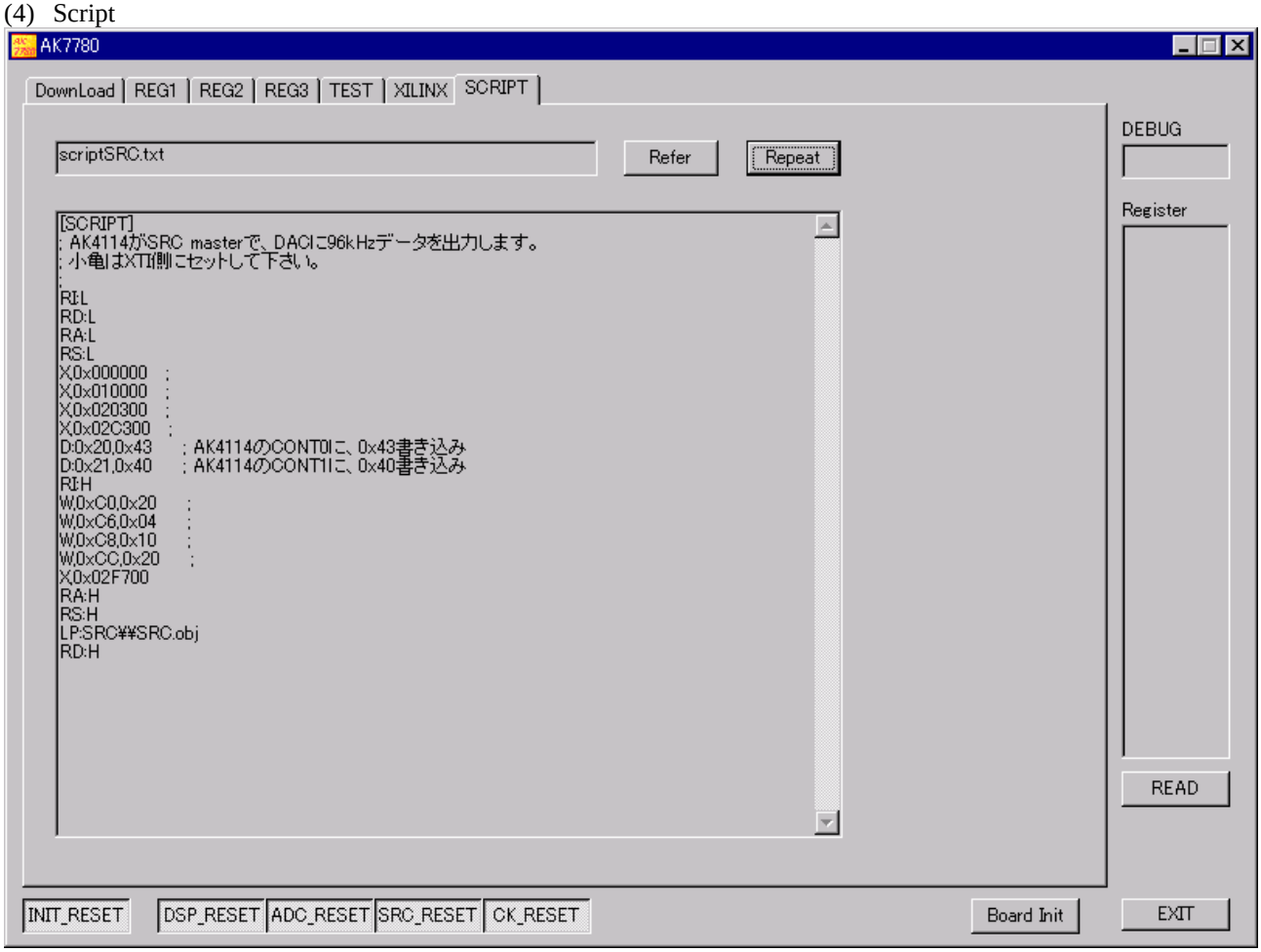


Figure 14. 「Script」 Dialogue

Select script file and runs. “Repeat” button runs current selected script once again.

Command	Description
[SCRIPT]	Script file header. If this header is missing, Header error will occur.
;comment	After semi-colon sentence will be ignored as comment.
W,<address>,<data> W,0xC0,0x00	AK7780 register access.
WL,<command>,<address>,<data>,… WL,0x82,0x0022,0x4000,0x4000,0x4000	AK7780 continuous data access. This is possible to use CRAM access in operating. Command data is byte, following data are word length.
D,<address>,<data>	AK4114 register access.
X,<address>,<data>	FPGA register access.
P,<message>	Display any message, and suspend script process.
RI:H / RI:L RS:H / RS:L RA:H / RA:L RD:H / RD:L RC:H / RC:L	AK7780 reset control. INIT_RESET, SRC_RESET, ADC_RESET, DSP_RESET and CK_RESET.
T,<wait> T,50mS	Wait script process. Unit is mS only.
LP:<filename>	Download PRAM data
LC:<filename>	Download CRAM data
LO:<filename>	Download OFFSET RAM data

Table 7. Script command

■ How to use

(1) D-to-D
Digital to Digital loop back. The AK4114 is master device, and the AK7780 operates in slave mode.
Please confirm that JP1 of main board is **XTL** side and JP5 of daughter board is **EXT** side.

(a) After starting up, Push “Board Initialize” button.
(b) Select SCRIPT tab, and runs scriptMASTER.txt.
(c) Push “refer” button and select DtoAD.txt file.
(d) Push “Assemble Write” button.

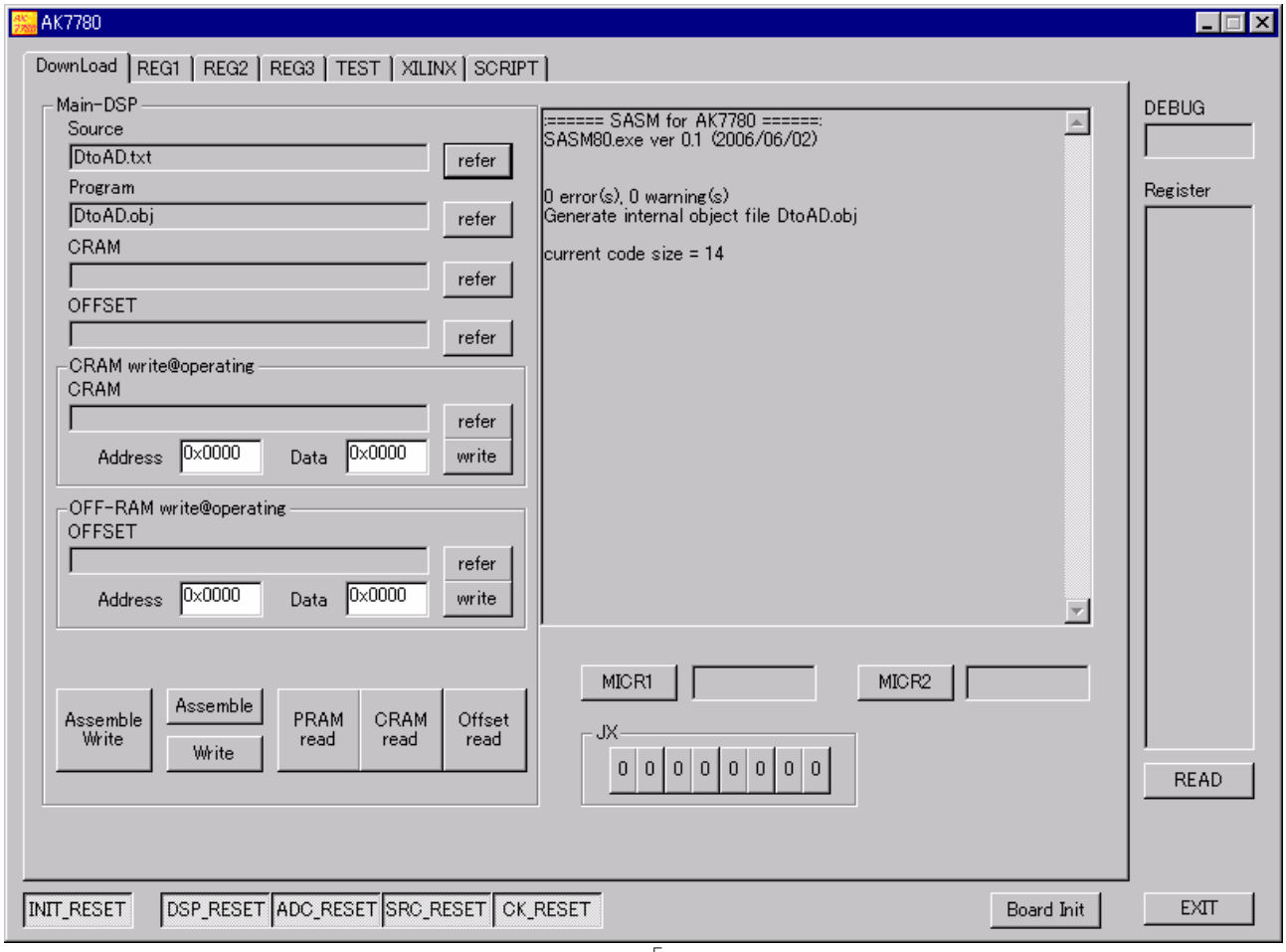


Figure 15. 「D-to-D」

(2) SRC operation confirmation

The AK4114 is the master device of SRC, and the AK7780 operates as master device with crystal oscillation. Input data from optical terminal goes via SRC, and DSP output will go to DAC at fs=96kHz.
Please confirm that JP1 of main board is **XTL** side and JP5 of daughter board is **XTL** side.

(a) After starting up, Push “Board Initialize” button.
(b) Select SCRIPT tab, and runs scriptSRC.txt.

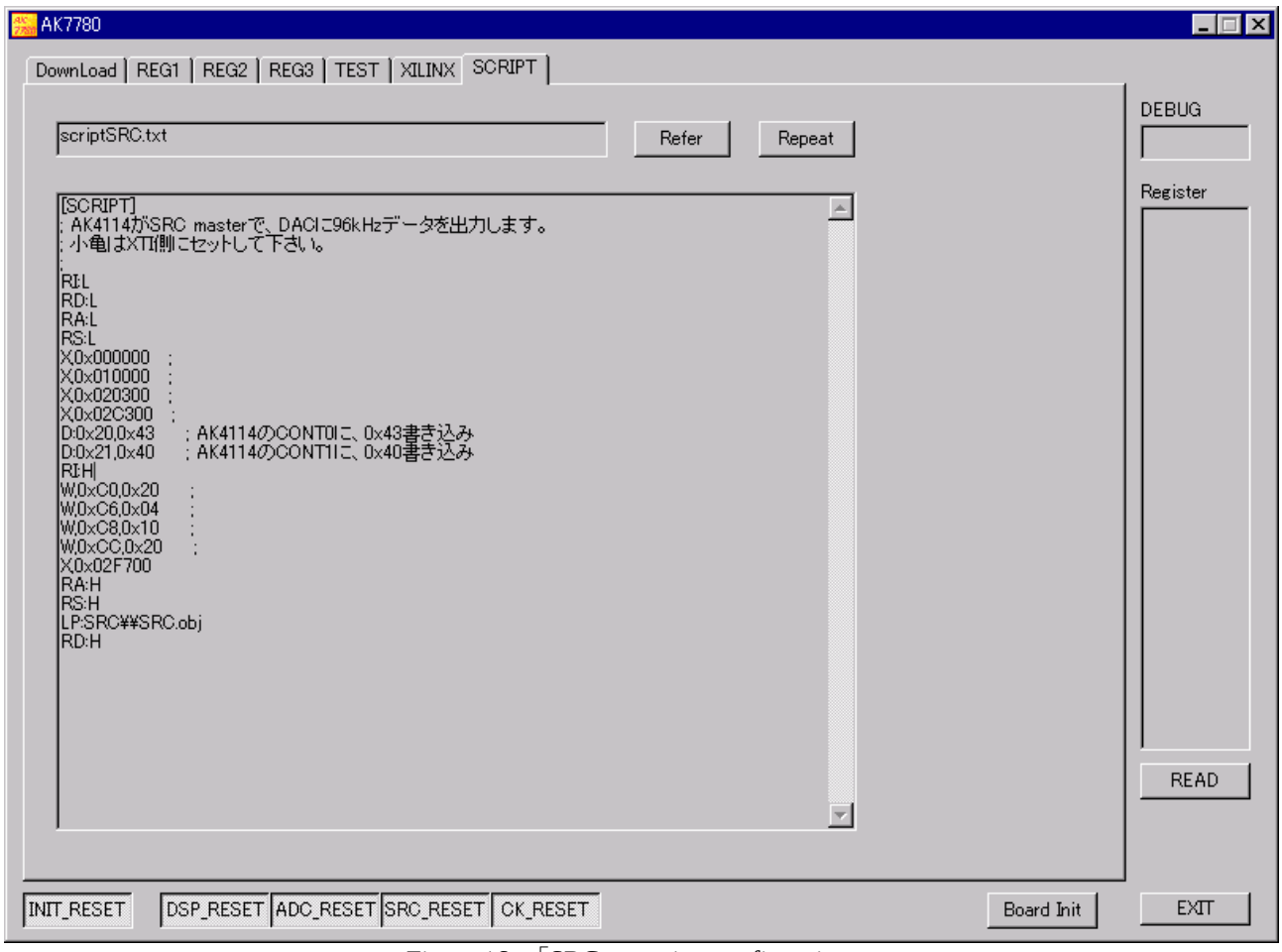
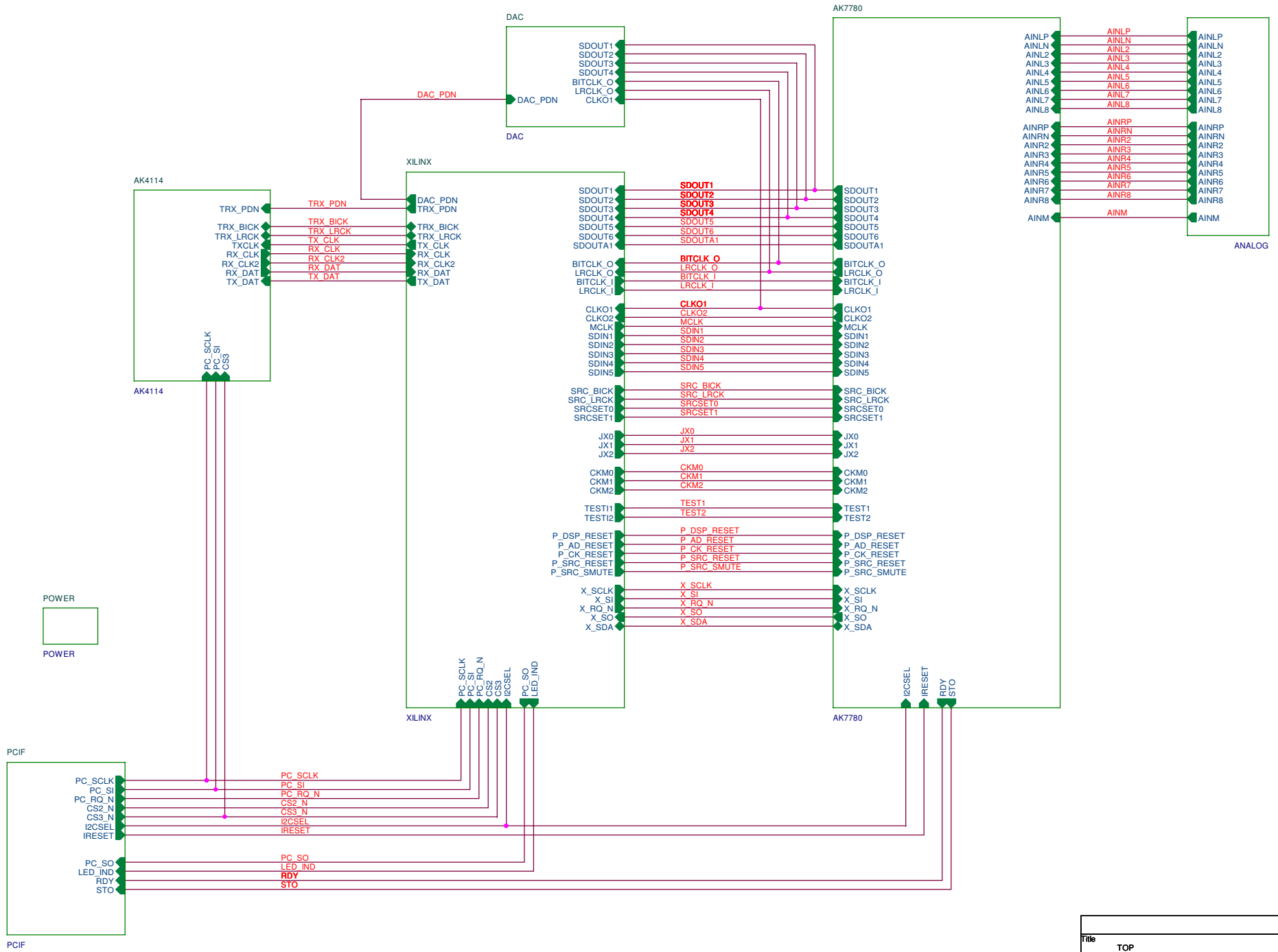


Figure 16. 「SRC operation confirmation」

This script file will set each register setting, and download SRC.obj automatically (SRC.obj is SRC-to-DSP output through program).

REVISION HISTORY

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
07/09/10	KM090600	0	First edition		


DAC
SDOUT1
SDOUT2
SDOUT3
SDOUT4
BITCLK_O
LRCLK_O
CLKO1
DAC_PDN
DAC_PDN
DAC
AK7780
AINLP
AINLN
AINL2
AINL3
AINL4
AINL5
AINL6
AINL7
AINL8
AINRP
AINRN
AINR2
AINR3
AINR4
AINR5
AINR6
AINR7
AINR8
AINM
ANALOG
AK4114
TRX_PDN
TRX_BICK
TRX_LRCK
TXCLK
RX_CLK
RX_CLK2
RX_DAT
TX_DAT
PC_SCLK
PC_SI
CS3
AK4114
XILINX
DAC_PDN
TRX_PDN
TRX_BICK
TRX_LRCK
TX_CLK
RX_CLK
RX_CLK2
RX_DAT
TX_DAT
SDOUT1
SDOUT2
SDOUT3
SDOUT4
SDOUT5
SDOUT6
SDOUTA1
BITCLK_O
LRCLK_O
BITCLK_I
LRCLK_I
CLKO1
CLKO2
MCLK
SDIN1
SDIN2
SDIN3
SDIN4
SDIN5
SRC_BICK
SRC_LRCK
SRCSET0
SRCSET1
JX0
JX1
JX2
CKM0
CKM1
CKM2
TESTI1
TESTI2
P_DSP_RESET
P_AD_RESET
P_CK_RESET
P_SRC_RESET
P_SRC_SMUTE
X_SCLK
X_SI
X_RQ_N
X_SO
X_SDA
PC_SCLK
PC_SI
PC_RQ_N
CS2
CS3
I2CSEL
PC_SO
LED_IND
XILINX
AK7780
I2CSEL
IRESET
RDY
STO
POWER
POWER
PCIF
PC_SCLK
PC_SI
PC_RQ_N
CS2_N
CS3_N
I2CSEL
IRESET
PC_SO
LED_IND
RDY
STO
PCIF
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TOP
Size
A3
Document Number
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Rev
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Date:
Friday, July 07, 2006
Sheet
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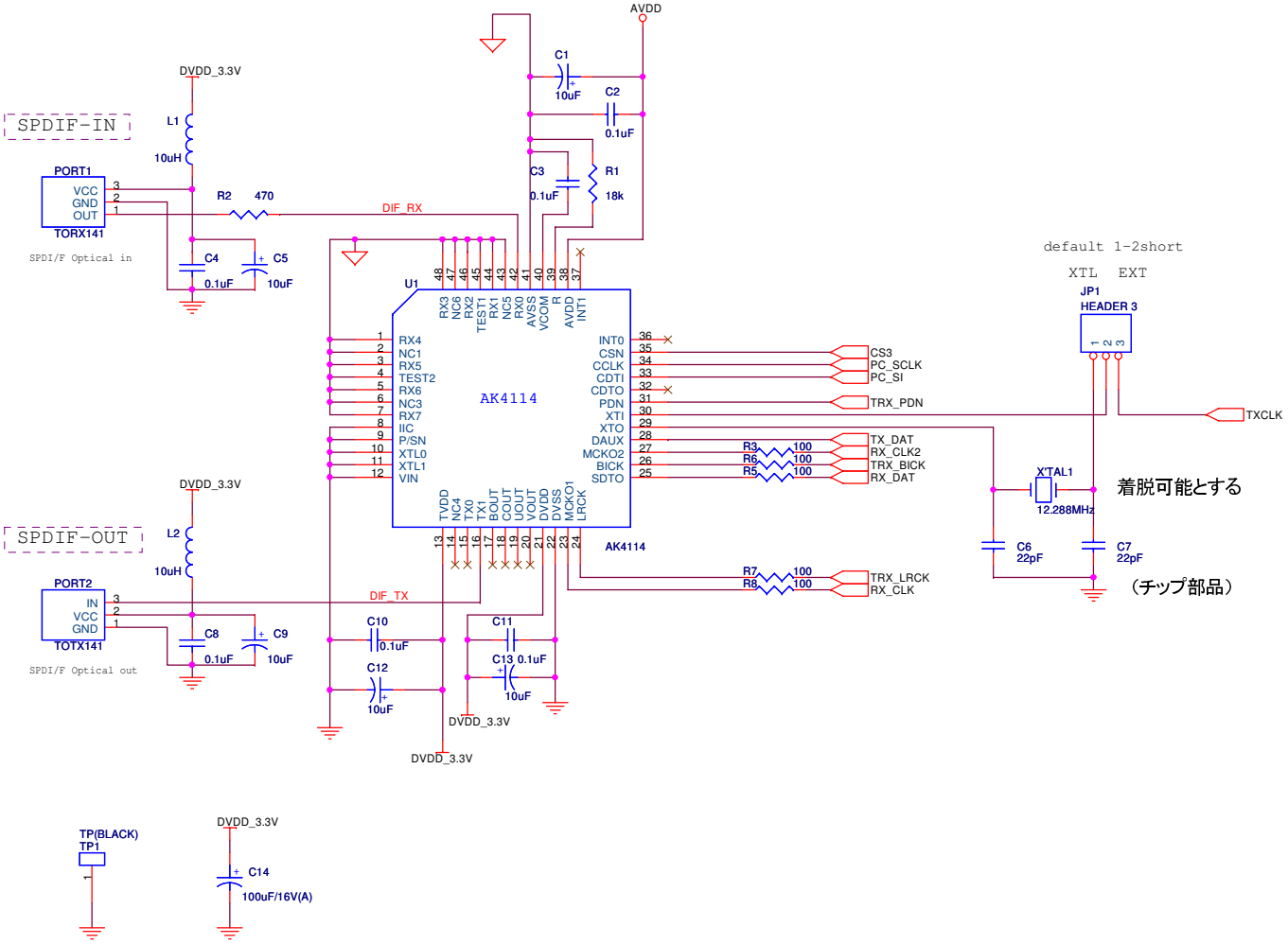
of
8



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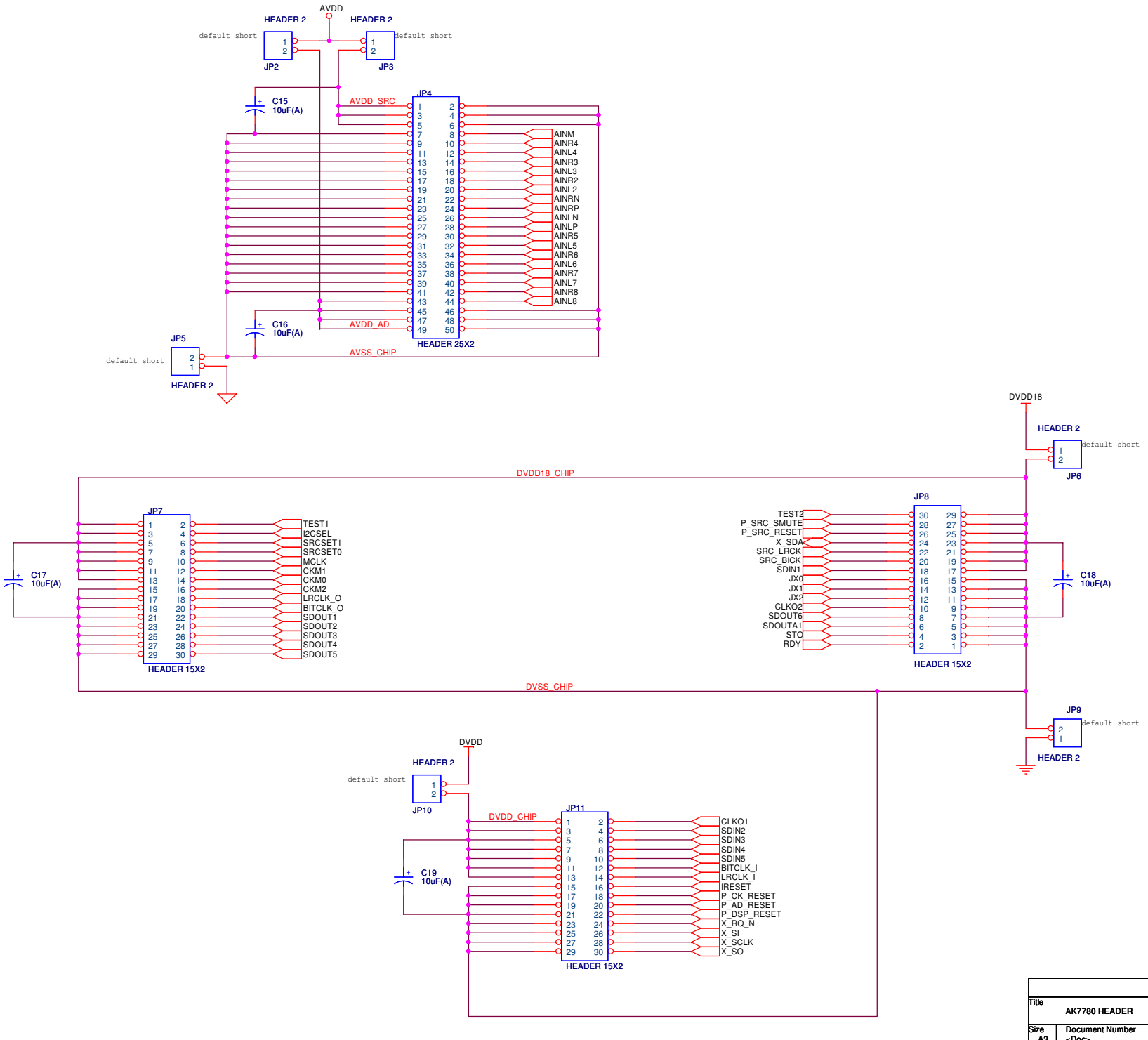

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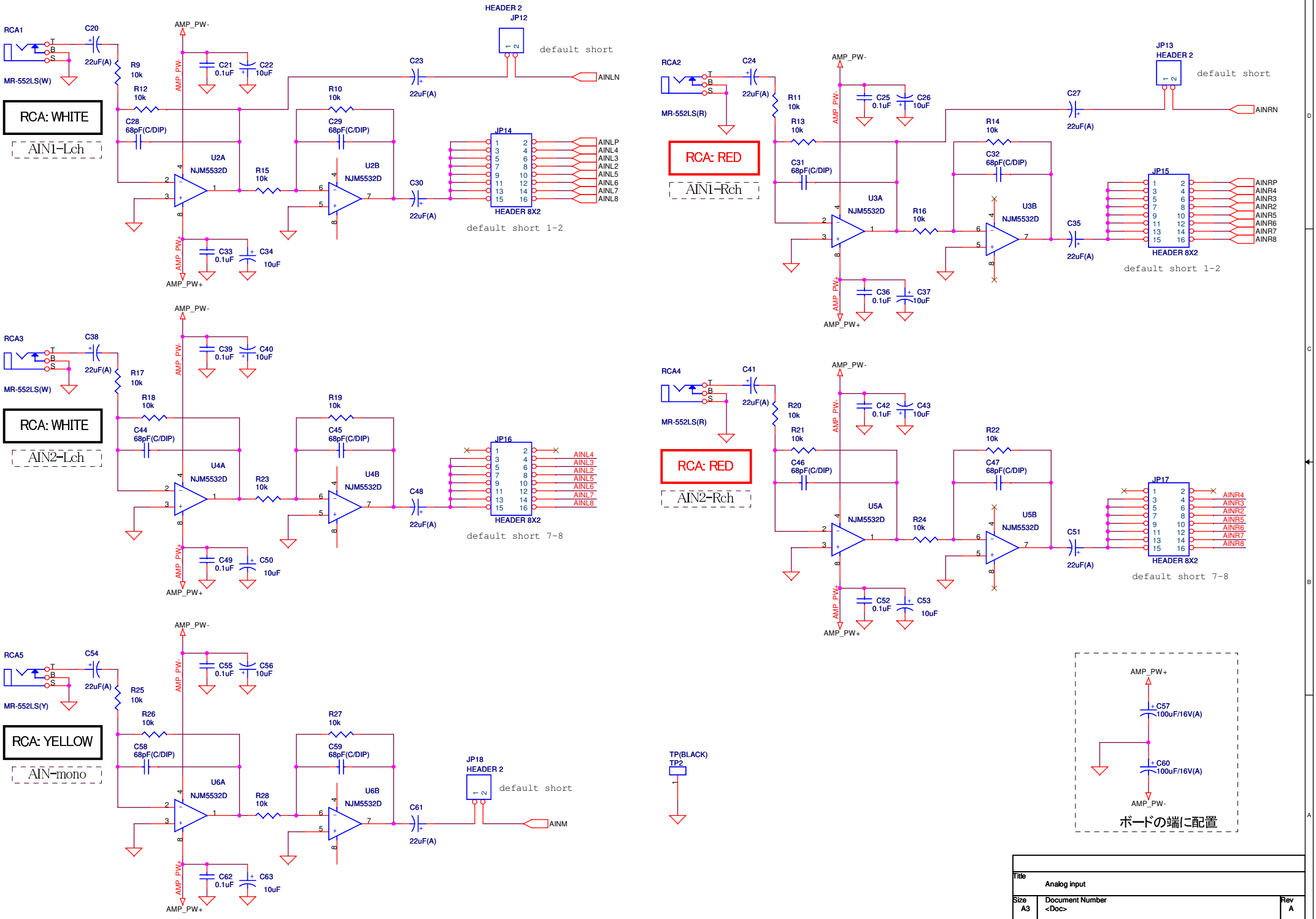
Date: Friday, July 07, 2006	Sheet 3 of 8	



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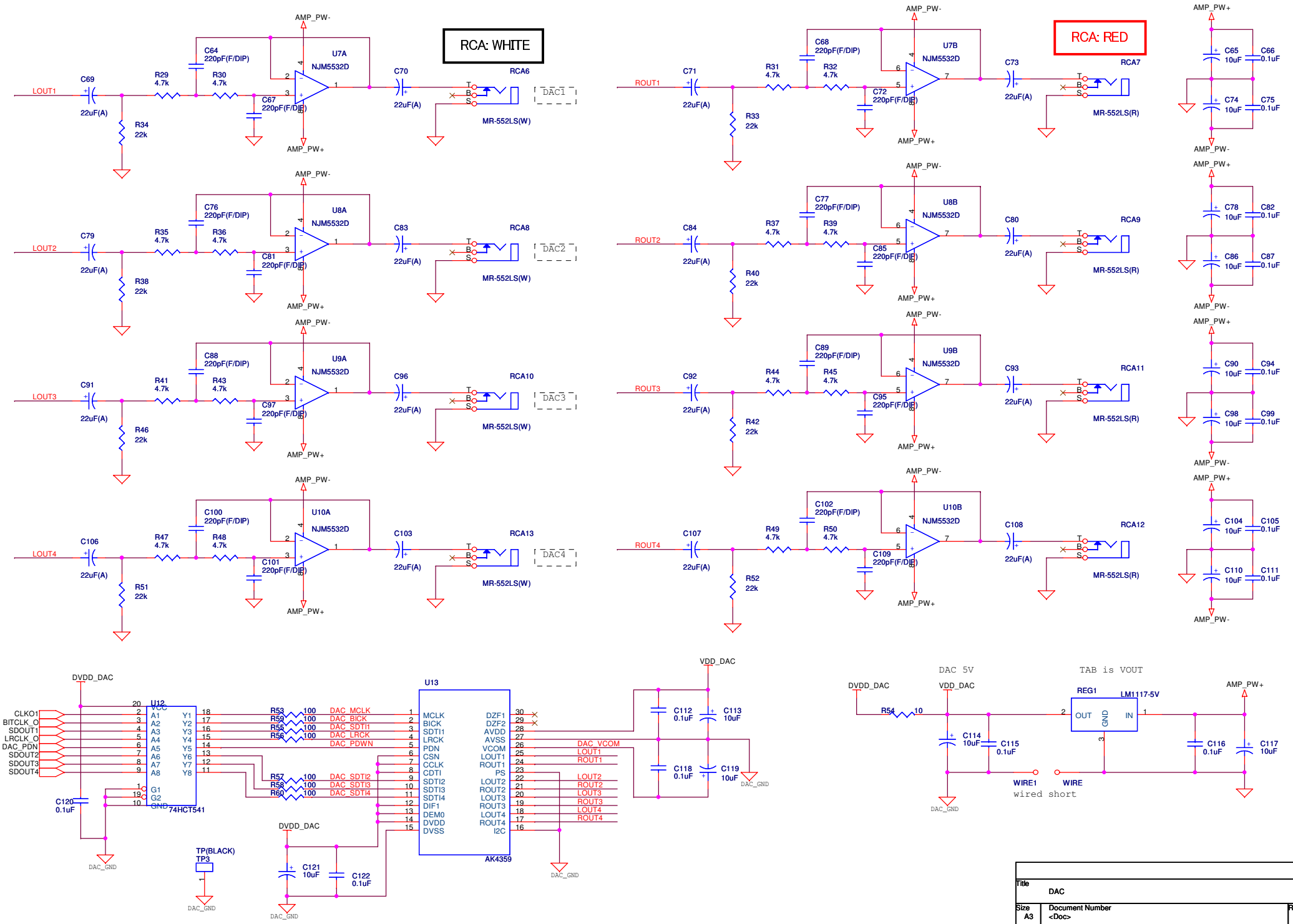
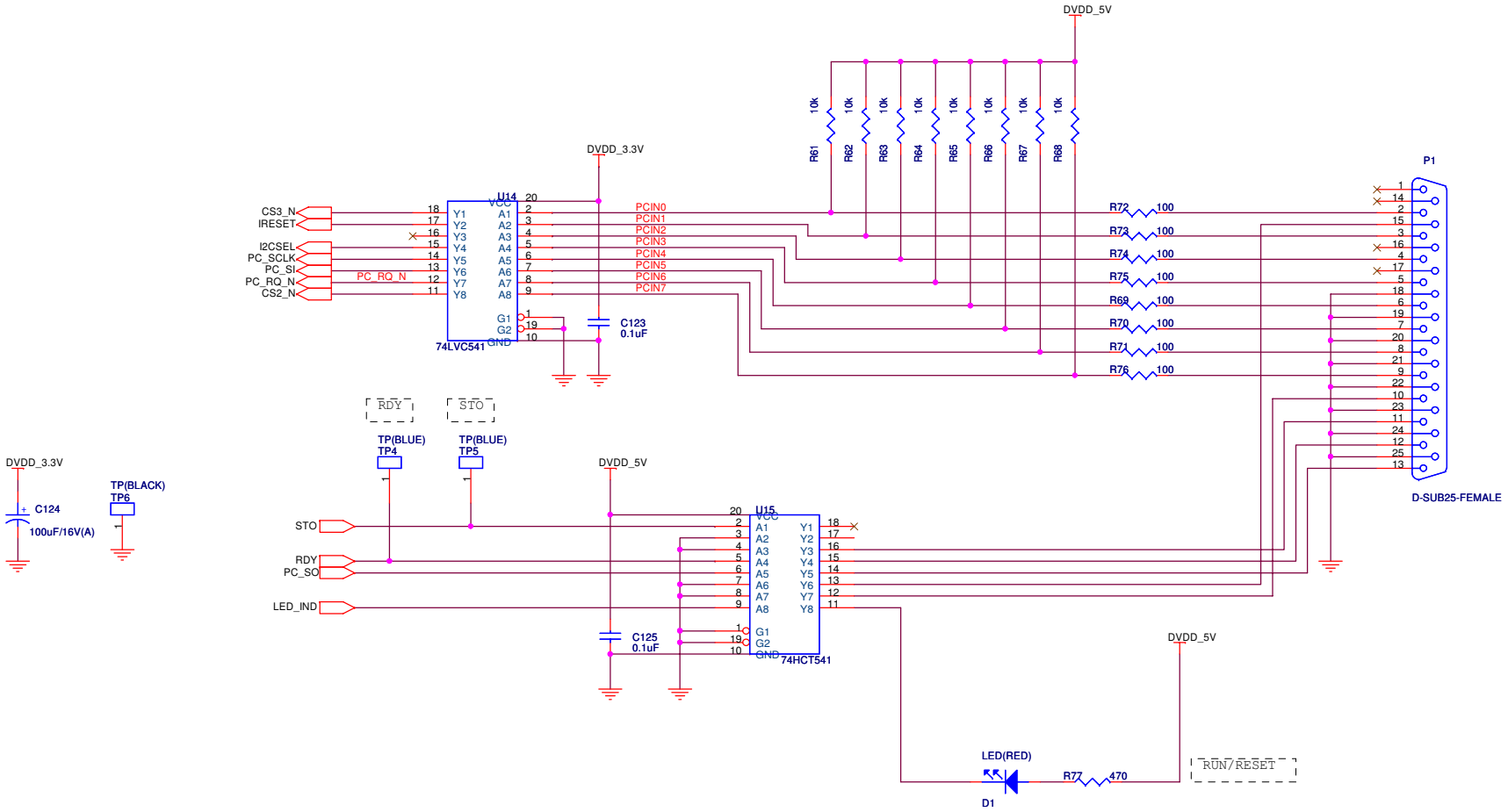
Size A3	Document Number <Doc>	Rev A
Date: Friday, July 07, 2006	Sheet 4 of 8	



Title	DAC	
Size A3	Document Number <Doc>	Rev A
Date: Thursday, July 06, 2006	Sheet 5 of 8	



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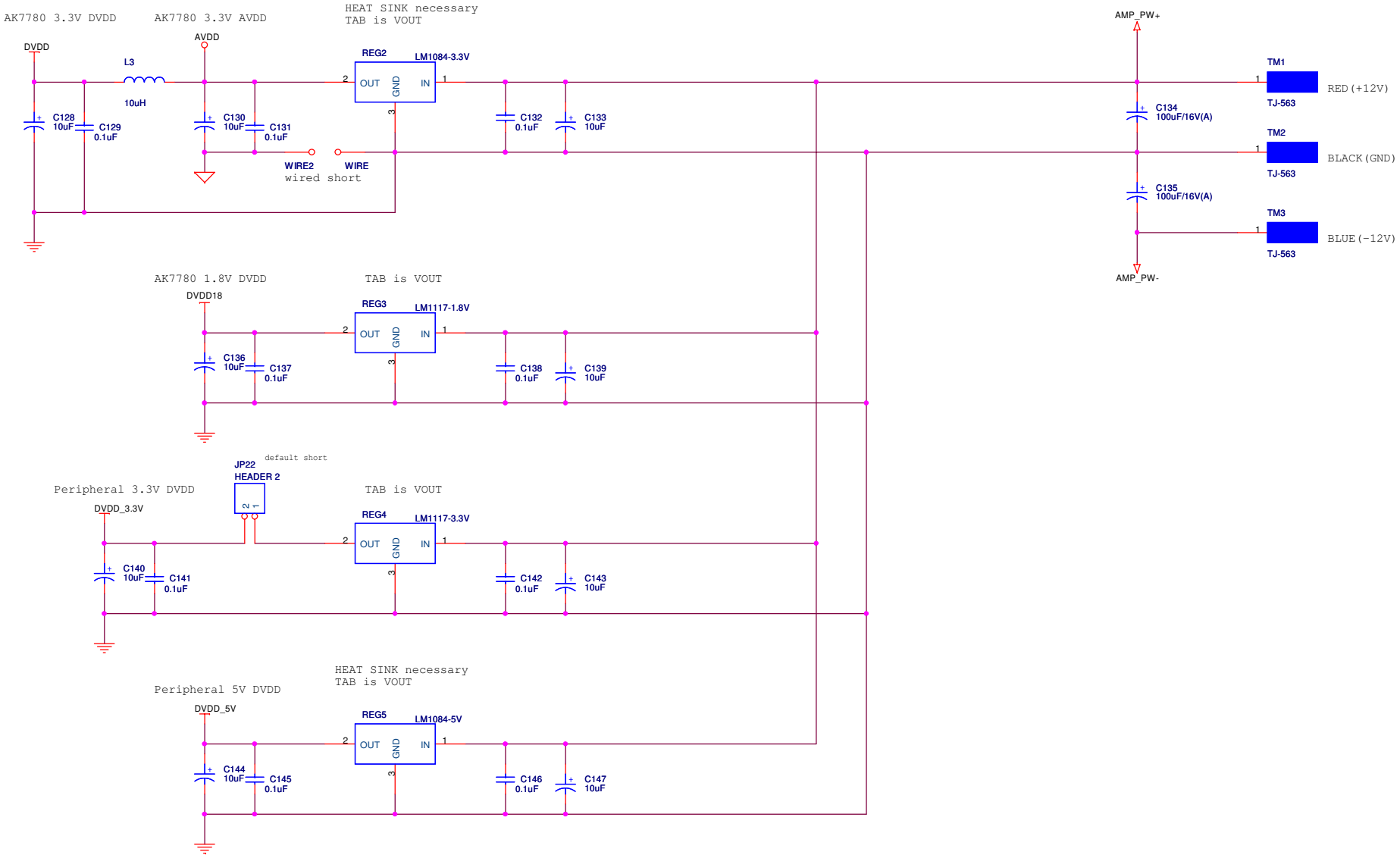
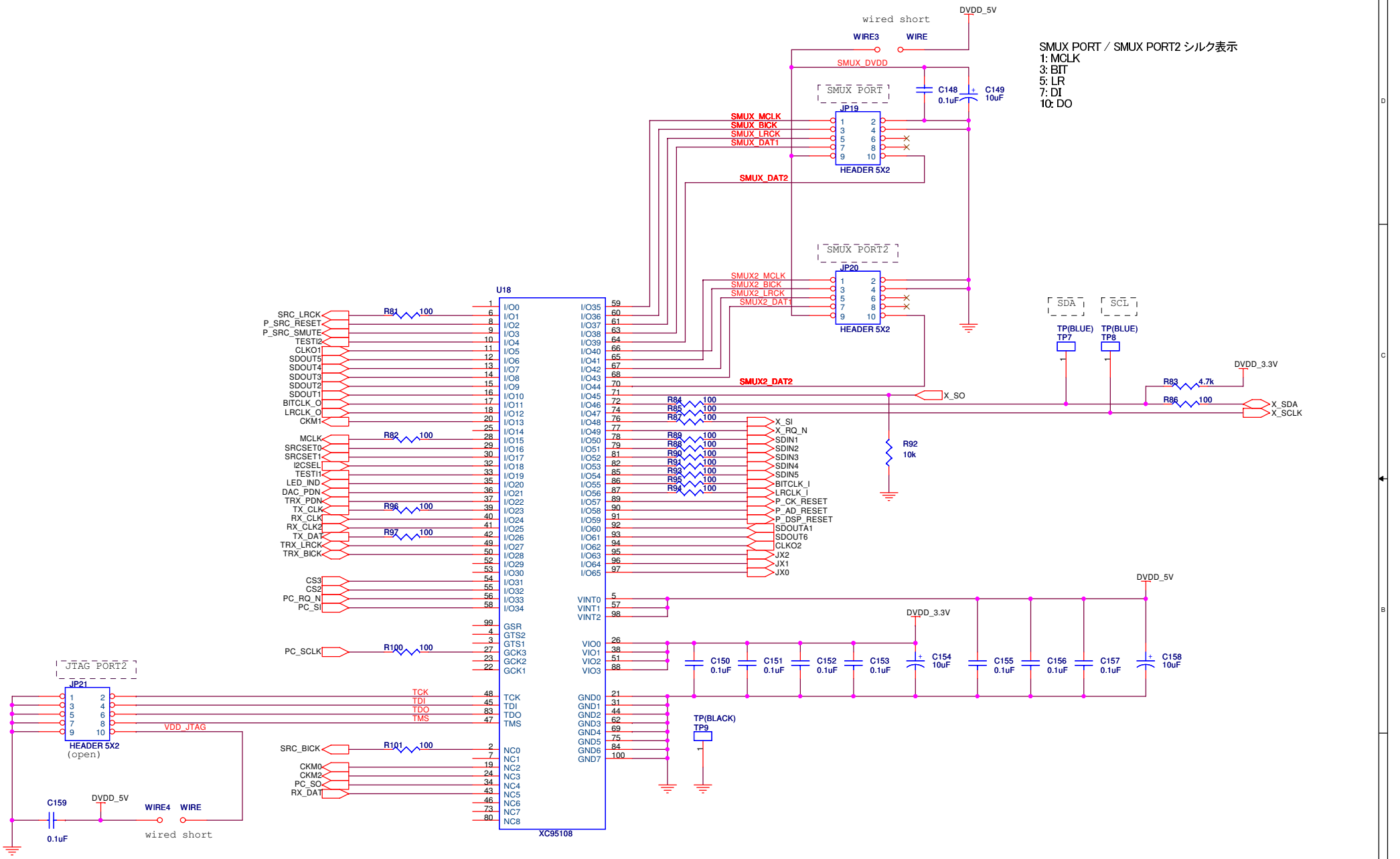
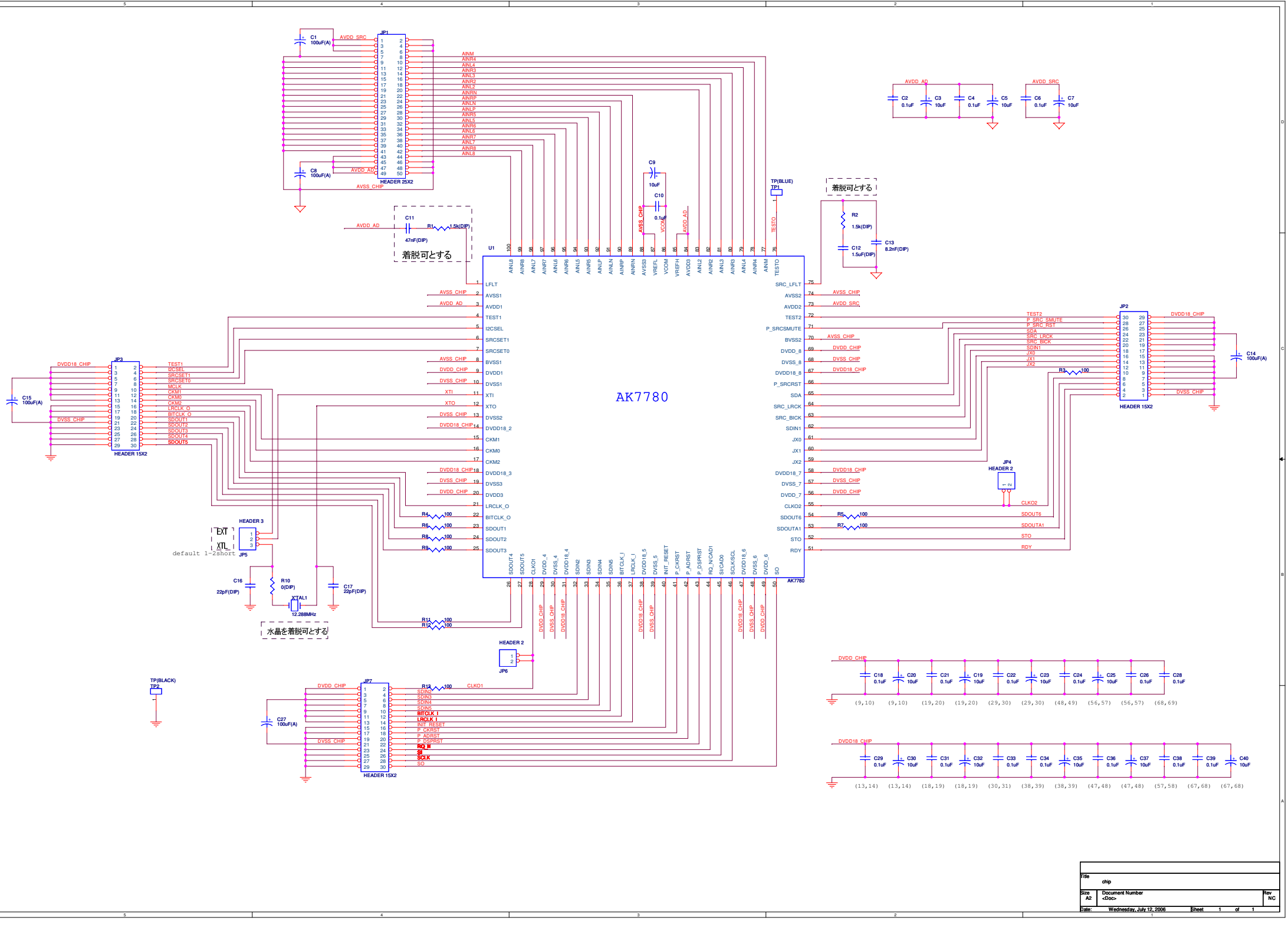
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Friday, July 07, 2006	Sheet 6 of 8	

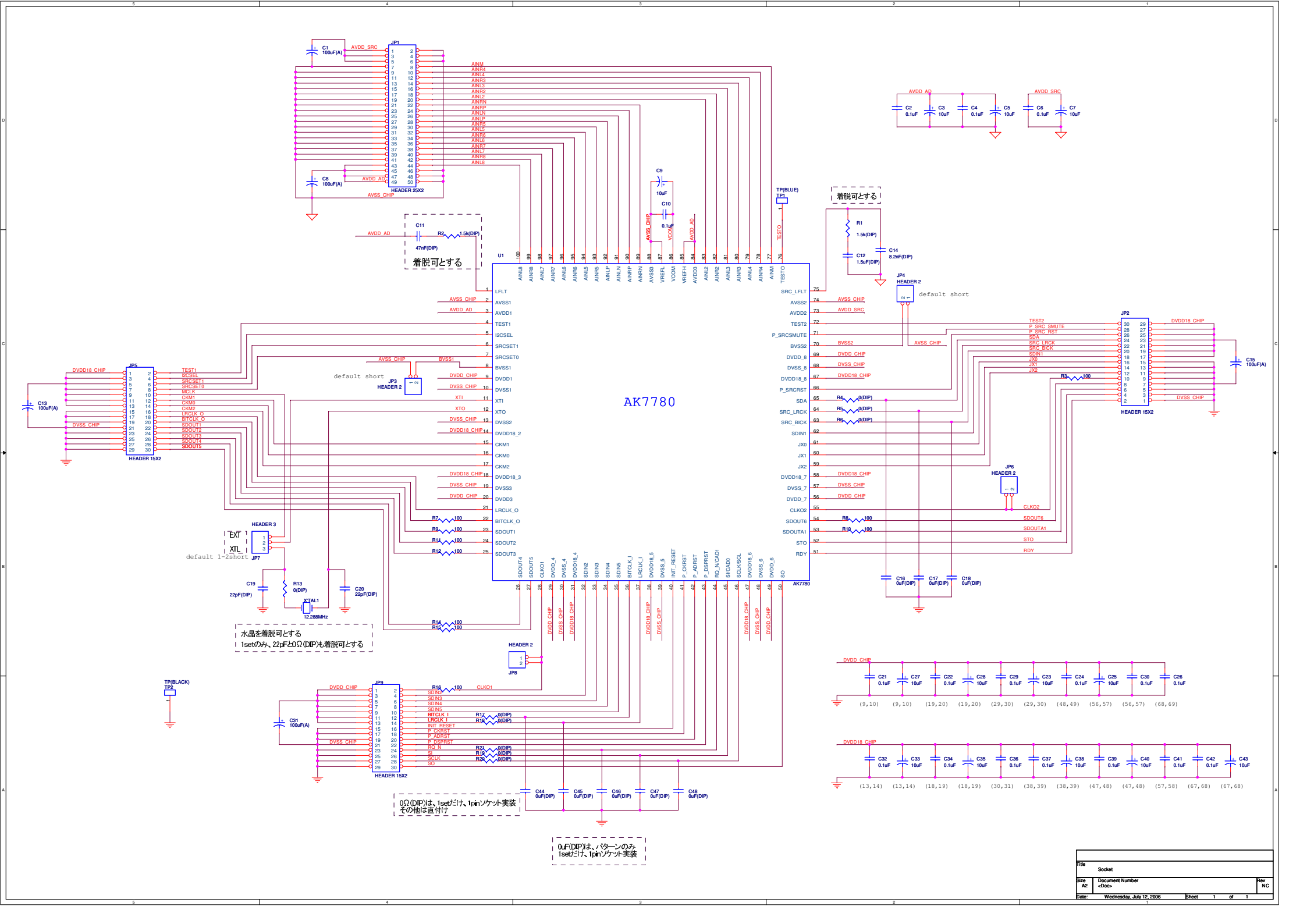


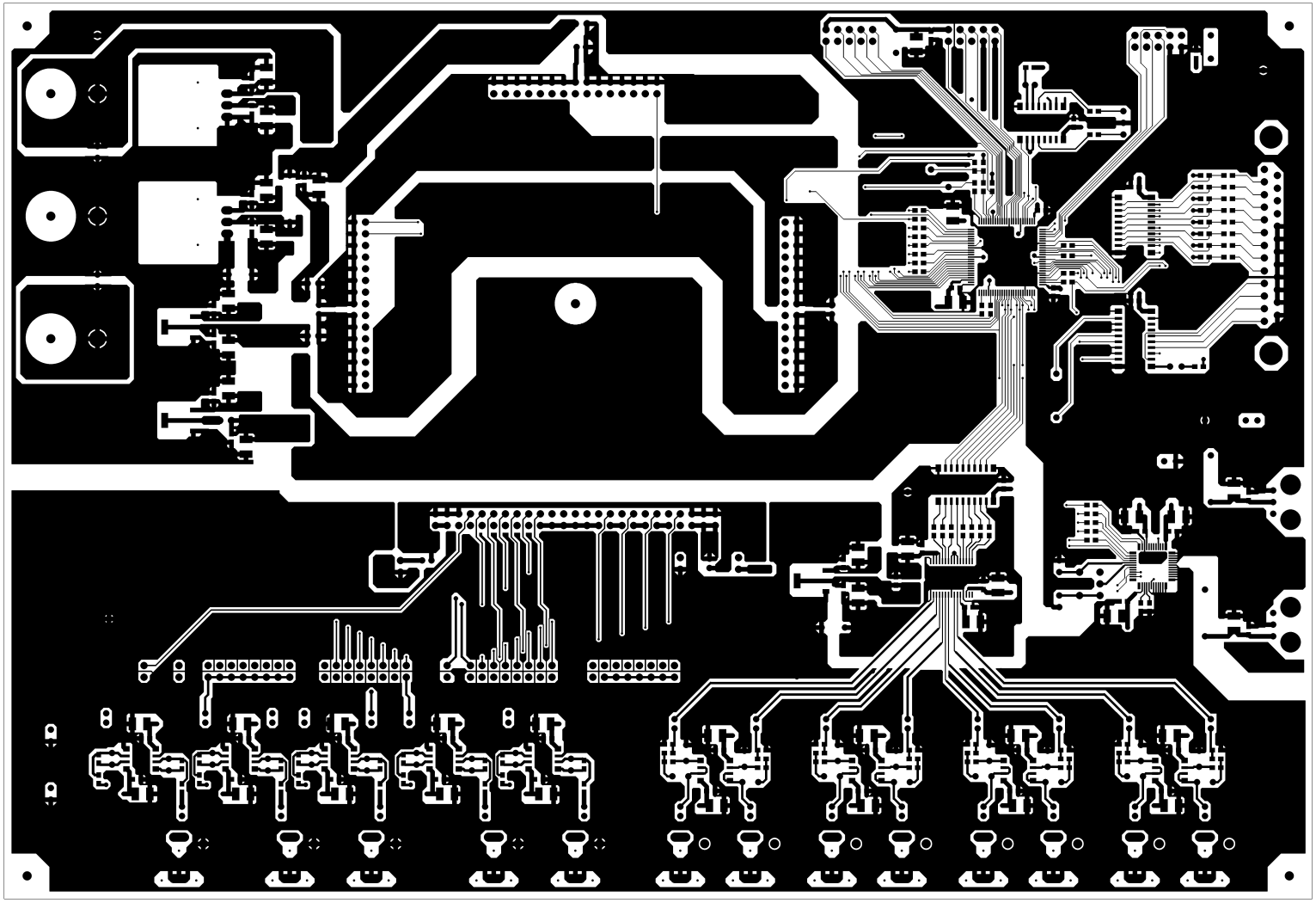
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, July 12, 2006	Sheet 7 of 8	



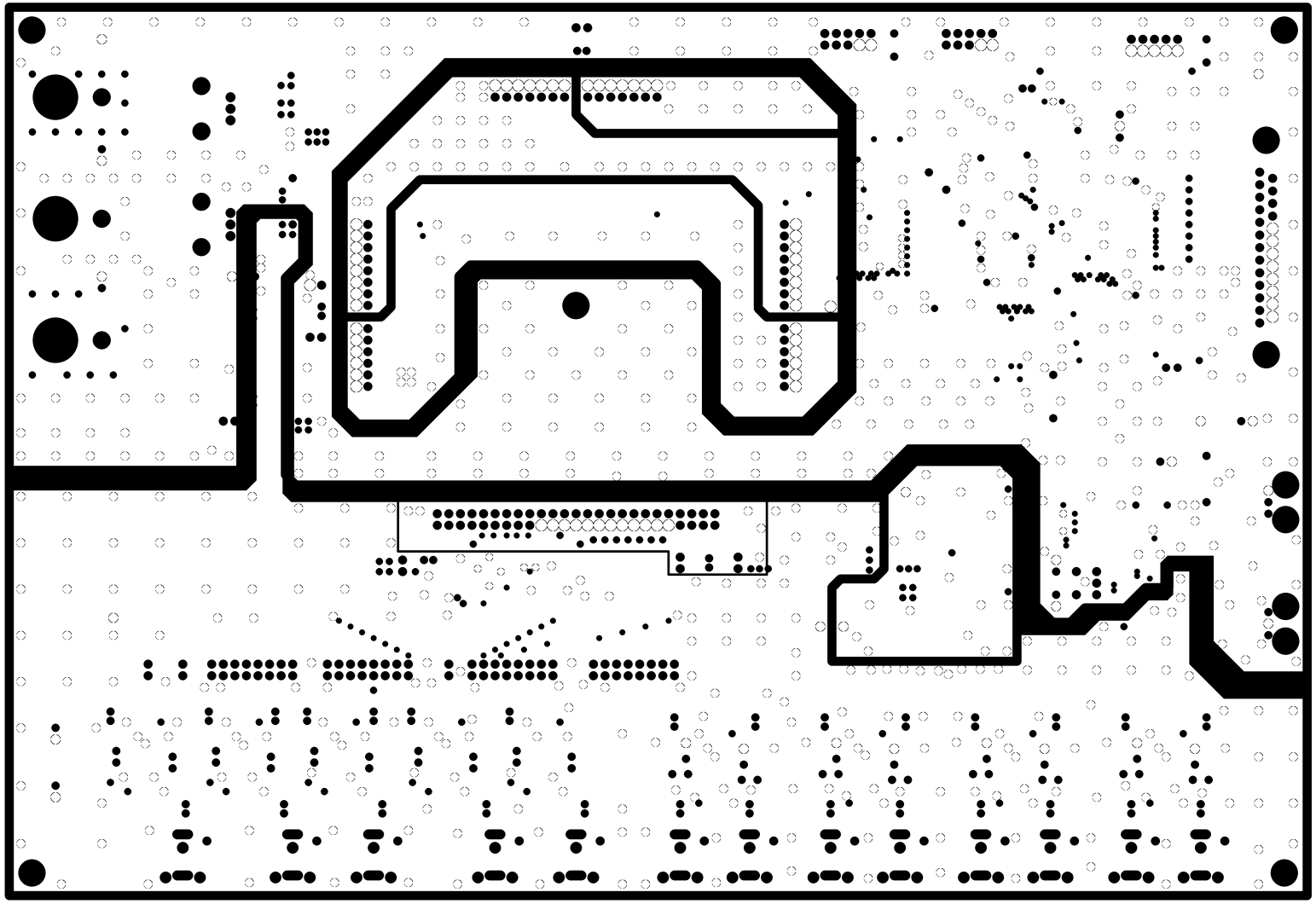
Title	<Title>	
Size A3	Document Number <Doc>	Rev <RevCode>
Date: Wednesday, July 12, 2006	Sheet 8 of 8	


AK7780
U1
JP1
HEADER 25X2
JP2
HEADER 15X2
JP3
HEADER 15X2
JP4
HEADER 2
JP5
HEADER 3
JP6
HEADER 2
JP7
HEADER 15X2
TP1
TP(BLUE)
TP2
TP(BLACK)
XTAL1
12.288MHz
着脱可とする
着脱可とする
水晶を着脱可とする
default 1-2short
EXT
XTL
AVDD_SRC
AVDD_AD
AVSS_CHIP
DVDD_CHIP
DVSS_CHIP
DVDD18_CHIP
AINM
AINR4
AINL4
AINR3
AINL3
AINR2
AINL2
AINRN
AINRP
AINLN
AINLP
AINR5
AINL5
AINR6
AINL6
AINR7
AINL7
AINR8
AINL8
TESTO
LFLT
AVSS1
AVDD1
TEST1
I2CSEL
SRCSET1
SRCSET0
BVSS1
DVDD1
DVSS1
XTI
XTO
DVSS2
DVDD18_2
CKM1
CKM0
DVDD18_3
DVSS3
DVDD3
LRCLK_O
BITCLK_O
SDOUT1
SDOUT2
SDOUT3
SRC_LFLT
AVSS2
AVDD2
TEST2
P_SRCSMUTE
BVSS2
DVDD_8
DVSS_8
DVDD18_8
P_SRCRST
SDA
SRC_LRCK
SRC_BICK
SDIN1
JX0
JX1
JX2
DVDD18_7
DVSS_7
DVDD_7
CLKO2
SDOUT6
SDOUTA1
STO
RDY
SDOUT4
SDOUT5
CLKO1
DVDD_4
DVSS_4
DVDD18_4
SDIN2
SDIN3
SDIN4
SDIN5
BITCLK_I
LRCLK_I
DVDD18_5
DVSS_5
INIT_RESET
P_CKRST
P_ADRST
P_DSPRST
RQ_N/CAD1
SI/CAD0
SCLK/SCL
DVDD18_6
DVSS_6
DVDD_6
SO
TEST2
P_SRC_SMUTE
P_SRC_RST
SDA
SRC_LRCK
SRC_BICK
SDIN1
JX0
JX1
JX2
DVDD18_CHIP
DVSS_CHIP
CLKO2
SDOUT6
SDOUTA1
STO
RDY
SDIN2
SDIN3
SDIN4
SDIN5
BITCLK_I
LRCLK_I
INIT_RESET
P_CKRST
P_ADRST
P_DSPRST
RQ_N
SI
SCLK
SO
C1 100uF(A)
C8 100uF(A)
C9 10uF
C10 0.1uF
C11 47nF(DIP)
R1 1.5k(DIP)
R2 1.5k(DIP)
C12 1.5uF(DIP)
C13 8.2nF(DIP)
C14 100uF(A)
C15 100uF(A)
C16 22pF(DIP)
C17 22pF(DIP)
R10 0(DIP)
R3 100
R4 100
R5 100
R6 100
R7 100
R8 100
R9 100
R11 100
R12 100
R13 100
C27 100uF(A)
C2 0.1uF
C3 10uF
C4 0.1uF
C5 10uF
C6 0.1uF
C7 10uF
C18 0.1uF
C20 10uF
C21 0.1uF
C19 10uF
C22 0.1uF
C23 10uF
C24 0.1uF
C25 10uF
C26 0.1uF
C28 0.1uF
(9,10) (9,10) (19,20) (19,20) (29,30) (29,30) (48,49) (56,57) (56,57) (68,69)
C29 0.1uF
C30 10uF
C31 0.1uF
C32 10uF
C33 0.1uF
C34 0.1uF
C35 10uF
C36 0.1uF
C37 10uF
C38 0.1uF
C39 0.1uF
C40 10uF
(13,14) (13,14) (18,19) (18,19) (30,31) (38,39) (38,39) (47,48) (47,48) (57,58) (67,68) (67,68)
Title chip
Size A2
Document Number <Doc>
Rev NC
Date: Wednesday, July 12, 2006
Sheet 1 of 1

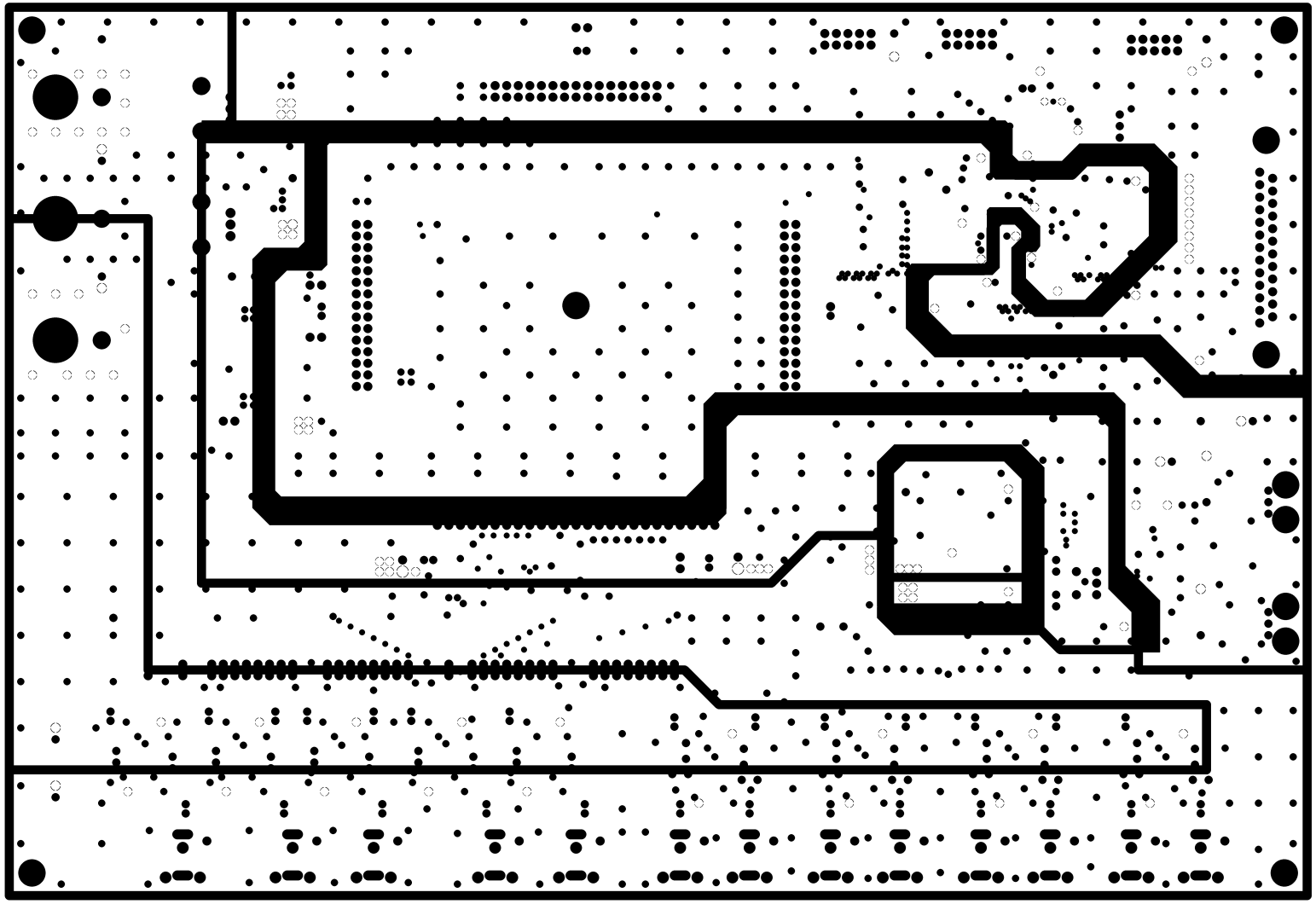

AK7780
U1
JP1
HEADER 25X2
JP5
HEADER 15X2
JP9
HEADER 15X2
JP2
HEADER 15X2
JP3
HEADER 2
default short
JP4
HEADER 2
default short
JP6
HEADER 2
JP7
HEADER 3
EXT
XTL
default 1-2short
JP8
HEADER 2
TP1
TP(BLUE)
TP2
TP(BLACK)
XTAL1
12.288MHz
着脱可とする
着脱可とする
水晶を着脱可とする
1setのみ、22pFとOΩ(DIP)も着脱可とする
0Ω(DIP)は、1setだけ、1pinソケット実装
その他は直付け
0uF(DIP)は、パターンのみ
1setだけ、1pinソケット実装
AVDD_SRC
AVDD_AD
AVSS_CHIP
DVDD18_CHIP
DVSS_CHIP
DVDD_CHIP
Title
Socket
Size
A2
Document Number
<Doc>
Rev
NC
Date:
Wednesday, July 12, 2006
Sheet
1
of
1



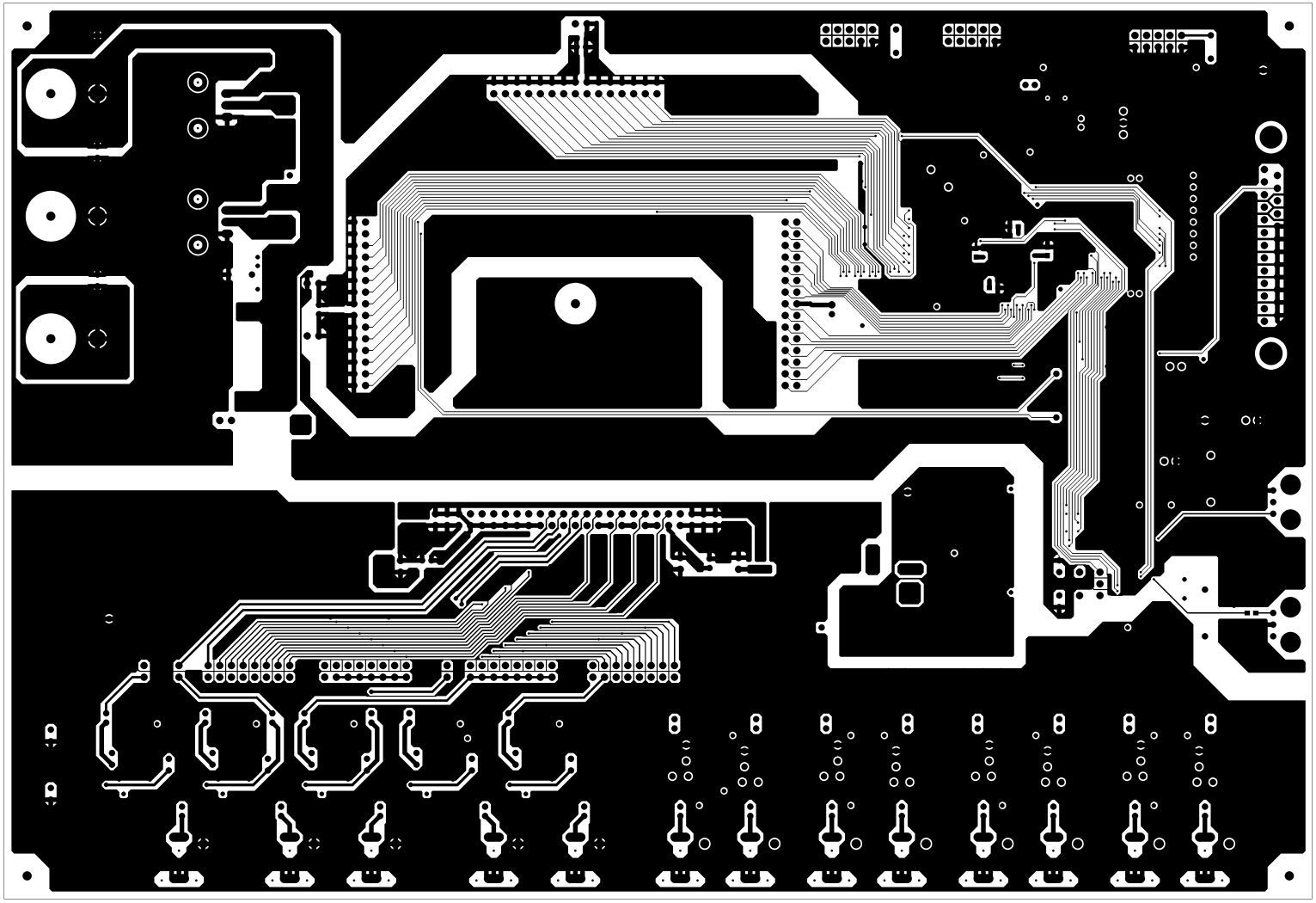
L1 パターン



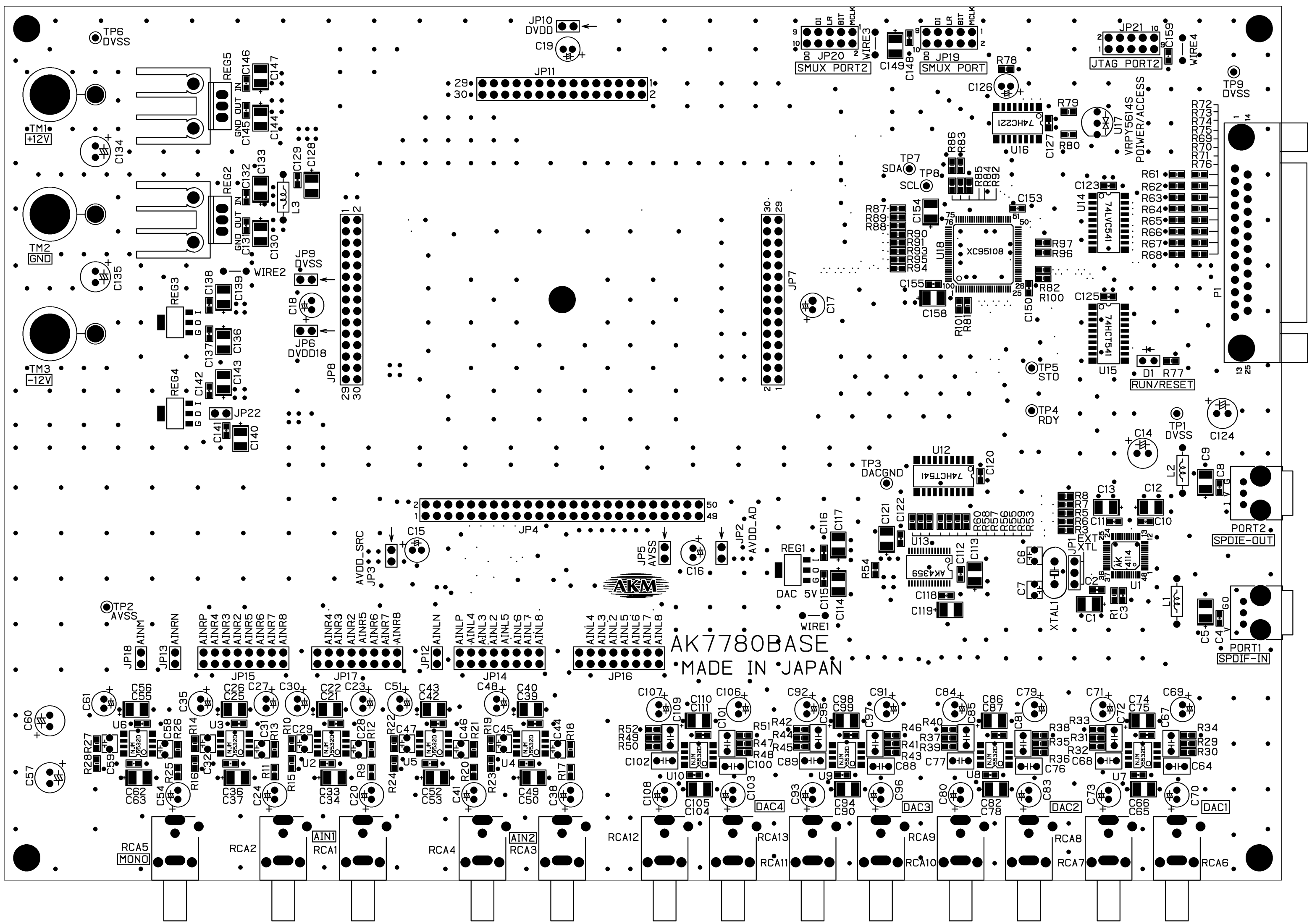
L2 GND



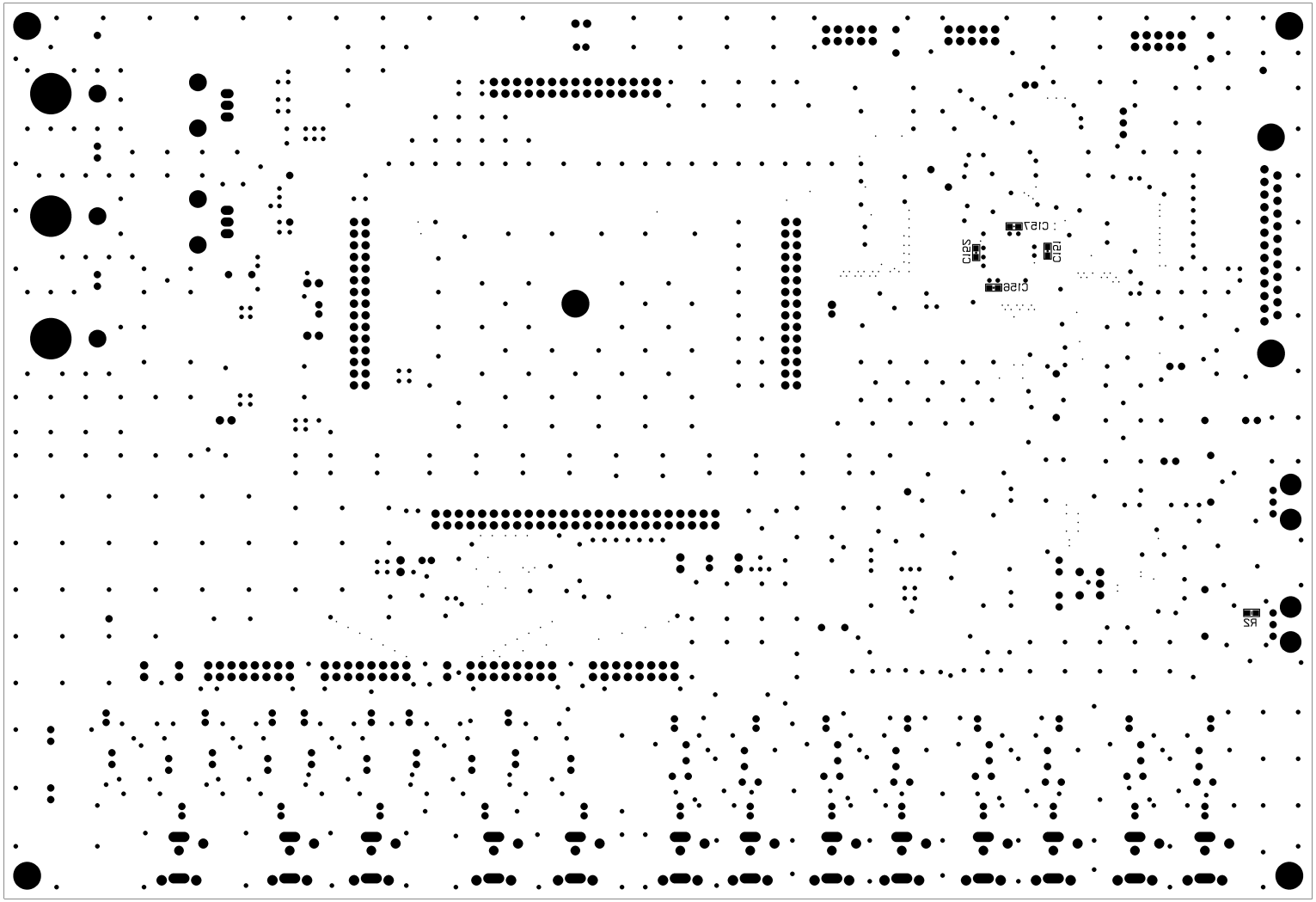
L3 VCC



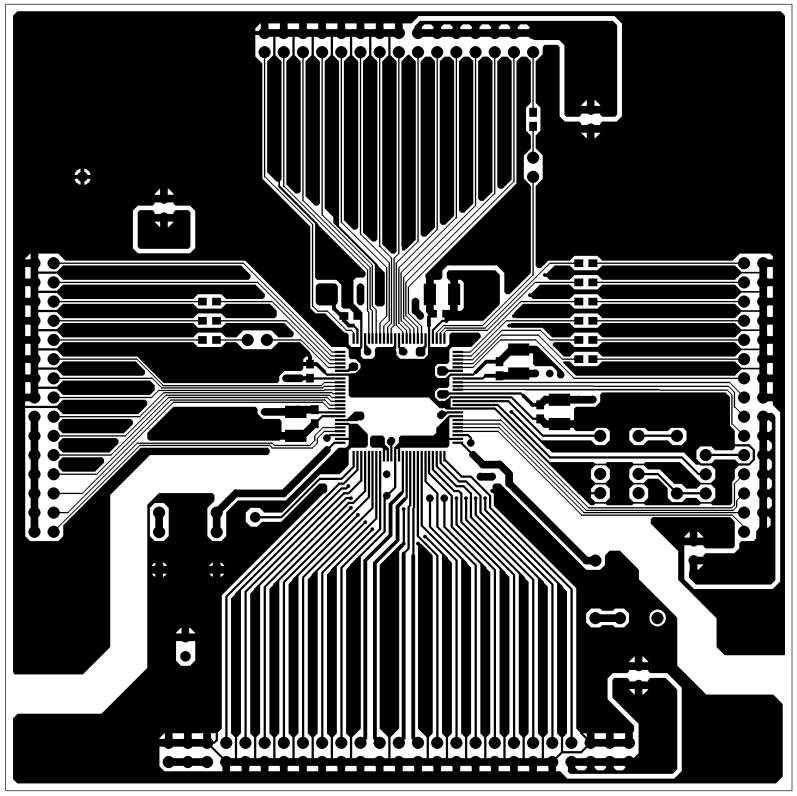
L4 パターン


AK7780BASE
MADE IN JAPAN
AKM
SMUX PORT2
SMUX PORT
JTAG PORT2
VRPY5614S
POWER/ACCESS
RUN/RESET
PORT2
SPDIE-OUT
PORT1
SPDIF-IN
+12V
GND
-12V
AVDD_SRC
AVDD_AD
DAC 5V
MONO
AIN1
AIN2
DAC4
DAC3
DAC2
DAC1
XC95108
74HC221
74LVC541
74HCT541
AK4359

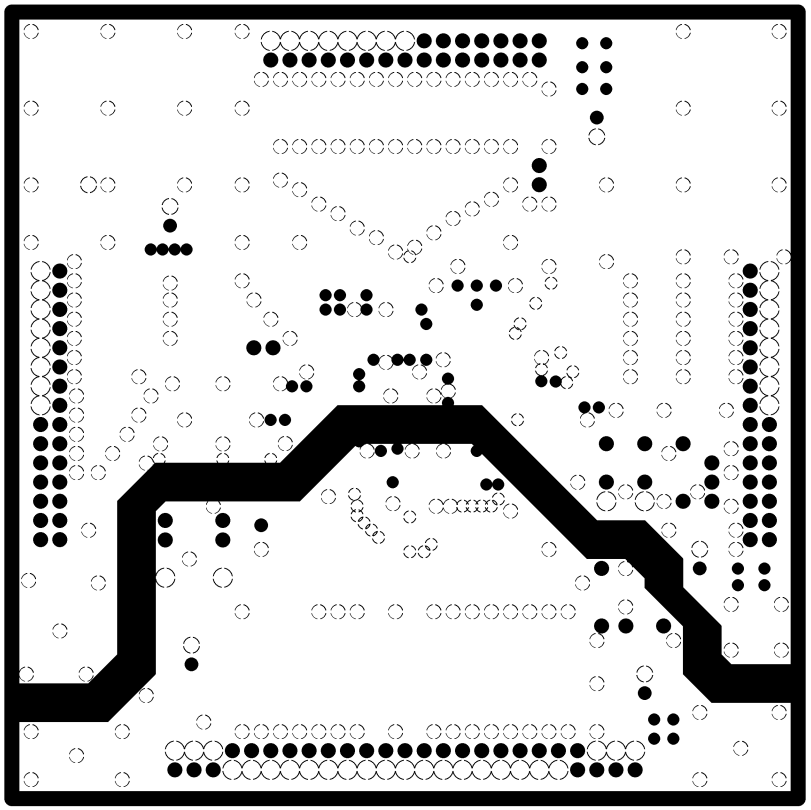
L1 S/R SILK



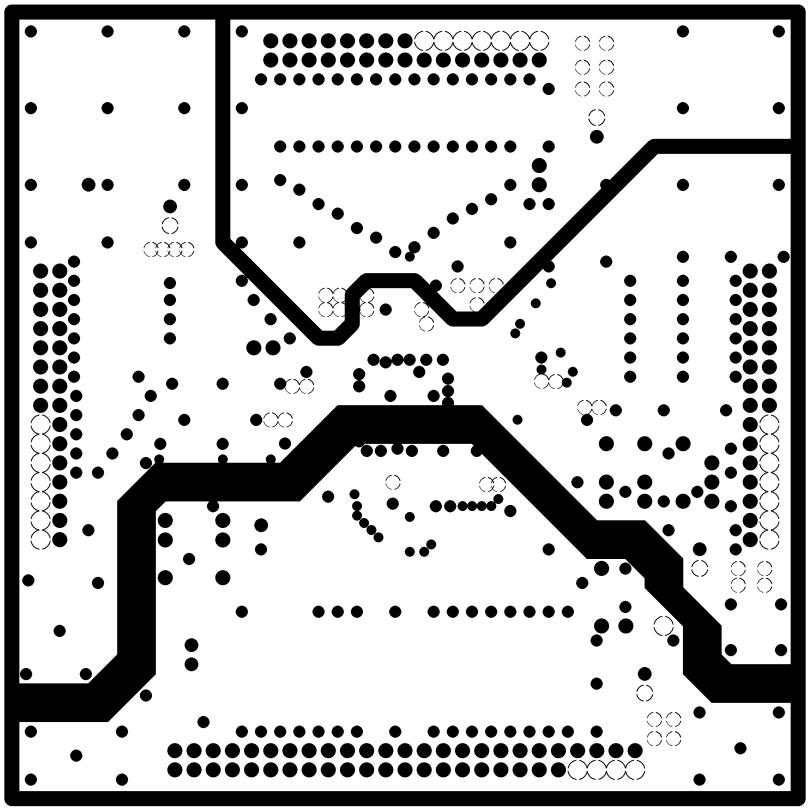
L4 S/R SILK



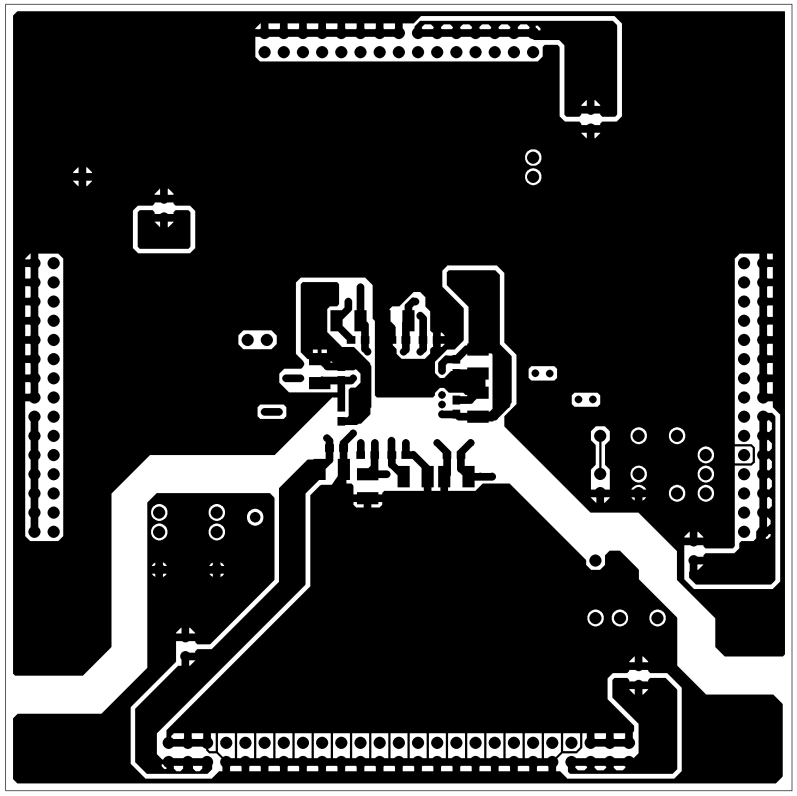
L1　パターン



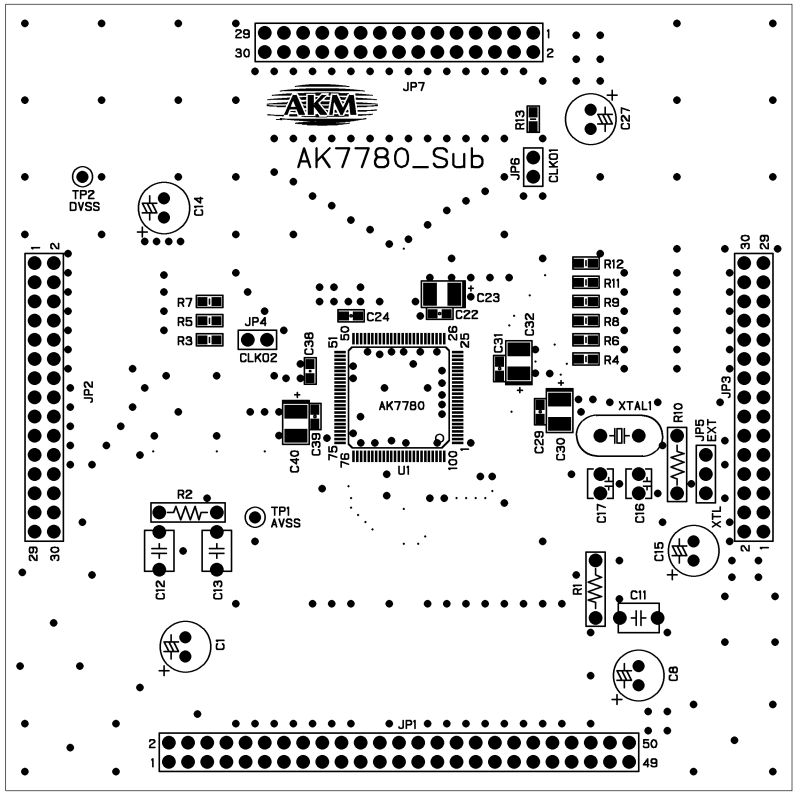
L2 GND



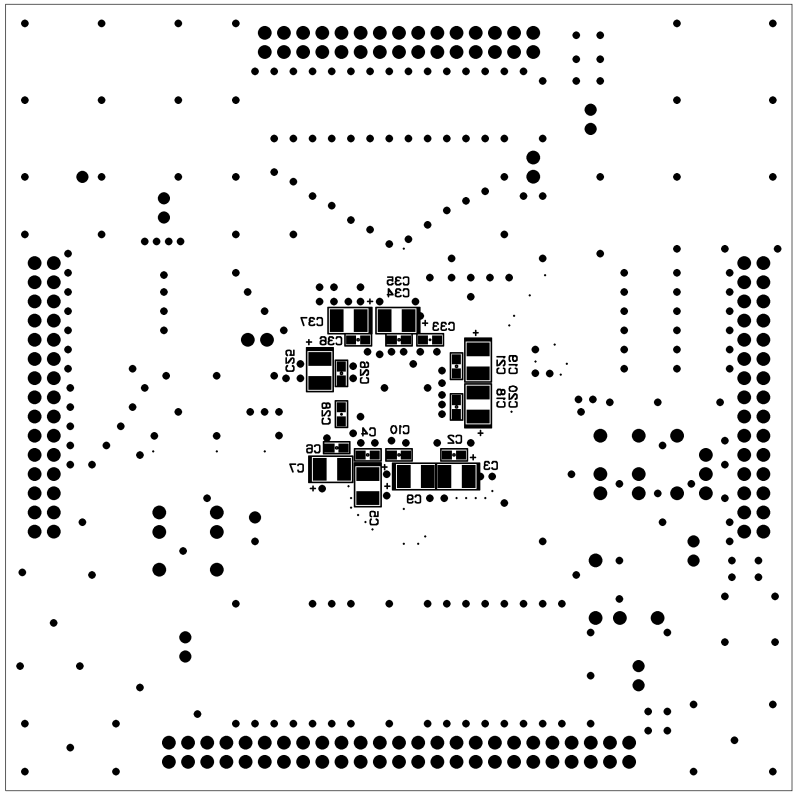
L3 VCC



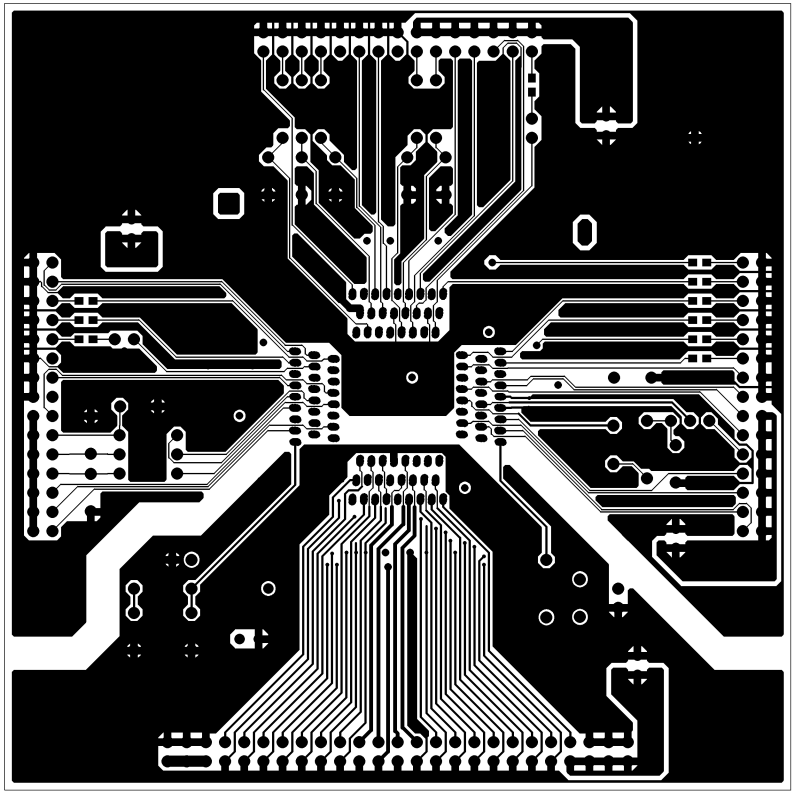
L4 パターン


AK7780_Sub
AKM
AK7780
JP7
JP1
JP2
JP3
JP4
JP5
JP6
TP1
AVSS
TP2
DVSS
CLKO1
CLKO2
EXT
XTAL1
XTL
U1
C1
C8
C11
C12
C13
C14
C15
C16
C17
C22
C23
C24
C27
C29
C30
C31
C32
C38
C39
C40
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13

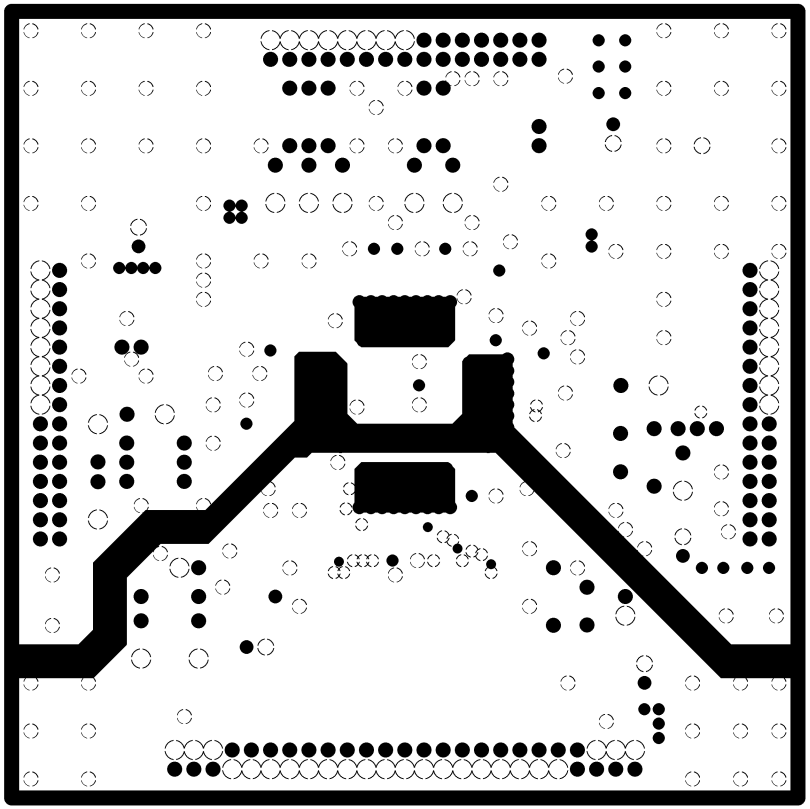
L1 S/R SILK



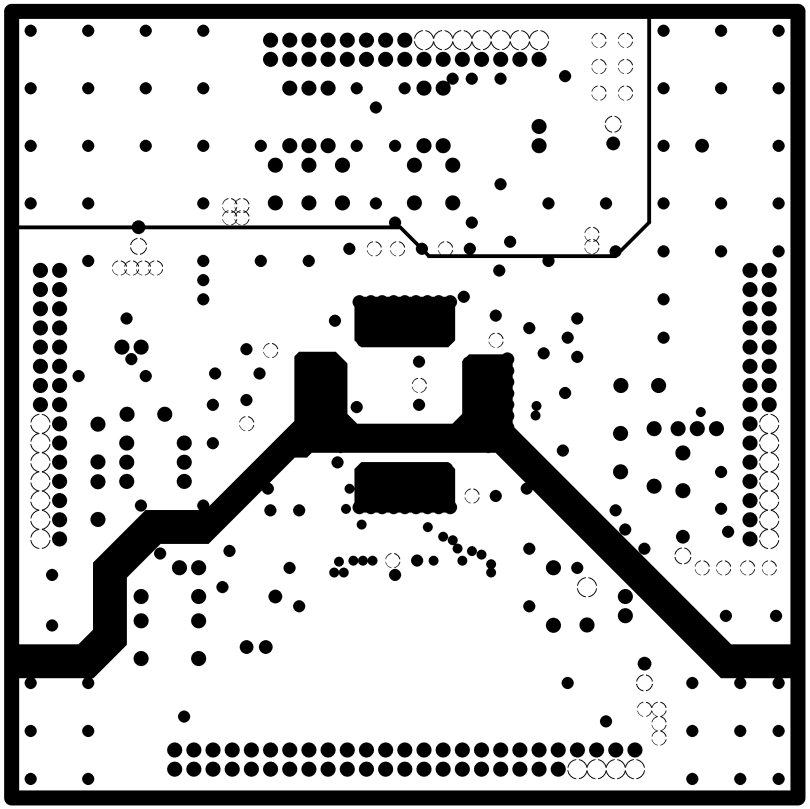
L4 S/R SILK



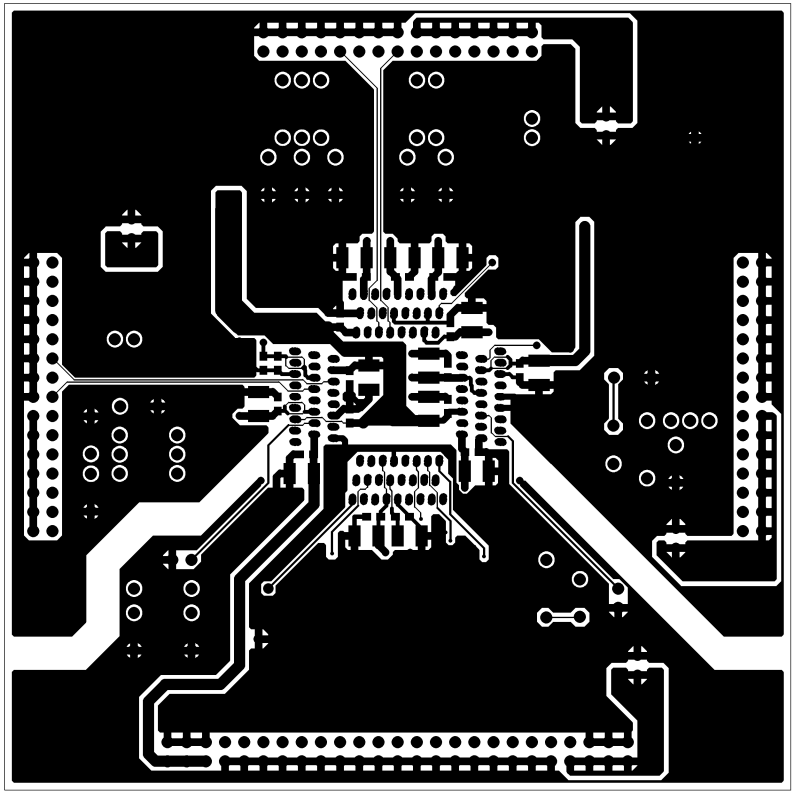
L1 層パターン



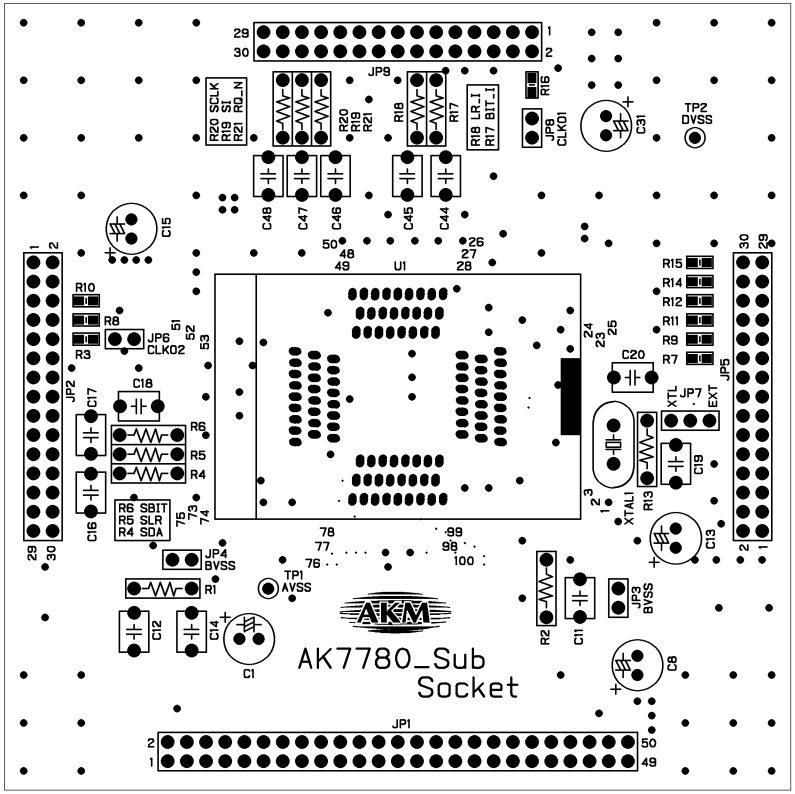
L2層(GND)



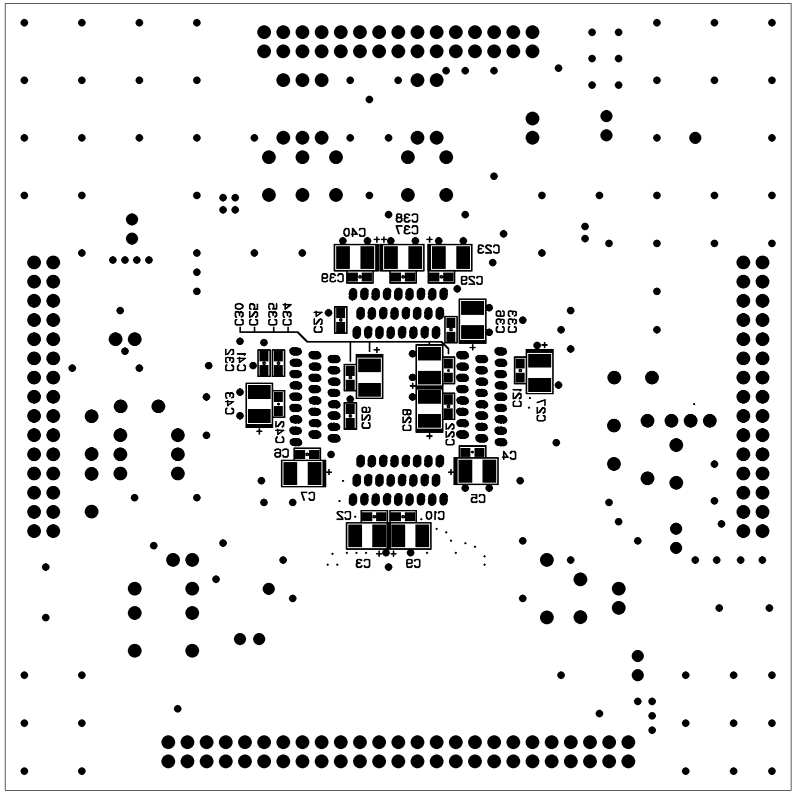
L3層（電源）



L4層パターン


AK7780_Sub
Socket
JP9
JP1
JP2
JP5
JP6
JP7
JP8
JP3
JP4
U1
TP1
AVSS
TP2
DVSS
CLK02
CLK01
XTAL
XTL
EXT
SCLK
SI
RD_N
LR_I
BIT_I
SBIT
SLR
SDA
BVSS

L1 層 レジスト シルク



L4層 レジスト シルク