# Am7968/Am7969

**TAXIchip™ Integrated Circuits**
**(Transparent Asynchronous Xmitter – Receiver Interface)**
**PRELIMINARY**

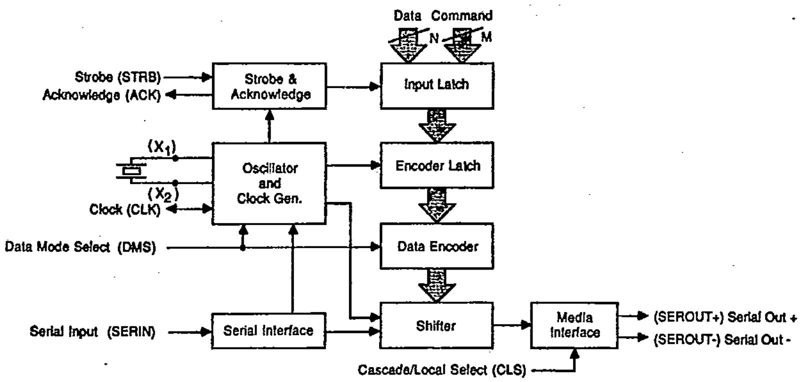


## DISTINCTIVE CHARACTERISTICS

- Parallel TTL bus interface
  - Eight Data and four Command Pins
  - or nine Data and three Command Pins
  - or ten Data and two Command Pins
- Transparent synchronous serial link
  - ECL 100K-compatible
  - FDDI PHY-0-compatible
  - AC or DC coupled
  - NRZI 4B/5B, 5B/6B encoding/decoding
- 32-100 Mbps (4-12.5 Mbytes/sec) data throughput
- Asynchronous input using STRB/ACK
- Automatic MUX/DEMUX of Data and Command
- Cascadable for longer patterns
- Complete on-chip PLL, Crystal Oscillator
- Single +5-V supply operation
- 28-pin PLCC, LCC or DIP

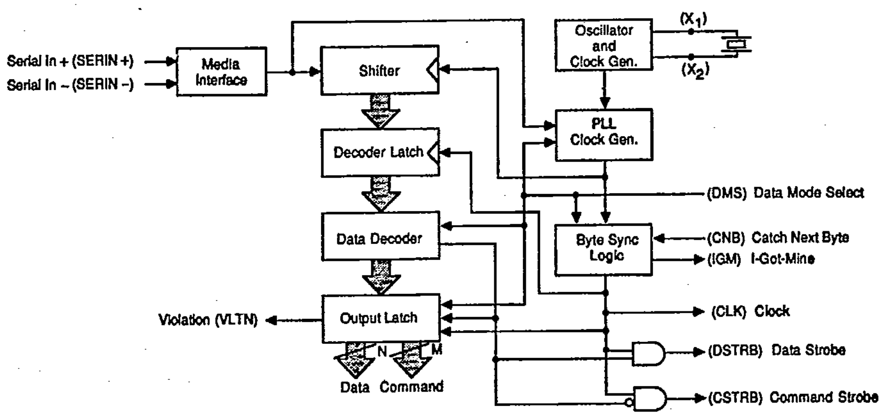
## BLOCK DIAGRAMS

### Am7968 TAXIchip Transmitter




BD007281

### Am7969 TAXIchip Receiver




BD007291

Note: N can be 8, 9, or 10 bits
Total of N + M = 12

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| Publication # | Rev. | Amendment |
|---|---|---|
| 07370 | B | /0 |

Issue Date: May 1987

## GENERAL DESCRIPTION



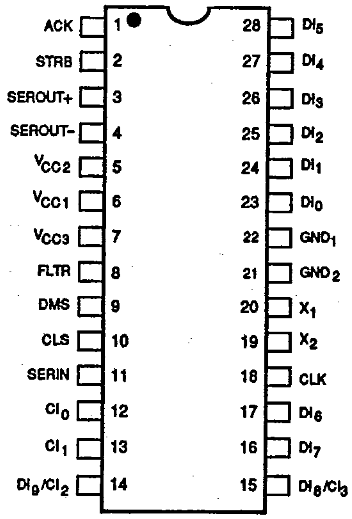
The Am7968 TAXIchip Transmitter and Am7969 TAXIchip Receiver Chipset is a general-purpose interface for very high-speed (4-12.5 Mbytes/sec, 40-125 Mbaud serially) point-to-point communications over coaxial or fiber-optic media. TAXIs emulate a pseudo-parallel register. They load data into one side and output it on the other, except in this case, the "other" side is separated by a long serial link.

The speed of a TAXIchip system is adjustable over a range of frequencies, with parallel bus transfer rates of 4 Mbytes/sec at the low end, and up to 12.5 Mbytes/sec at the high end. The TAXIchip's flexible bus interface scheme accepts bytes that are either 8, 9, or 10 bits wide. Multiple TAXIs can also be cascaded to accomodate a wider data bus. Byte transfers can be Data or Command signalling.

## CONNECTION DIAGRAMS
### Top View

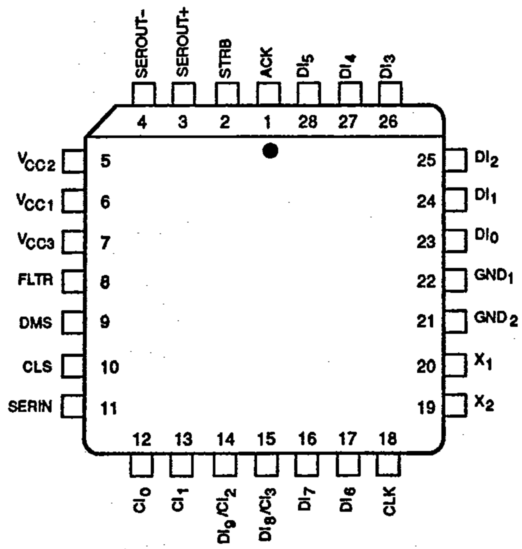
### Am7968

DIPs




CD010771

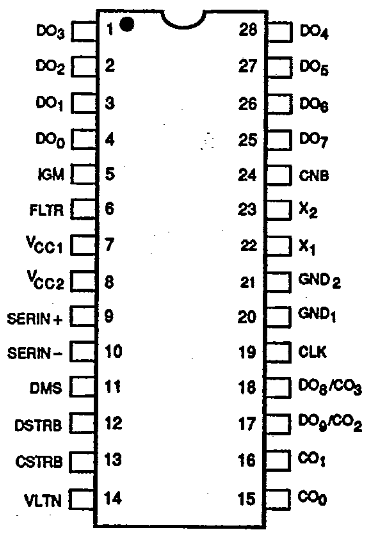
PLCC*




CD010781

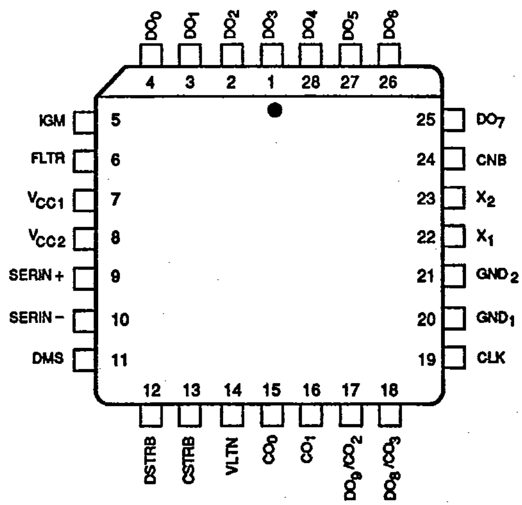
### Am7969

DIPs




CD010791

PLCC*



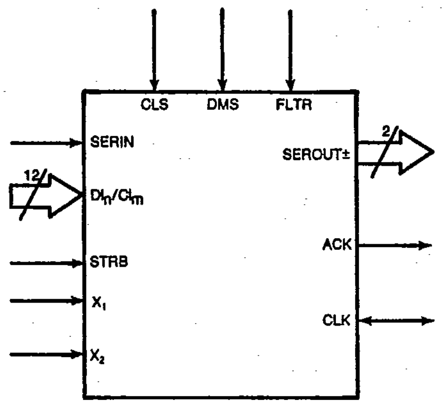

CD010801

Note: Pin 1 is marked for orientation.
* Also available in 28-Pin Ceramic Leadless Chip Carrier; pinout identical to PLCC.

## LOGIC SYMBOLS

T-75-37-05

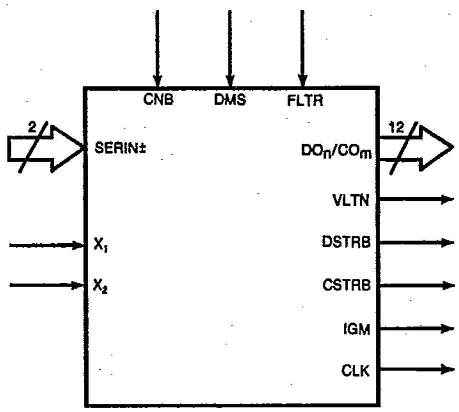
**Am7968**




LS002050

$V_{CC}$ = Power Supply (3)
GND = Ground (2)

**Am7969**




LS002061

$V_{CC}$ = Power Supply (2)
GND = Ground (3)

## ORDERING INFORMATION

### Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

**a. Device Number**
**b. Speed Option** (if applicable)
**c. Package Type**
**d. Temperature Range**
**e. Optional Processing**

AM7968 -100 D C B

**e. OPTIONAL PROCESSING**
Blank = Standard processing
B = Burn-in

**d. TEMPERATURE RANGE**
C = Commercial (0 to +70°C)
E = Extended Commercial (−55 to +125°C)

**c. PACKAGE TYPE**
P = 28-Pin Plastic DIP (PD 028)
D = 28-Pin Ceramic DIP (CD 028 or SD 028)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

**b. SPEED OPTION**
−70 = Max. Serial Encoded Transmission Rate is 70 MHz
−100 = Max. Serial Encoded Transmission Rate is 100 MHz
−125 = Max. Serial Encoded Transmission Rate is 125 MHz

**a. DEVICE NUMBER/DESCRIPTION**
Am7968 TAXIchip Transmitter
AM7969 TAXIchip Receiver

| Valid Combinations | |
|---|---|
| AM7968-70 | PC, PCB, DC, DCB, DE, DEB, JC, JCB, LE, LEB |
| AM7968-100 | |
| AM7968-125 | |
| AM7969-70 | |
| AM7969-100 | |
| AM7969-125 | |

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

## ORDERING INFORMATION (Cont'd.)

### APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:
**a. Device Number**
**b. Speed Option** (if applicable)
**c. Device Class**
**d. Package Type**
**e. Lead Finish**

AM7969 -100 /B X A

**e. LEAD FINISH**
A = Hot Solder Dip

**d. PACKAGE TYPE**
X = 28-Pin Ceramic DIP (CD 028 or SD 028)
3 = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

**c. DEVICE CLASS**
/B = Class B

**b. SPEED OPTION**
−70 = Max. Serial Encoded Transmission Rate is 70 MHz
−100 = Max. Serial Encoded Transmission Rate is 100 MHz
−125 = Max. Serial Encoded Transmission Rate is 125 MHz

**a. DEVICE NUMBER/DESCRIPTION**
Am7968 TAXIchip Transmitter
Am7969 TAXIchip Receiver

| Valid Combinations | |
|---|---|
| AM7968-70 | /BXA, /B3A |
| AM7968-100 | |
| AM7968-125 | |
| AM7969-70 | |
| AM7969-100 | |
| AM7969-125 | |

**Valid Combinations**

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

**Group A Tests**

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### Am7968 TAXIchip Transmitter

**$DI_0 - DI_7$ Parallel Data In (TTL Inputs)**

These eight inputs accept parallel data from the host system, to be latched, encoded and transmitted.

**$DI_8/CI_3$ Parallel Data (8) In or Command (3) In (TTL Input)**

*$DI_8/CI_3$* input is either Data or Command, depending upon the state of *DMS*.

**$DI_9/CI_2$ Parallel Data (9) In or Command (2) In (TTL Input)**

*$DI_9/CI_2$* input is either Data or Command, depending upon the state of *DMS*.

**$CI_0 - CI_1$ Parallel Command In (TTL Inputs)**

These two inputs accept parallel command information from the host system. If one or more command bits are logic "1", the command bit pattern is latched, encoded, and transmitted in place of any pattern on the Data inputs.

**STRB Input Strobe Signal (TTL Input)**

A rising edge on the *STRB* input causes the Data *($DI_0 - DI_9$)* or the Command *($CI_0 - CI_3$)* inputs to be latched into the Am7968 Transmitter. The *STRB* signal is normally taken LOW, after *ACK* has risen.

**ACK Input-Strobe Acknowledge (TTL Output)**

The rising edge of *ACK* signifies that the Am7968 is ready to accept new Data and Command. The timing of *ACK's* response to *STRB* depends on the condition of the Input Latch (in a given CLK cycle) and on the Transmitter's operating mode (Local or Cascade).

In Local mode, if the Input Latch is empty, data is immediately stored and *ACK* closely follows *STRB*. If the Input Latch contains previously stored data when *STRB* is asserted, *ACK* is delayed until the next falling edge of *CLK*.

If *STRB* is asserted when in Cascade mode, *ACK* will stay LOW until Sync is detected in the Shifter. The rising edge of *ACK* signifies that all Cascaded data has propagated downstream.

**SERIN Serial Data In (ECL Input)**

The *SERIN* input accepts ECL voltage swings, which are referenced to +5.0 V. *SERIN* data passes into the internal Shifter and allows one Am7968 Transmitter to be cascaded with another. *SERIN* directly connects to another Am7968 Transmitter's *SEROUT+* output. This pin has an internal pull-down resistor and is interpreted as a logic "0" when left unconnected.

**SEROUT+, SEROUT− Differential Serial Data Out (Differential ECL Outputs)**

These differential ECL outputs generate data at ECL voltage levels referenced to +5.0 V. They are capable of driving 50-Ω terminated lines, either directly or through isolating capacitors.

**$X_1$, $X_2$ Crystal Oscillator Inputs (Inputs)**

These two crystal input pins connect to an oscillator which operates at the fundamental frequency of a parallel resonant crystal. The byte rate matches the crystal frequency.

Alternatively, *$X_1$* can be driven by an external TTL frequency source. In multiple TAXI systems this external source could be another Am7968's *CLK* output.

**DMS Data Mode Select (Input)**

Data Mode Select input determines the Data pattern width. When it is wired to GND, the Am7968 Transmitter will assume Data to be eight bits wide, with four bits of Command. When it is wired to $V_{CC}$, the Am7968 Transmitter will assume Data to be nine bits wide, with three bits of Command. If *DMS* is left floating (or terminated to 1/2 $V_{CC}$), the Am7968 will assume Data to be ten bits wide, with two bits of Command.

**CLS Cascade/Local Select (Input)**

Cascade/Local Select input determines the mode of operation. When it is wired to $V_{CC}$, the Am7968 Transmitter is in Cascade mode and should be connected to another Am7968 Transmitter. In Cascade mode the Am7968 will output NRZ data instead of NRZI data, and will disable its *CLK* output. When *CLS* is wired to GND, the Am7968 Transmitter assumes a Local mode connection to the media. It will output NRZI encoded data, and will enable its *CLK* output driver.

When this input is left unconnected, it floats to an intermediate level which puts the Am7968 Transmitter into its test mode. In Test mode, the internal clock multiplier is switched out, and the internal logic is clocked directly from the *CLK* pin. Test mode is not intended for normal operation.

**CLK Clock (TTL I/O)**

*CLK* is an I/O pin that supplies the byte-rate clock reference to drive all internal logic and to synchronize cascaded Am7968 Transmitters. When *CLS* is connected to ground (Local mode), *CLK* is enabled as a free-running (byte rate) clock output which runs at the Crystal Oscillator frequency; this output can be used to drive the *$X_1$* input of TAXIchip Receivers or the *CLK* input of other Am7968s which are in Cascade mode. When *CLS* is connected to $V_{CC}$ (Cascade mode), the *CLK* pin acts as an input reference for the internal PLL clock multiplier, and a synchronizing reference for cascaded Am7968 Transmitters. In Test mode *CLK* becomes a 'bit rate' input.

**FLTR Filter (Input)**

The *FLTR* pin allows a low-pass filter to be added to the PLL frequency multiplier.

**$V_{CC1}$, $V_{CC2}$, $V_{CC3}$ Power Supply**

*$V_{CC1}$*, *$V_{CC2}$* and *$V_{CC3}$* are +5.0-volt nominal power supply pins. *$V_{CC1}$* powers TTL, *$V_{CC2}$* powers ECL and *$V_{CC3}$* powers Logic and Analog circuitry.

**$GND_1$, $GND_2$ Ground Pins**

*$GND_1$* is a TTL Ground and *$GND_2$* is Logic and Analog Ground.

## PIN DESCRIPTION (Cont'd.)

### Am7969 TAXIchip Receiver

**$DO_0 - DO_7$ Parallel Data Out (TTL Outputs)**
These eight outputs reflect the most recent valid Data received by the Am7969 Receiver.

**$DO_8/CO_3$ Parallel Data (8) Out or Command (3) Out (TTL Output)**
*$DO_8/CO_3$* output will be either a Data or Command bit, depending upon the state of *DMS.*

**$DO_9/CO_2$ Parallel Data (9) Out or Command (2) Out (TTL Output)**
*$DO_9/CO_2$* output will be either a Data or Command bit, depending upon the state of *DMS.*

**$CO_0 - CO_1$ Parallel Command Out (TTL Output)**
These two outputs reflect the most recent valid Command data received by the Am7969 Receiver.

**DSTRB Output Data Strobe (TTL Output)**
The rising edge of this output signals the presence of new Data on the $DO_0 - DO_9$ lines. Data is valid just before the rising edge of *DSTRB* .

**CSTRB Command Data Strobe (TTL Output)**
The rising edge of this output signals the presence of new Command data on the $CO_0 - CO_3$ lines. Command bits are valid just before the rising edge of *CSTRB.*

**VLTN Violation (TTL Output)**
The rising edge of this output indicates that a transmission error has been detected. It changes state at the same time $DO_i$ or $CO_i$ change and will be followed by either *DSTRB* or *CSTRB.* This pin goes LOW when the next valid byte is decoded.

**IGM I-Got-Mine (TTL Output)**
This pin signals cascaded Am7969 Receivers that their upstream neighbor has captured its assigned data byte. *IGM* falls at the mid-byte point, when the first half of a sync byte is detected in the Shifter. It rises when, at the mid-byte point, it detects a non-sync pattern.

**CLK Clock (TTL Output)**
This is a free-running clock output which runs at the Crystal Oscillator rate (byte rate), and is synchronous with the serial transfer rate. It falls at the time that the Decoder Latch is loaded from the Shifter, rises at mid-byte, and can be used to drive $X_1$ inputs on other Am7969s if no other source is available.

**CNB Catch Next Byte Input (TTL Input)**
This input controls the Cascade mode on the Am7969 Receiver. If this input is connected to its *CLK* output, the TAXI will be in the Local mode, and each received byte will be captured, decoded and latched to the outputs.

If the *CNB* input is HIGH, it allows the Am7969 Receiver to capture the first byte after a sync. The Am7969 Receiver will wait for another sync before latching the data out, and capturing another. If *CNB* is toggled LOW, it will react as if it had decoded a sync byte.

In Cascade mode, *CNB* input is typically connected to an upstream Am7969's *IGM* output. The first Am7969 Receiver in line will have its *CNB* input connected to $V_{CC}$.

**SERIN+, SERIN− Differential Serial Data In (ECL Inputs)**
Both pins have internal pull-down resistors. This data is shifted serially into the Shifter. The *SERIN+* and *SERIN−* differential ECL inputs accept ECL voltage swings, which are referenced to +5.0 V. When *Serin−* is grounded, the Am7969 is put into Test Mode; *Serin+* becomes a single-ended ECL input, the PLL clock generator is bypassed, and $X_1$ determines the bit rate (rather than the byte rate).

**$X_1$, $X_2$ Crystal Oscillator Inputs (Inputs)**
These two crystal input pins connect to an oscillator which oscillates at the fundamental frequency of a parallel resonant crystal (byte rate). Alternatively, $X_1$ can be driven by an external frequency source. In multiple TAXI systems, this external source could be another TAXI's *CLK* output (preferably that of a neighboring Am7968).

**DMS Data Mode Select (Input)**
*DMS* selects the Data pattern width. When it is wired to GND, the Am7969 Receiver will assume Data to be eight bits wide, with four bits of Command. When it is wired to $V_{CC}$, the Am7969 Receiver will assume Data to be nine bits wide, with three bits of Command. If *DMS* is left floating (or terminated to 1/2 $V_{CC}$), the Am7969 Receiver will assume Data to be ten bits wide, with two bits of Command.

**FLTR Filter (Input)**
The *FLTR* pin is to allow a low-pass filter to be added to the PLL frequency multiplier.

**$V_{CC1}$, $V_{CC2}$ Power Supply**
*$V_{CC1}$ and $V_{CC2}$ are +5.0-volt nominal power supply pins.* $V_{CC1}$ powers TTL, and $V_{CC2}$ powers Logic and Analog circuitry.

**$GND_1$, $GND_2$ Ground**
$GND_1$ is a TTL Ground, $GND_2$ is a Logic and Analog Ground.

## FUNCTIONAL DESCRIPTION

### System Configuration

The TAXIchip system (see Block Diagrams and Figure 2) has two main configurations, Local mode and Cascade mode (Figures 3 & 4). In the Local mode, each Transmitter/Receiver pair is connected by a separate high-speed serial link. In the Cascade mode, one high-speed serial link is shared by several TAXI pairs.

In either mode, the Am7968 Transmitter accepts inputs from a sending host system using a simple *STRB/ACK* handshake. Parallel bits are saved by the Am7968's input latch on the rising edge of a *STRB* input. The input latch can be updated on every *CLK* cycle; if it still contains previously stored data when a second *STRB* pulse arrives, the second *ACK* response is delayed until the next *CLK* cycle.

The inputs to an Am7968 Transmitter can be either Data or Command and may originate from two different parts of the host system. A byte cycle may contain Data or Command, but not both. Data represents the normal data channel message traffic between host systems. Commands can come from a communication control section of the host system. Commands occur at a relatively infrequent rate but have priority over Data. Examples include communication specific commands such as REQUEST-TO-SEND or CLEAR-TO-SEND; or application specific commands such as MESSAGE-ADDRESS-FOLLOWS, MESSAGE-TYPE-FOLLOWS, INITIALIZE YOUR SYSTEM, ERROR, RETRANSMIT, HALT, etc.

The Am7968 Transmitter switches between Data and Command by examining Command input patterns. All 0's on Command Input pins cause information on the Am7968's Data Input pins to be latched into the device on the rising edge of *STRB*. All other Command patterns cause a Command symbol to be sent in response to an input strobe. The pattern on the Data Inputs is ignored when a Command symbol is sent. In either case, if there is no *STRB* before the next byte boundary, a Sync symbol will be transmitted. The Sync pattern maintains link synchronism and provides pulses to keep the Receiver Phase-Locked-Loop (PLL) circuits in lock.

The Sync pattern utilized by TAXIchips keeps the automatic gain control (AGC) fiber-optic transceiver circuits in their normal range because the pattern has zero DC offset. It was also chosen for its unique pattern which never occurs in any Data or Command messages. This feature allows Sync to be used to establish byte boundaries.

The Am7969 Receiver detects the difference between Data and Command patterns and routes each to the proper Output Latch. When a new Data pattern is captured by the output latch, *DSTRB* is pulsed and Command information remains unchanged. If a Command pattern is sent to the output latch or if Sync is received, *CSTRB* is pulsed and Data outputs remain in their previous state. Reception of a Sync pattern clears the Command outputs to all 0's.

Noise-induced bit errors can distort transmitted bit patterns. The Am7969 Receiver logic detects most noise-induced transmission errors. Invalid bit patterns are recognized and indicated by the assertion of the violation (*VLTN*) output pin. This signal rises to a logic "1" state at the same time that Data or Command outputs change and remains HIGH until a valid pattern is detected by the Data Decoder. The error detection method used in the Receiver cannot identify bit errors which transform one valid Command or Data pattern to another. Fault-sensitive systems should use additional error checking mechanisms to guarantee message integrity.

## Am7968 Transmitter

The Transmitter can accept messages from either of two sources: parallel input pins (Command or Data) or the *SERIN* input. The device will send data which appears on its *SERIN* pin only if there is no new parallel information to be sent (evident by lack of strobe). This single-ended ECL input is intended to be left open or connected to the *SEROUT+* pin of another TAXI Transmitter (see Cascade Mode). Once latched into an Am7968, a parallel message is encoded, serialized, and shifted out to the serial link. The idle time between transmitted bytes is filled with Sync bytes.

## Am7969 Receiver

Receivers accept differential signals on the *SERIN+/SERIN–* input pins. This information, previously encoded by an Am7968 Transmitter, is loaded into a decoder.

When serial patterns are received, they are decoded and routed to the appropriate outputs. If the received message is a Command, it is stored in the output latch, appears at the Command output pins, and *CSTRB* is pulsed; Data output pins continue holding the last Data byte and *DSTRB* stays inactive. If a Data message follows the reception of a Command, Command output pins continue holding the previous Command byte and *CSTRB* stays inactive. The command outputs will retain their states until another Command signal is received (Sync is considered to be a valid command which resets Command outputs to "0").

## Byte Width

TAXIchips have twelve parallel interface pins which are designated to carry either Command or Data bits. The Data Mode Select (*DMS*) pin on each chip can be set to select one of three modes of operation: eight Data and four Command bits, nine Data and three Command, or ten Data and two Command. This allows the system designer to select the byte-width which best suits system needs.

T-75-37-05

## Am7968 Encoder/Am7969 Decoder

To guarantee that the Am7969's PLL can stay locked onto an incoming bit stream, the data encoding scheme must provide an adequate number of transitions in each data pattern. This implies a limit on the maximum time allowed between transitions. The TAXIchip encoding scheme is based on the ANSI X3T9.5 (FDDI) committee's 4-bit/5-bit (4B/5B) code.

An ANSI X3T9.5 system uses an 8-bit parallel data pattern. This pattern is divided into two 4-bit nibbles which are each encoded into a 5-bit symbol. Of the thirty-two patterns possible with these five bits, sixteen are chosen to represent the sixteen input Data patterns. Some of the others are used as Command symbols. Those remaining represent invalid patterns that fail either the run-length test or DC balance tests.

Transmitters in 8-bit mode use two 4B/5B encoders to encode eight Data bits into a 10-bit pattern. In 9-bit mode, Transmitters use one 5B/6B encoder and one 4B/5B encoder to code nine Data bits into an 11-bit pattern. In 10-bit mode, two 5B/6B encoders are used to change ten bits of Data into a 12-bit pattern. (See Tables 1 and 2 for encoding patterns).

The Am7968 Transmitter further encodes all symbols using NRZI (Non Return to Zero, Invert on ones). NRZI represents a "1" by a transition and a "0" by the lack of a transition. In this system a "1" can be a HIGH-to-LOW or LOW-to-HIGH transition. This combination of 4B/5B and NRZI encoding ensures at least two transitions per symbol and permits a maximum of three consecutive non-transition bit times. The Am7969 then uses the same method to decode incoming symbols so that the whole encoding/decoding process is transparent to the user.

Serially transmitted patterns with this code will have the same average amount of HIGH and LOW times. This DC balance minimizes pattern-sensitive decoding errors which are caused by jitter in AC-coupled systems.

## Operational Modes

### Local Mode

In this mode, a single Transmitter/Receiver pair is used to transfer 8, 9, or 10 bits of parallel Data over a private serial link. On the Am7968, *CLS* is tied to ground and *SERIN* is left open. The Am7969 Receiver continuously deserializes the incoming bit stream, decodes the resulting patterns, and saves parallel data at its output latches (see Figure 3).

Local mode provides the fastest potential parallel throughput because data can be transferred on every clock cycle. On the other hand, it is not necessary for the host to match the byte rate set by the Transmitter's crystal oscillator; the Am7968 automatically sends a Sync pattern during each clock cycle in which no new Data or Command messages are being transmitted.

### Cascade Mode

For very wide parallel buses, TAXI's can be Cascaded to send multiple-byte words over a single serial channel (see Figure 4). The primary Transmitter has its *SEROUT±* pins tied to the media (or an optical data link) and its SERIN pin is connected to the *SEROUT+* pin of its upstream neighbor. This *SERIN–/SEROUT+* connection is repeated for each subsequent Am7968 in the chain. *CLS* on the primary Transmitter is tied to ground, putting it in Local mode, and is connected to $V_{CC}$ on all other Am7968s in the chain, putting them in

Cascade mode. The *DMS* pin must be tied to the same level on every TAXI, putting each of them in the same bit configuration (8-, 9-, or 10-bit mode). The *CLK* output of the primary Transmitter is tied to the *CLK* input pin of each upstream Am7968. The Am7969 Receivers all have their *SERIN+* and *SERIN-* pins connected to the media (or an optical data link). *IGM* of each Am7969 is connected to *CNB* of its downstream neighbor or is left open on the Receiver farthest downstream. *CNB* of the first Receiver is tied HIGH, making this device the only Receiver in the chain that can act on the first non-Sync pattern in a message (see below).

In a Cascaded system, all Transmitters simultaneously latch their message upon seeing a common *STRB*. Cascaded Transmitters must place at least one Sync between words. This is easily accomplished by using the *ACK* response from the Am7968 second from the media as a "ready" indication.

Each TAXIchip Receiver monitors the serial link and a special acknowledgement scheme is used to direct symbols into each of the Am7969s. When a Catch-Next-Byte (*CNB* ) input is HIGH, the Receiver will capture the next non-Sync symbol from the serial link. It then waits for a Sync symbol or for its *CNB* to be set LOW before saving the message in its decoder latch. At this point, the device forces its I-Got-Mine (*IGM* ) pin HIGH to tell the downstream Receiver to capture the next symbol. This output returns LOW whenever a Sync byte is detected or when *CNB* goes LOW. This *IGM-CNB* exchange continues down the chain until the last Receiver captures its respective byte. The next byte to appear on the serial link will be a Sync symbol which is detected by all of the cascaded Am7969s. On the following Clock cycle their messages are transferred to the output latch of each device and sent to the receiving host. *IGM* pins on all Receivers are also set LOW when the first half of the Sync symbol is detected.

#### Unbalanced Mode

While Local and Cascade modes require an equal number of Receivers and Transmitters used in a link to be equal, Unbalanced mode allows unequal combinations to be used. This implementation follows the same general rules as Cascade mode.

### Asynchronous Operation

In Local mode, inputs to the Am7968 Transmitter Input Latch can be asynchronous to its internal clock. Data *STRB* will latch data into the Am7968 Transmitter and an internal clock will transfer the data to the Encoder Latch at the first byte boundary. Data can be entered at any rate less than the maximum transfer rate without regard to actual byte boundaries. Individual data events can be strobed into the Am7968 Transmitter at less than the byte transfer time, if the *STRB/ACK* protocol is observed.

In systems where Am7969 Receivers lose byte/symbol sync, and on power-up, internal logic detects this loss-re-acquisition of sync and modifies the *CLK* output. *CLK* output is actually a buffered version of the signal which controls Data transfers inside the Am7979 Receiver on byte boundaries. Byte boundaries move when the Am7969 Receiver loses, and re-acquires sync. To protect slave systems (which may use this output as a master clock) from having clocks which are too narrow, the output logic will stretch an output when the output pulse would have been less than a byte-time long. The data being processed just prior to this re-acquisition of sync will be lost. The Sync symbol, and all subsequent data will be processed correctly.

### TAXI User Test Modes

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Cascade/Local Select (*CLS* ) input can be used to force the Am7968 Transmitter into a Test mode. This will allow testing of the logic in the Latches, Encoder, and Shifter without having to first stabilize the PLL clock multiplier. If *CLS* is open or terminated to approximately $V_{CC}/2$, the internal $V_{CO}$ is switched out and everything is clocked directly from the *CLK* input. This means that the serial output data rate will be at the byte Clock rate and not at 10X, 11X, or 12X, as is the case in normal operation.

Differential *SERIN+/SERIN-* inputs can be used to force the Am7969 Receiver into a Test mode. This will allow testing of the logic in the Latches, Encoder, and Shifter without having to first stabilize the PLLs. If *SERIN-* is tied to ground, the internal $V_{CO}$ is switched out and $X_1$ becomes the internal bit rate clock. This means that the serial data rate will be at the crystal rate, not at 10X, 11X, or 12X, as is the case in normal operation. In this mode, *SERIN+* becomes a single-ended serial data input with nominal 100K ECL threshold voltages.

These switches make the parts determinate, synchronous systems, instead of statistical, asynchronous ones. An automatic test system will be able to clock each part through the functional test patterns at any rate or sequence that is convenient. After the logic has been verified, the part can be put back into the normal mode, and the PLL functions verified knowing that the rest of the chip is functional.

### Oscillator

The Am7968 and Am7969 contain an inverting amplifier intended to form the basis of a pierce oscillator. In designing this oscillator, it is necessary to consider several factors related to the application.

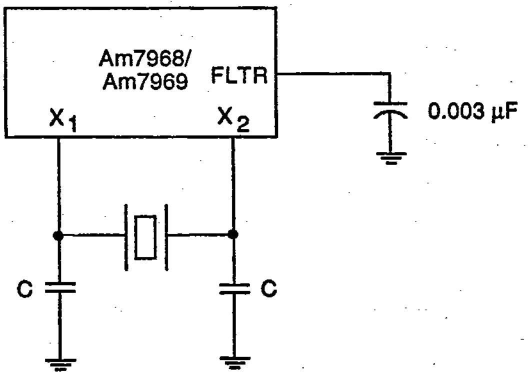
The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the TAXIchips is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystals are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO).

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained, crystal oscillators operate at their fundamental frequency.

A typical crystal specification for use in this circuit is:

| | |
|---|---|
| Frequency Range: | 4 - 12.5 MHz |
| Resonance: | Parallel Mode |
| Tolerance: | ±0.1% or to match system requirements |

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.




C = 150 pF for a 12.5-MHz Crystal,
220 pF for a 4-MHz Crystal.

**Figure 1. Connections for 4-12.5 MHz**

**TABLE 1. TAXIchip ENCODER PATTERNS**

| 4B/5B ENCODER SCHEME | | | 5B/6B ENCODER SCHEME | | |
|---|---|---|---|---|---|
| HEX Data | 4-Bit Binary Data | 5-Bit Encoded Symbol | HEX Data | 5-Bit Binary Data* | 6-Bit Encoded Symbol |
| 0 | 0000 | 11110 | 00 | 00000 | 110110 |
| 1 | 0001 | 01001 | 01 | 00001 | 010001 |
| 2 | 0010 | 10100 | 02 | 00010 | 100100 |
| 3 | 0011 | 10101 | 03 | 00011 | 100101 |
| 4 | 0100 | 01010 | 04 | 00100 | 010010 |
| 5 | 0101 | 01011 | 05 | 00101 | 010011 |
| 6 | 0110 | 01110 | 06 | 00110 | 010110 |
| 7 | 0111 | 01111 | 07 | 00111 | 010111 |
| 8 | 1000 | 10010 | 08 | 01000 | 100010 |
| 9 | 1001 | 10011 | 09 | 01001 | 110001 |
| A | 1010 | 10110 | 0A | 01010 | 110111 |
| B | 1011 | 10111 | 0B | 01011 | 100111 |
| C | 1100 | 11010 | 0C | 01100 | 110010 |
| D | 1101 | 11011 | 0D | 01101 | 110011 |
| E | 1110 | 11100 | 0E | 01110 | 110100 |
| F | 1111 | 11101 | 0F | 01111 | 110101 |
| | | | 10 | 10000 | 111110 |
| | | | 11 | 10001 | 011001 |
| | | | 12 | 10010 | 101001 |
| | | | 13 | 10011 | 101101 |
| | | | 14 | 10100 | 011010 |
| | | | 15 | 10101 | 011011 |
| | | | 16 | 10110 | 100001 |
| | | | 17 | 10111 | 011111 |
| | | | 18 | 11000 | 101010 |
| | | | 19 | 11001 | 101011 |
| | | | 1A | 11010 | 101110 |
| | | | 1B | 11011 | 101111 |
| | | | 1C | 11100 | 111010 |
| | | | 1D | 11101 | 111011 |
| | | | 1E | 11110 | 111100 |
| | | | 1F | 11111 | 111101 |

***Note:** HEX data is parallel input data which is represented by the 4- or 5-bit binary data listed in the column to the immediate right of HEX data. Binary bits are listed from left to right in the following order:

8-Bit Mode: $D_7$, $D_6$, $D_5$, $D_4$ (4-Bit Binary), and $D_3$, $D_2$, $D_1$, $D_0$ (4-Bit Binary)
9-Bit Mode: $D_8$, $D_7$, $D_6$, $D_5$, $D_4$ (5-Bit Binary), and $D_3$, $D_2$, $D_1$, $D_0$ (4-Bit Binary)
10-Bit Mode: $D_8$, $D_7$, $D_6$, $D_5$, $D_4$ (5-Bit Binary), and $D_9$, $D_3$, $D_2$, $D_1$, $D_0$ (5-Bit Binary)

Serial bits are shifted out with the most significant bit of the most significant nibble coming out first.

### TABLE 2. TAXIchip COMMAND DATA SYMBOLS

| Am7968 TRANSMITTER | | | | Am7969 RECEIVER | |
|---|---|---|---|---|---|
| Command Input | | Encoded Symbol | FDDI Meaning | Command Output | |
| HEX | Binary | | | HEX | Binary |
| **8-Bit TAXIs** | | | | | |
| 0 | 0000 | XXXXX XXXXX | Data | No Change (Note 3) | No Change (Note 3) |
| No STRB (Note 1) | No STRB (Note 1) | 11000 10001 | JK (8-bit Sync) | 0 | 0000 |
| 1 | 0001 | 11111 11111 | II | 1 | 0001 |
| 2 | 0010 | 01101 01101 | TT | 2 | 0010 |
| 3 | 0011 | 01101 11001 | TS | 3 | 0011 |
| 4 | 0100 | 11111 00100 | IH | 4 | 0100 |
| 5 | 0101 | 01101 00111 | TR | 5 | 0101 |
| 6 | 0110 | 11001 00111 | SR | 6 | 0110 |
| 7 | 0111 | 11001 11001 | SS | 7 | 0111 |
| 8 | 1000 | 00100 00100 | HH | 8 | 1000 |
| 9 | 1001 | 00100 11111 | HI | 9 | 1001 |
| A (Note 2) | 1010 | 00100 00000 | HQ | A | 1010 |
| B | 1011 | 00111 00111 | RR | B | 1011 |
| C | 1100 | 00111 11001 | RS | C | 1100 |
| D (Note 2) | 1101 | 00000 00100 | QH | D | 1101 |
| E (Note 2) | 1110 | 00000 11111 | QI | E | 1110 |
| F (Note 2) | 1111 | 00000 00000 | QQ | F | 1111 |
| **9-Bit TAXIs** | | | | | |
| 0 | 000 | XXXXXX XXXXX | Data | No Change (Note 3) | No Change (Note 3) |
| No STRB (Note 1) | No STRB (Note 1) | 011000 10001 | LK (9-bit Sync) | 0 | 000 |
| 1 | 001 | 111111 11111 | I'I | 1 | 001 |
| 2 | 010 | 011101 01101 | T'T | 2 | 010 |
| 3 | 011 | 011101 11001 | T'S | 3 | 011 |
| 4 | 100 | 111111 00100 | I'H | 4 | 100 |
| 5 | 101 | 011101 00111 | T'R | 5 | 101 |
| 6 | 110 | 111001 00111 | S'R | 6 | 110 |
| 7 | 111 | 111001 11001 | S'S | 7 | 111 |
| **10-Bit TAXIs** | | | | | |
| 0 | 00 | XXXXXX XXXXXX | Data | No Change (Note 3) | No Change (Note 3) |
| No STRB (Note 1) | No STRB (Note 1) | 011000 100011 | LM (10-bit Sync) | 0 | 00 |
| 1 | | 111111 111111 | I'I' | 1 | 01 |
| 2 | | 011101 011101 | T'T' | 2 | 10 |
| 3 | | 011101 111001 | T'S' | 3 | 11 |

Notes:
1. Command pattern Sync cannot be explicitly sent by Am7968 Transmitter with any combination of inputs and *STRB*, but is used to pad between user data.
2. These commands will disrupt Cascade Am7968 Transmitters and should be used only in Local mode.
3. A strobe with all 0s on the Command input lines will cause Data to be sent. See Table 1.

## Am7968 Transmitter Functional Block Description

### Crystal Oscillator/Clock Generator

The serial link speed is derived from a master frequency source (byte rate). This source can either be the built-in Crystal Oscillator, or a clock signal applied through the $X_1$ pin. This signal is buffered and sent to the *CLK* output when Am7968 Transmitter is in Local mode.

In Cascade mode, the Am7968 Transmitter *CLK* pin becomes an input and is always taken from the *CLK* output of the Am7968 that is farthest "downstream" and is in Local mode.

*CLK* input is multiplied by ten (8-bit mode), eleven (9-bit mode), or twelve (10-bit mode), using the internal PLL to create the bit rate.

The working frequency can be varied over a three-to-one range. The crystal frequency required to achieve 125 Mbaud/sec on the serial link, and the resultant usable data transfer rate will be:

| Mode | Crystal Frequency | Am7968 Input and Am7969 Maximum Parallel Throughput | Internal Divide Ratio |
|---|---|---|---|
| 8-Bit | 12.50 MHz | 80 ns/pattern (100 Mbit/sec) | 125/10 |
| 9-Bit | 11.36 MHz | 88 ns/pattern (102 Mbit/sec) | 125/11 |
| 10-Bit | 10.42 MHz | 96 ns/pattern (104 Mbit/sec) | 125/12 |

### Input Latch

The Am7968's Input Latch accommodates asynchronous strobing of Data and Command by being divided into two stages.

If *STRB* is asserted when both stages are empty, Data or Command bits are transferred directly to the second stage of the Input Latch and *ACK* rises shortly after *STRB*. This pattern is now ready to move to the Encoder Latch at the next falling edge of *CLK*.

An input pattern is strobed into the first stage of the Input Latch only when the second stage is BUSY (contains previously stored data). The Transmitter will be BUSY when *STRB* is asserted a second time in a given *CLK* cycle. Contents of the first stage are not protected from subsequent *STRBs* within the same *CLK* cycle. At the falling edge of *CLK*, previously stored data is transferred from the second stage to the Encoder Latch and the new data is clocked into the second stage of the Input Latch. If in Local mode, *ACK* will rise at this time.

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### Encoder Latch

Input to the Encoder Latch is clocked by an internal signal which is synchronous with the shifted byte being sent on the serial link. Whenever a new input pattern is strobed into the Input Latch, the data is transferred to the Encoder Latch at the next opportunity.

### Data Encoder

Encodes twelve data inputs (8, 9, 10 Data bits or 4, 3, 2 Command inputs) into 10, 11, or 12 bits. The Command data inputs control the transmitted symbol. If all Command inputs are LOW, the symbol for the Data bits will be sent. If Command inputs have any other pattern then the symbol representing that Command will be transmitted.

### Shifter

The Shifter is parallel loaded from the Encoder at the first available byte boundary, and then shifted until the next byte boundary. The Shifter is serially loaded at all times, but if a parallel load is required, it over-writes the serial data before it appears at the Media interface. The serial data which is loaded into the Shifter will come from one of two sources:

1. If the Am7968 Transmitter is receiving good data at its *SERIN* input, then the serial data will come from the external serial input.
2. If the Am7968 Transmitter is not receiving good data (good data never has five consecutive 0s), then the serial data will be generated by an internal state machine which generates a repeating Sync pattern.

### Serial Interface

The Serial Interface is a level-restoring buffer in Cascade mode. In Local mode it generates the Sync symbol to pad the spaces between user-data patterns.

### Media Interface

The Media Interface is differential ECL, referenced to +5 V. It is capable of driving 50-Ω terminated lines.

## Am7969 Receiver Functional Block Description

### Crystal Oscillator/Clock Generator

The serial link speed of the Am7969 Receiver must be the same data rate used by the Transmitter's oscillator and is derived from a master frequency source (byte rate). This source can either be the built-in Crystal Oscillator, or a clock signal applied through the $X_1$ pin. The frequency source is then multiplied by ten (8-bit mode), eleven (9-bit mode) or twelve (10-bit mode) using an internal PLL.

### Media Interface

*SERIN+*, *SERIN−* inputs are to be driven by differential ECL voltages, referenced to +5 V. These inputs serve both as a serial data input, and a reference for PLL tracking.

### PLL Clock Generator

A PLL Clock Generator recovery loop follows the incoming data and allows the encoded clock and data stream to be decoded into a separated clock and data pattern. Its center frequency is determined by the Crystal Oscillator and Clock Generator and is capable of tracking data with frequency offsets of ±0.1% and with up to ±40% bit time jitter.

### Shifter

The Shifter is serially loaded from the Media Interface, using the bit clock generated by PLL.

### Byte Sync Logic

The incoming data stream is a continuous stream of data bits, without any significant signal which denotes byte boundaries. This logic will continuously monitor the data stream, and upon discovering the reserved code used for Am7969 Receiver Sync, initialize a synchronous counter which counts bits, and indicates byte boundaries.

The logic signal that times data transfers from the Shifter to the Decoder Latch is buffered and sent to the *CLK* output to be used by other Am7969 Receivers, or for other on-card clock functions. This output is synchronous with the byte boundary and is synchronous with the Receivers's byte clock.

Byte Sync Logic is responsible for generating the strobe signals for Parallel Output Latches. It also generates the *IGM* (I-Got-Mine) signal when the first byte after a Sync symbol is transferred. Parallel outputs are made on a byte boundary, when *CNB* falls, or when Sync is detected.

The I-Got-Mine (*IGM*) signal will fall when the first half of a Sync is detected in the Shifter or when *CNB* goes LOW. It will remain LOW until the first half of a non-Sync byte is detected in the Shifter, whereupon it will rise (assuming that the *CNB* input is HIGH). A continuous stream of normal data or command bytes will cause *IGM* to go HIGH and remain HIGH. A continuous stream of Sync's will cause *IGM* to stay LOW. *IGM* will go HIGH during the byte before data appears at the output. This feature could be used to generate an early warning of incoming data.

**Decoder Latch**

Data is loaded from the Shifter to this latch at each symbol/byte boundary. It serves as the input to the Data Decoder.

**Data Decoder**

Decodes ten, eleven or twelve data inputs into twelve outputs. In 8-bit mode, data is decoded into either an 8-bit Data pattern or a 4-bit Command pattern. In 9-bit mode, data is decoded into either a 9-bit Data pattern or a 3-bit Command pattern. In 10-bit mode, data is decoded into either a 10-bit Data pattern or a 2-bit Command pattern.

The decoder separates Data symbols from Command symbols, and causes the appropriate strobe output to be asserted.

**Parallel Output Latch** T-75-37-05

Output Latch will be clocked by the byte clock, and will reflect the most recent data on the link. Any Data pattern will be latched to the Data outputs and will not affect the status of the Command outputs. Likewise, any Command pattern will be latched to the Command outputs without affecting the state of the Data outputs.

Any data transfer, either Data or Command will be synchronous with an appropriate output strobe. However, there will be *CSTRBs* when there is no active data on the link, since sync is a valid Command code.

Any pattern which does not decode to a valid Command or Data pattern is flagged as a violation. The output of the decoder during these violations is indeterminate and will result in either a *CSTRB* or *DSTRB* output when the indeterminate pattern is transferred to the output latch.

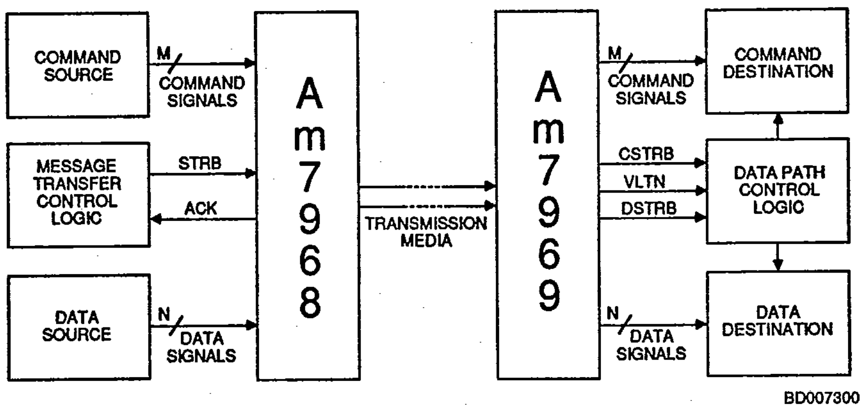


**Figure 2. TAXIchip System Block Diagrams**

Note: N can be 8, 9, or 10 bits
Total of M + N = 12

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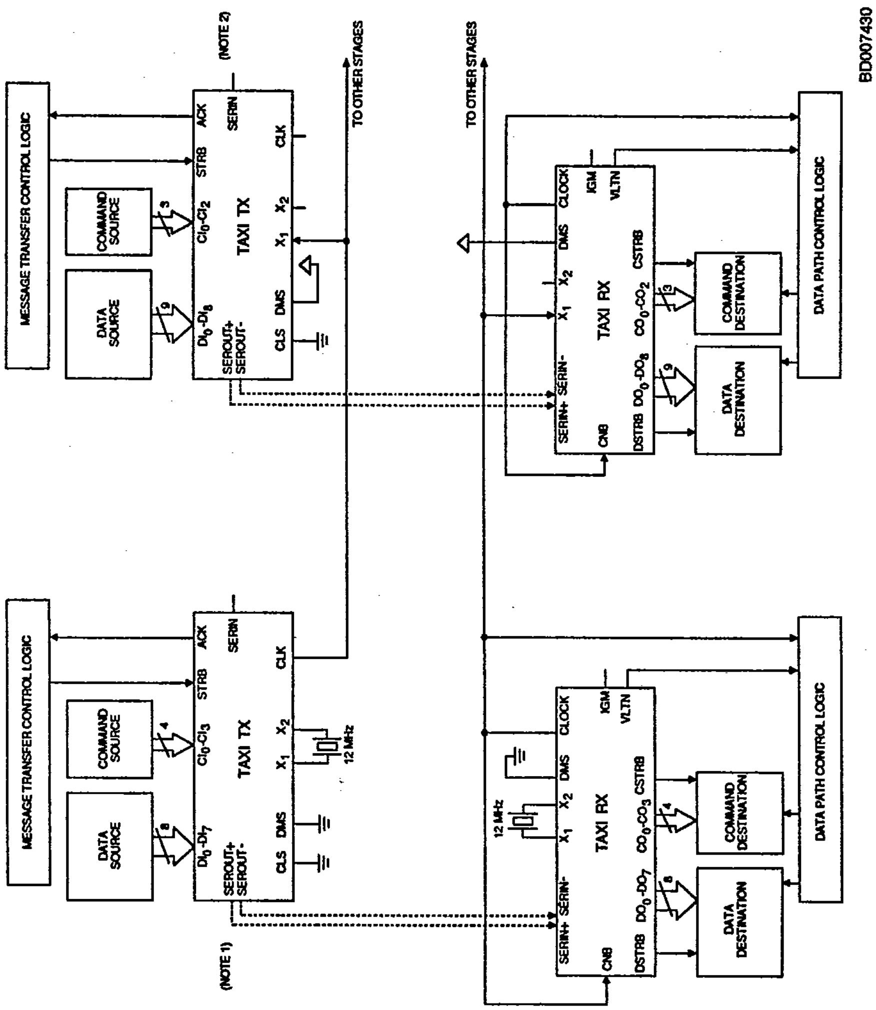


**Figure 3. TAXIchip System in Local Mode**

Notes 1. DMS = GND = 8-Bit Mode
CLS = GND = Local Mode
SERIN = OPEN = Local Mode
2. DMS = $V_{CC}$ = 9-Bit Mode
CLS = GND = Local Mode
SERIN = OPEN = Local Mode

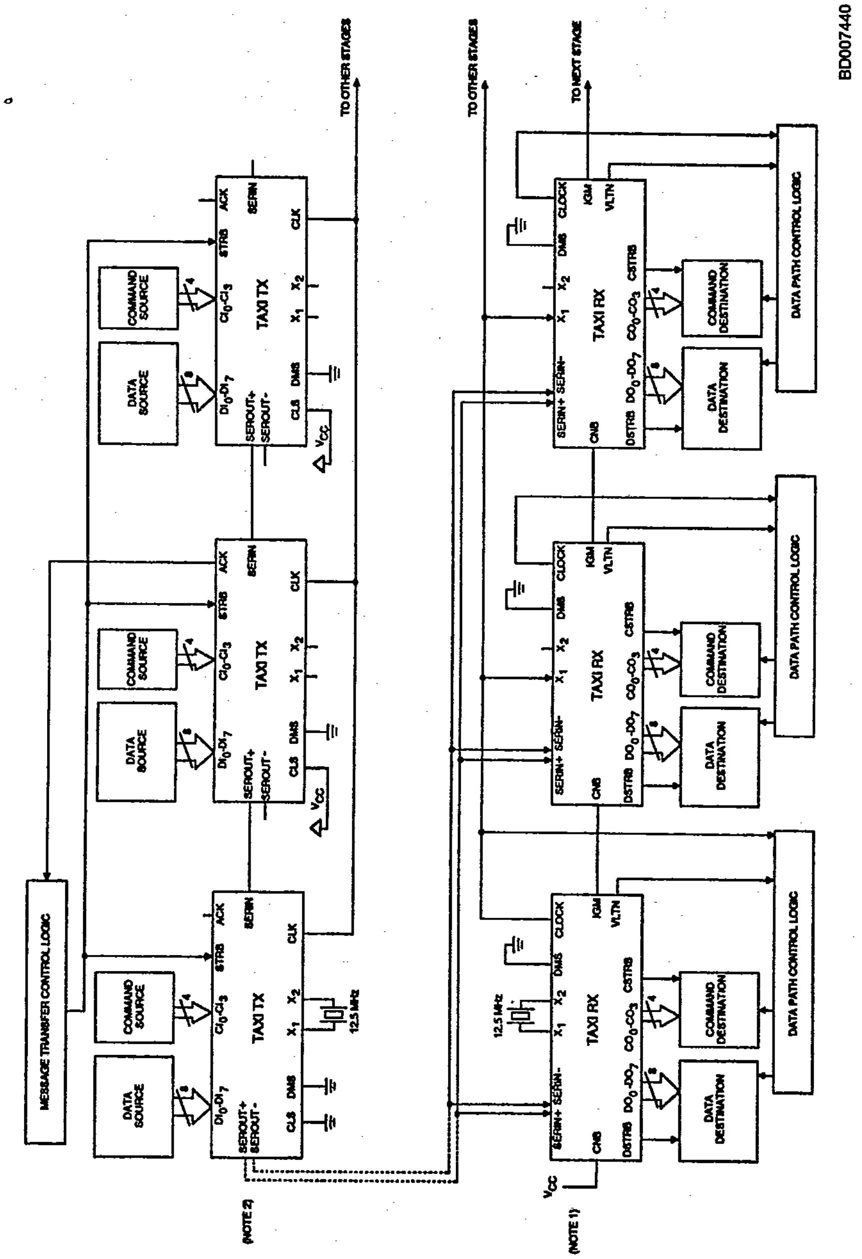


**Figure 4. TAXIchip System In Cascade Mode**

Notes 1. For Receiver
DMS = GND = 8-Bit Mode
2. For Transmitter
DMS = GND = 8-Bit Mode
CLS = $V_{CC}$ = Cascade Mode
CLS = GND = Local Mode

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ............................. −65 to +150°C
Ambient Temperature Under Bias ............ −55 to +125°C
Supply Voltage to Ground
Potential Continuous ........................... −0.5 to +7.0 V
DC Voltage Applied to Outputs ......... −0.5 V to $V_{CC}$ Max.
DC Input Voltage ................................ −0.5 to +5.5 V
DC Output Current ...................................... ±100 mA
DC Input Current .............................. −30 to +5.0 mA

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ($T_A$) ................................. 0 to +70°C
Supply Voltage ($V_{CC}$) ....................... +4.5 to +5.5 V

Military (M) Devices
Temperature ($T_A$) ............................ −55 to +125°C
Supply Voltage ($V_{CC}$) ....................... +4.5 to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

**Am7968 TAXIchip Transmitter**

| Parameter Symbols | Parameter Descriptions | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DI_0$ − $DI_7$, $DI_8/CI_3$, $DI_9/CI_2$, $CI_0$ − $CI_1$, STRB, ACK, CLK** | | | | | | | |
| $V_{OH1}$ | Output HIGH Voltage ACK | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OH}$ = −1 mA | 2.4 | | | V |
| $V_{OH2}$ | Output HIGH Voltage CLK | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OH}$ = −1 mA | 2.4 | | | V |
| $V_{OL1}$ | Output LOW Voltage ACK | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OL}$ = 8 mA | | | 0.45 | V |
| $V_{OL2}$ | Output LOW Voltage CLK | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OL}$ = 16 mA | | | 0.45 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. (Note 9) | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. (Note 9) | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min. | $I_{IN}$ = −18 mA | | | −1.5 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4 V | | | | −400 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_I$ | Input Leakage Current | $V_{CC}$ = Max., | All Inputs Except CLK | | | 50 | μA |
| | | $V_{IN}$ = 5.5 V | CLK Input | | | 150 | |
| $I_{SC1}$ | Output Short Circuit Current ACK (Note 4) | $V_{CC}$ = Max. | | −15 | | −85 | mA |
| $I_{SC2}$ | Output Short Circuit Current CLK (Note 4) | $V_{CC}$ = Max. | | −30 | | −100 | mA |

Table continued on next page.
Notes: See notes following end of Switching Characteristics tables.

**Am7968 TAXIchip Transmitter (Cont'd.)**

| Parameter Symbols | Parameter Descriptions | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Serial Interface Signals: SERIN, SERIN+, SERIN–** | | | | | | | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. ECL Load | | $V_{CC}$ –1.025 | | $V_{CC}$ –0.88 | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. ECL Load | | $V_{CC}$ –1.81 | | $V_{CC}$ –1.62 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. | | $V_{CC}$ –1.165 V | | $V_{CC}$ –0.88 V | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. | | $V_{CC}$ –1.81 V | | $V_{CC}$ –1.475 V | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ – 1.81 V | | 0.5 | | | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ – 0.88 V | | | | 220 | μA |
| **Miscellaneous Signals: $X_1$, $V_{CC1}$ – $V_{CC3}$** | | | | | | | |
| $V_{IHX}$ | Input HIGH Voltage $X_1$ | | | TBD | | | V |
| $V_{ILX}$ | Input LOW Voltage $X_1$ | | | | | TBD | V |
| $I_{ILX}$ | Input LOW Current $X_1$ | $V_{IN}$ = 0 V | | | | –1.2 | mA |
| $I_{IHX}$ | Input HIGH Current $X_1$ | $V_{IN}$ = 3.5 V | | | | +1.2 | mA |
| $I_{CC}$ | Supply Current | CLS = GND, SEROUT = ECL Load, DMS = 0 or 3 V, $V_{CC1}$ = $V_{CC2}$ = $V_{CC3}$ = Max. | Pin $V_{CC1}$ (TTL) | | 25 | | mA |
| | | | Pin $V_{CC2}$ (ECL) | | 19 | | mA |
| | | | Pin $V_{CC3}$ (CML) | | 84 | | mA |

Notes: See notes following end of Switching Characteristics tables.

**Am7969 TAXIchip Receiver**

| Parameter Symbols | Parameter Descriptions | Test Conditions (Note 1) | | Min. | Typ. (Note 2) | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DO_0-DO_7$, $DO_8/CO_3$, $DO_9/CO_2$, $CO_0-CO_1$, DSTRB, CSTRB, IGM, CLK, CNB, VLTN** | | | | | | | |
| $V_{OH1}$ | Output HIGH Voltage (All outputs except CLK) | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OH}$ = −1 mA | 2.4 | | | V |
| $V_{OH2}$ | Output HIGH Voltage CLK | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OH}$ = −1 mA | 2.4 | | | V |
| $V_{OL1}$ | Output LOW Voltage (All outputs except CLK) | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OL}$ = 8 mA | | | 0.45 | V |
| $V_{OL2}$ | Output LOW Voltage CLK | $V_{CC}$ = Min., $V_{IN}$ = 0 or 3 V | $I_{OL}$ = 16 mA | | | 0.45 | V |
| **Bus Interface Signals** (Cont'd.) | | | | | | | |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = Max. (Note 9) | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = Max. (Note 9) | | | | 0.8 | V |
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min. | $I_{IN}$ = −18 mA | | | −1.5 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = 0.4 V | | | | −400 | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = 2.7 V | | | | 50 | μA |
| $I_I$ | Input Leakage Current | $V_{CC}$ = Max., $V_{IN}$ = 5.5 V | | | | 50 | μA |
| $I_{SC1}$ | Output Short Circuit Current (All outputs except CLK) (Note 4) | $V_{CC}$ = Max. | | −15 | | −85 | mA |
| $I_{SC2}$ | Output Short Circuit Current CLK (Note 4) | $V_{CC}$ = Max. | | −15 | | −100 | mA |
| **Serial Interface Signals: SERIN+, SERIN−** | | | | | | | |
| $V_{IHS}$ | Input HIGH Voltage SERIN+ | $V_{CC}$ = Min. (Note 9) | | $V_{CC}$ −1.165 | | $V_{CC}$ −0.88 | V |
| $V_{ILS}$ | Input LOW Voltage SERIN+ | $V_{CC}$ = Max. (Note 9) | | $V_{CC}$ −1.81 | | $V_{CC}$ −1.475 | V |
| $V_{THT}$ | Test Mode Threshold SERIN− | $V_{CC}$ = Max. (Note 9) | | | | 1.5 | V |
| $V_{DIF}$ | Differential Input Voltage | $V_{CC}$ = Max. | | 0.3 | | 1.1 | V |
| $V_{ICM}$ | Input Common Mode Voltage | (Note 6) | | 3.05 | | $V_{CC}$ −0.55 | V |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN} = V_{CC} - 1.81$ V | | 0.5 | | | μA |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN} = V_{CC} - 0.88$ V | SERIN+ | | | 220 | μA |
| | | | SERIN− | | | 800 | |
| **Miscellaneous Signals: $X_1$, $V_{CC1}$, $V_{CC2}$** | | | | | | | |
| $V_{IHX}$ | Input HIGH Threshold $X_1$ | | | TBD | | | V |
| $V_{ILX}$ | Input LOW Threshold $X_1$ | | | | | TBD | V |
| $I_{ILX}$ | Input LOW Current $X_1$ | $V_{IN}$ = 0 V | | | | −1.2 | mA |
| $I_{IHX}$ | Input HIGH Current $X_1$ | $V_{IN}$ = 3.5 V | | | | +1.2 | mA |
| $I_{CC}$ | Supply Current | $V_{CC1} = V_{CC2}$ = Max., SERIN− > 2.5 V (Note 6) | Pin $V_{CC1}$(TTL) | | 37 | | mA |
| | | | Pin $V_{CC2}$(CML) | | 128 | | |

Notes: See notes following end of Switching Characteristics tables.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 20)

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**Am7968 TAXIchip Transmitter**

| No. | Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DI_0-DI_7$, $DI_8/CI_3$, $DI_9/CI_2$, $CI_0-CI_1$, STRB, ACK, CLK** | | | | | | | |
| 1 | $t_P$ | CLK Period | | 80 | | 250 | ns |
| 2 | $t_{PW}$ | CLK Pulse Width HIGH | | 30 | | | ns |
| 3 | $t_{PW}$ | CLK Pulse Width LOW | | 30 | | | ns |
| 4 | $t_{PW}$ | STRB Pulse Width HIGH (Note 7) | | 15 | | | ns |
| 5 | $t_{PW}$ | STRB Pulse Width LOW | | 15 | | | ns |
| 6 | $t_U$ | Pre CLK Uncertainty Time (Notes 10 & 11) | | | | 5 | ns |
| 7 | $t_U$ | Post CLK Uncertainty Time (Notes 10 & 11) | | | | $\frac{t_1}{n}+10$ | ns |
| 8 | $t_P$ | STRB Period (Note 17) | | $(3 \times t_1/n)$ | | | ns |
| 9 | $t_S$ | Data-STRB Setup Time | | 5 | | | ns |
| 10 | $t_H$ | Data-STRB Hold Time | | 10 | | | ns |
| 11 | $t_H$ | ACK ↑ to STRB ↓ Hold (Note 8) | TTL Output Load | 0 | | | ns |
| 12 | $t_H$ | ACK ↓ to STRB ↑ Hold | TTL Output Load | 0 | | | ns |
| 13 | $t_{PD}$ | STRB ↑ to ACK ↑ | TTL Output Load | | | 35 | ns |
| 14 | $t_{PD}$ | STRB ↓ to ACK ↓ | TTL Output Load | | | 20 | ns |
| 15 | $t_{PD}$ | CLK ↓ to ACK ↑ (Note 18) | TTL Output Load | | | $\frac{t_1}{n}+25$ | ns |
| 16 | $t_R$ | ACK Rise Time (Note 3) | TTL Output Load | | | 17 | ns |
| 17 | $t_F$ | ACK Fall Time (Note 3) | TTL Output Load | | | 10 | ns |
| 18 | $t_R$ | CLK Rise Time (Note 3) | TTL Output Load | | | 17 | ns |
| 19 | $t_F$ | CLK Fall Time (Note 3) | TTL Output Load | | | 10 | ns |
| **Serial Interface Signals: SERIN, SEROUT+, SEROUT−** | | | | | | | |
| 20 | $t_{PD}$ | CLK ↓ to SEROUT± Delay | ECL Output Load | TBD | | | ns |
| 22 | $t_{SK}$ | SEROUT± Skew | ECL Output Load | −200 | | +200 | ps |
| 23 | $t_R$ | SEROUT± Output Rise Time | ECL Output Load | | 2.0 | | ns |
| 24 | $t_F$ | SEROUT± Output Fall Time | ECL Output Load | | 2.0 | | ns |
| 25 | $t_S$ | SERIN to CLK ↓ Setup Time | ECL Output Load | $\frac{-t_1}{2n}$ | | $\frac{t_1}{2n}$ | ns |
| 26 | $t_{PW}$ | SEROUT ± Pulse Width LOW | ECL Output Load | $\frac{t_1}{n}-3\%$ | | $\frac{t_1}{n}+3\%$ | ns |
| 27 | $t_{PW}$ | SEROUT ± Pulse Width HIGH | ECL Output Load | $\frac{t_1}{n}-3\%$ | | $\frac{t_1}{n}+3\%$ | ns |
| **Miscellaneous Signals: $X_1$ (Note 15)** | | | | | | | |
| 29 | $t_{PW}$ | $X_1$ Pulse Width HIGH (Note 12) | TTL Output Load on CLK | 35 | | | ns |
| 30 | $t_{PW}$ | $X_1$ Pulse Width LOW (Note 12) | TTL Output Load on CLK | 35 | | | ns |
| 32 | $t_{PD}$ | $X_1$ ↑ to CLK ↑ | TTL Load | | | 20 | ns |
| 33 | $t_{PD}$ | $X_1$ ↓ to CLK ↓ | TTL Load | | | 20 | ns |

Note: See notes following end of Switching Characteristics tables.

**Am7969 TAXIchip Receiver** T-75-37-05

| No. | Parameter Symbol | Parameter Description | Test Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| **Bus Interface Signals: $DO_0-DO_7$, $DO_8/CO_3$, $DO_9/CO_2$, DSTRB, CSTRB, IGM, CLK, CNB, VLTN.** | | | | | | | |
| 35 | $t_P$ | $X_1$ Clock Period | | 80 | | 250 | ns |
| 36 | $t_{PD}$ | Data Valid to STRB ↑ Delay (Notes 13 & 14) | TTL Output Load | $\frac{t_{35}}{n}$ | | | ns |
| 37 | $t_{PD}$ | CLK ↓ to STRB ↑ (Note 14) | TTL Output Load | | | $\left(\frac{2t_{35}}{n}+15\right)$ | ns |
| 38 | $t_{PD}$ | CLK ↑ to STRB ↓ | TTL Output Load | $\frac{t_{35}}{n}-5$ | | | ns |
| 39 | $t_{PD}$ | CLK ↓ to Data Valid Delay | TTL Output Load | | | 15 | ns |
| 41 | $t_{PW}$ | CLK Pulse Width HIGH (Note 14) | TTL Output Load | $(5 \times t_{35}/n) - 15$ | | | ns |
| 42 | $t_{PW}$ | CLK Pulse Width LOW (Note 14) | TTL Output Load | $(5 \times t_{35}/n) - 15$ | | | ns |
| 43 | $t_{PD}$ | SERIN to CLK ↓ Delay | TTL Output Load | TBD | | TBD | ns |
| 44 | $t_{PD}$ | CLK ↑ to IGM ↓ (Note 14) | TTL Output | | | $\frac{t_{35}}{n}+15$ | ns |
| 45 | $t_{PD}$ | CLK ↑ to IGM ↑ (Note 14) | TTL Output | | | $\frac{3t_{35}}{2n}+5$ | ns |
| 46 | $t_{PD}$ | CNB ↓ to IGM ↓ | TTL Output | | | 20 | ns |
| 47 | $t_S$ | CNB ↑ to CLK ↑ Setup Time (Note 5) | | $-\left(\frac{t_{35}}{n}-15\right)$ | | | ns |
| 47A | $t_S$ | CNB ↓ to CLK ↑ Setup Time (Note 14) | | $-\left(\frac{t_{35}}{n}-15\right)$ | | | ns |
| 48 | $t_H$ | CNB ↓ to CLK ↑ Hold | | $\left(\frac{t_{35}}{n}+15\right)$ | | | ns |
| 49 | $t_{PW}$ | CNB Pulse Width LOW | | 15 | | | ns |
| 50 | $t_R$ | STRB Rise Time (Note 3) | | | | 17 | ns |
| 51 | $t_F$ | STRB Fall Time (Note 3) | | | | 10 | ns |
| 52 | $t_R$ | CLK Rise Time (Note 3) | | | | 17 | ns |
| 53 | $t_F$ | CLK Fall Time (Note 3) | | | | 10 | ns |
| **Serial Interface Signals: SERIN+, SERIN−** | | | | | | | |
| 57 | $t_J$ | SERIN± Input Jitter (Note 16) | | $-0.4 \times \frac{t_{35}}{n}$ | | $+0.4 \times \frac{t_{35}}{n}$ | ns |
| **Miscellaneous: $X_1$ (Note 15)** | | | | | | | |
| 60 | $t_{PW}$ | $X_1$ Pulse Width HIGH | | 35 | | | ns |
| 61 | $t_{PW}$ | $X_1$ Pulse Width LOW | | 35 | | | ns |

Notes: See notes following Switching Characteristics tables.

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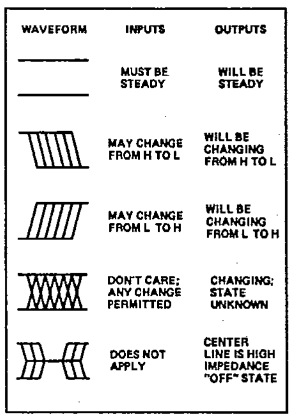
Notes:* 1. For conditions shown as Min., or Max, use the appropriate value specified under operating range.
2. Typical limits are at $V_{CC} = 5.0$ V, 25°C ambient and maximum loading.
3. Rise and fall time measurements are made at 20% and 80% points.
4. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
5. If the CNB ↑ to CLK ↑ setup time is violated, IGM will stay LOW.
6. Voltage applied to either SERIN± pins must not be above $V_{CC}$ or below +2.5 V to assure proper operation.
7. $t_4$ guarantees that data is latched. ACK ($t_{11}$) timing may not be valid.
8. If $t_{11}$ is not met, ACK response and timing are not guaranteed, but data will still be latched on STRB ↑ (see $t_4$).
9. Measured with device in Test mode while monitoring output logic states.
10. 'n' is determined by the state of DMS and CLS inputs. When CLS is OPEN, n = 1. When CLS is either HIGH or LOW and when: DMS is LOW, n = 10,
DMS is HIGH, n = 11,
DMS is OPEN, n = 12
11. If STRB occurs outside the Uncertainty Zone ($t_6$ and $t_7$ are satisified), then STRB-ACK Delay is defined by $t_{13}$ if the Input Latch is empty, or by $t_{15}$ if the Input Latch is BUSY. If STRB occurs inside the Uncertainty Zone ($t_6$ or $t_7$ violated), the ACK Delay may be defined by either $t_{13}$ or $t_{15}$.
12. $X_1$ Pulse Width is measured at a point where CLK output exactly meets CLK input ($t_2$ or $t_3$) spec limit.
13. 'STRB' is either DSTRB or CSTRB. 'Data' is either Data or Command.
14. 'n' is determined by the state of DMS and SERIN– inputs. When SERIN– is strapped to GND, n = 1. When SERIN– is OPEN or above 1.5 V and when: DMS is LOW, n = 10,
DMS is HIGH, n = 11,
DMS is OPEN, n = 12
15. Crystal frequency should be between 4 MHz and 12.5 MHz a tolerance of ±0.1%. Jitter on the $X_1$ input must be less than ±0.2 ns.
16. This specification applies to any edge of an incoming pattern.
17. $t_8$ is a restriction only if $t_6$ or $t_7$ are violated.
18. ACK delay is determined by $t_{15}$ only when Busy (input latch is full), in Cascade mode, or when $t_6$ or $t_7$ are violated.
19. If the CNB ↓ to CLK ↑ setup time is violated, then data will be output one byte time later.
20. All timing references are made with respect to +1.5 V for TTL-level signals or to the 50% point between $V_{OH}$ and $V_{OL}$ for ECL signals. ECL input rise and fall times must be 2 ns ± 0.2 ns between 20% and 80% points. TTL input rise and fall times must be 2 ns between 1 V and 2 V.

* Notes listed correspond to the respective references made in the DC Characteristics and the Switching Characteristics tables.

## KEY TO SWITCHING WAVEFORMS

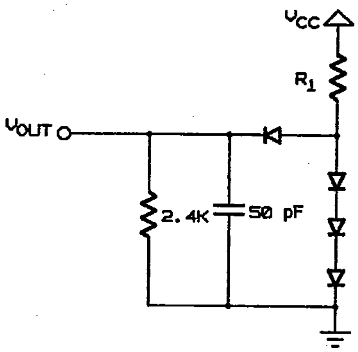



KS000010

## SWITCHING TEST CIRCUITS

T-75-37-05

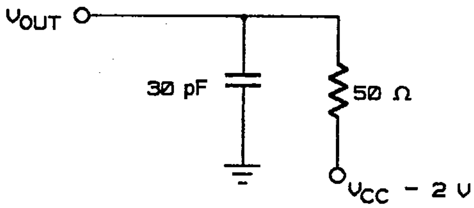
### TTL Output Load




TC002820

Notes: 1. $R_1$ = 500 Ω for the $I_{OL}$ = 8 mA and $R_1$ = 250 Ω for the $I_{OL}$ = 16 mA
2. All diodes IN916 or IN3064, or equivalent
3. $C_L$ = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
4. AMD uses ATE load configurations and forcing functions. This figure is for reference only.

### ECL Output Load

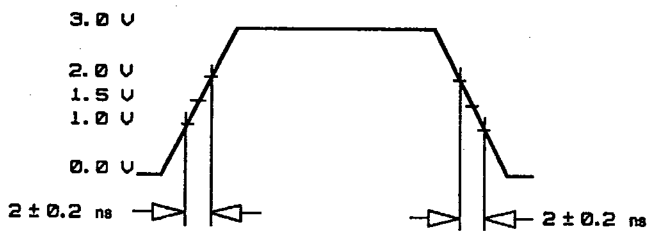



TC002831

Notes: 1. $C_L$ = 30 pF includes scope probe, wiring and stray capacitances without device in text fixture.
2. AMD uses ATE load configurations and forcing functions. This figure is for reference only.

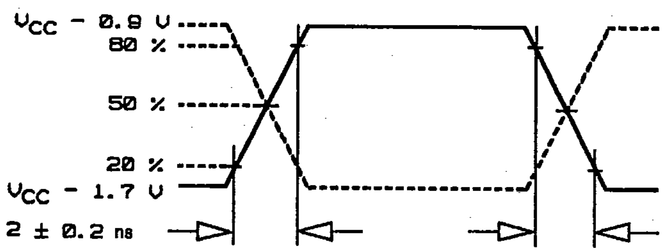
## SWITCHING TEST WAVEFORMS

### TTL Input Waveform




WF020272

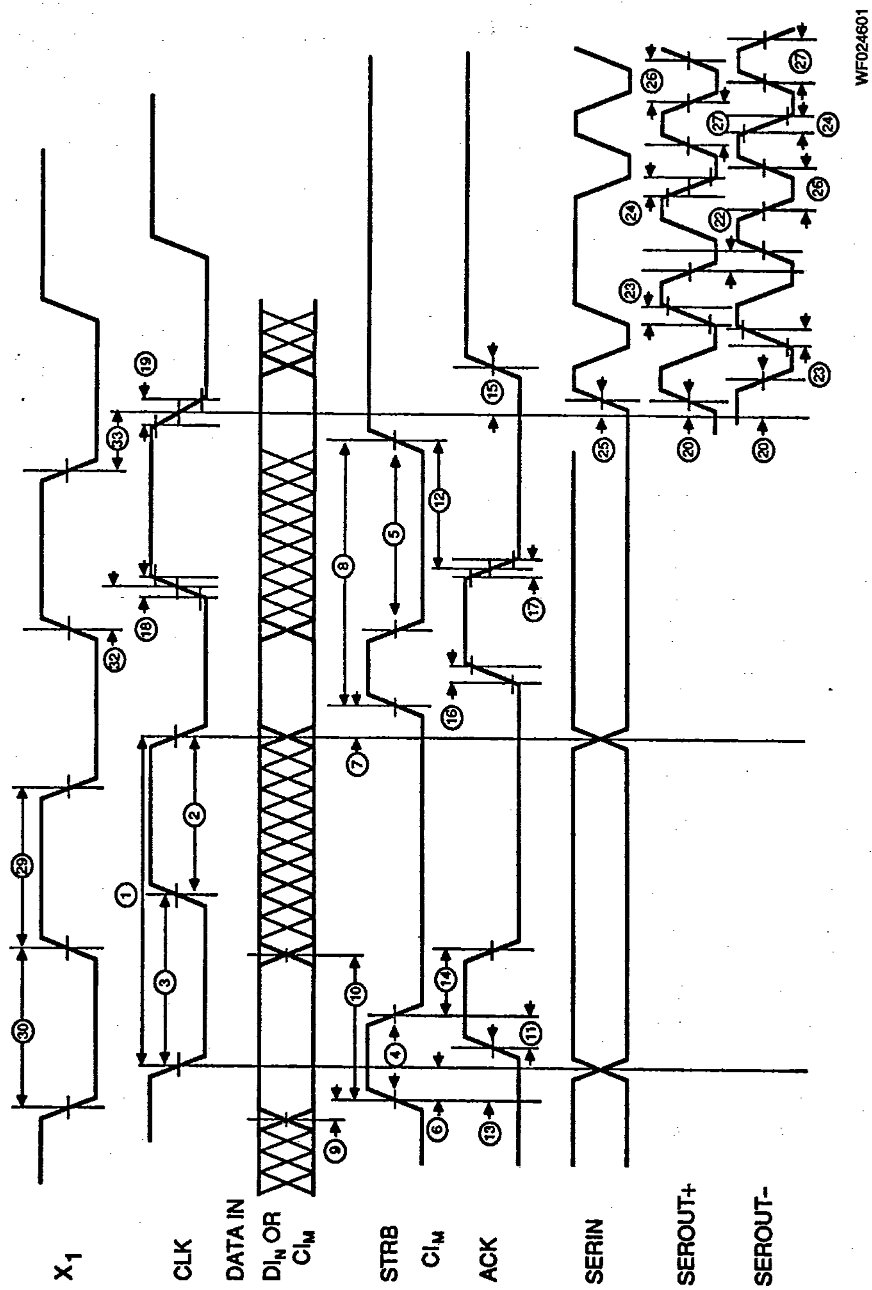
### ECL Input Waveform



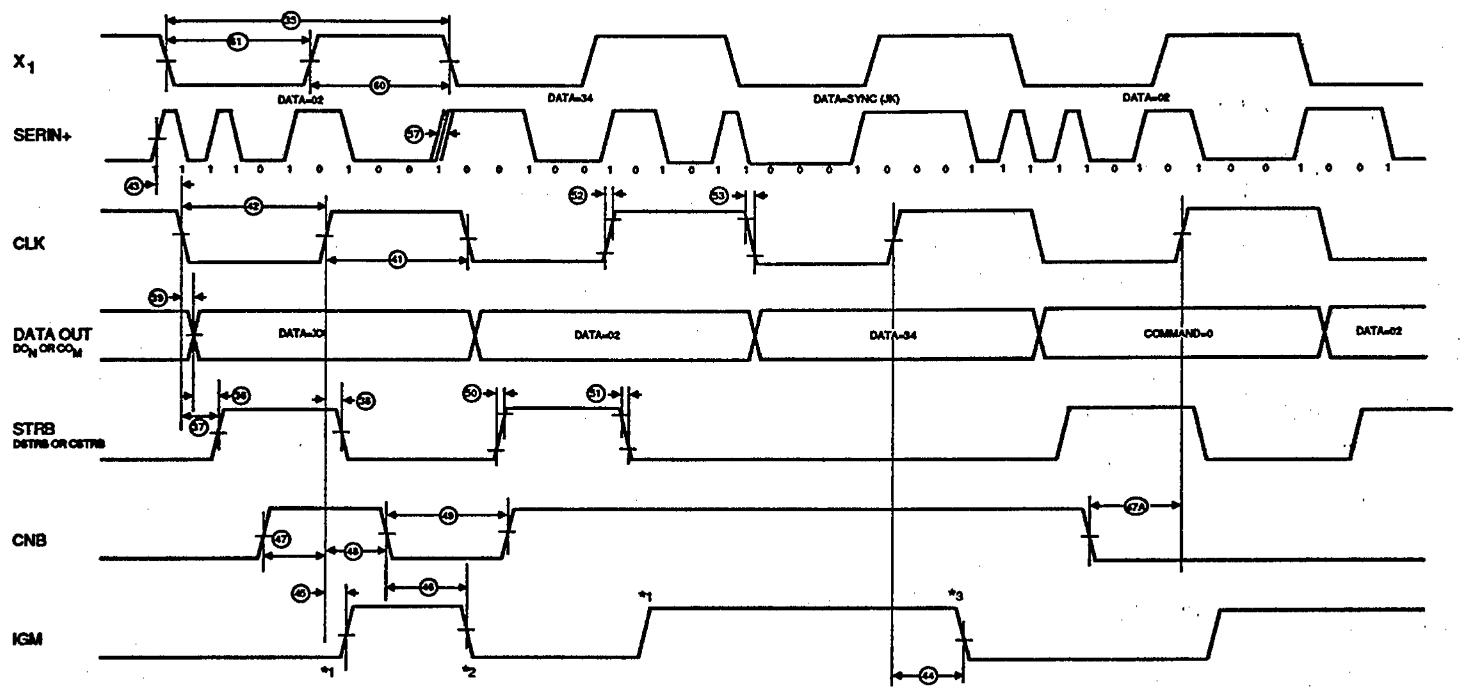

WF020282

## SWITCHING WAVEFORMS

**Am7968 TAXIchip Transmitter**



## Am7969 TAXIchip Receiver

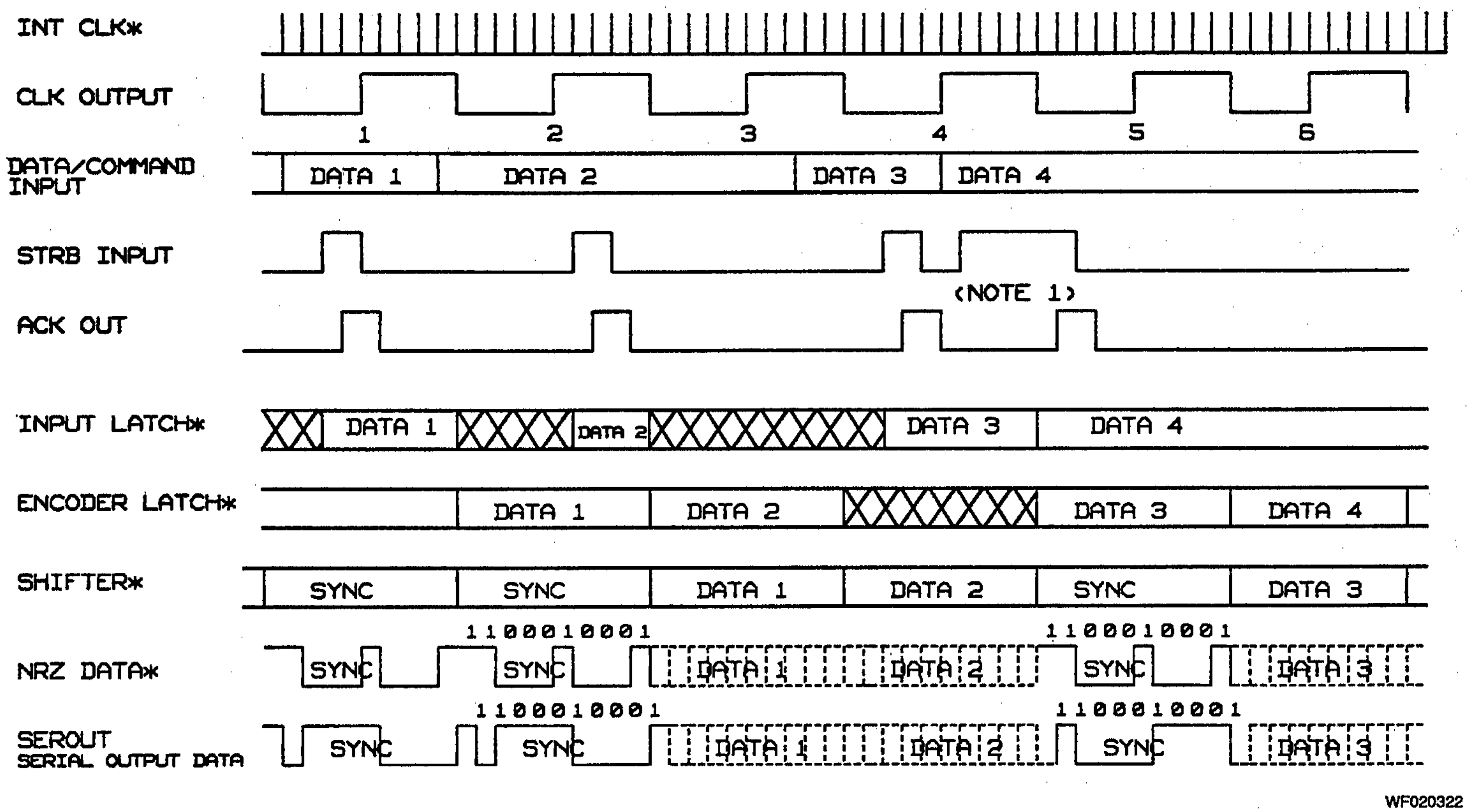



*1 IGM RISES BECAUSE CNB = 1 & SERIN = FIRST HALF OF NON-SYNC BYTE
*2 IGM FALLS BECAUSE CNB FALLS
*3 IGM FALLS BECAUSE SERIN = FIRST HALF OF SYNC BYTE

Note: This diagram illustrates how timing relationships are measured. Functional operation is clarified on following pages.

## SWITCHING WAVEFORMS (Cont'd.)

**TAXIchip Transmitter**

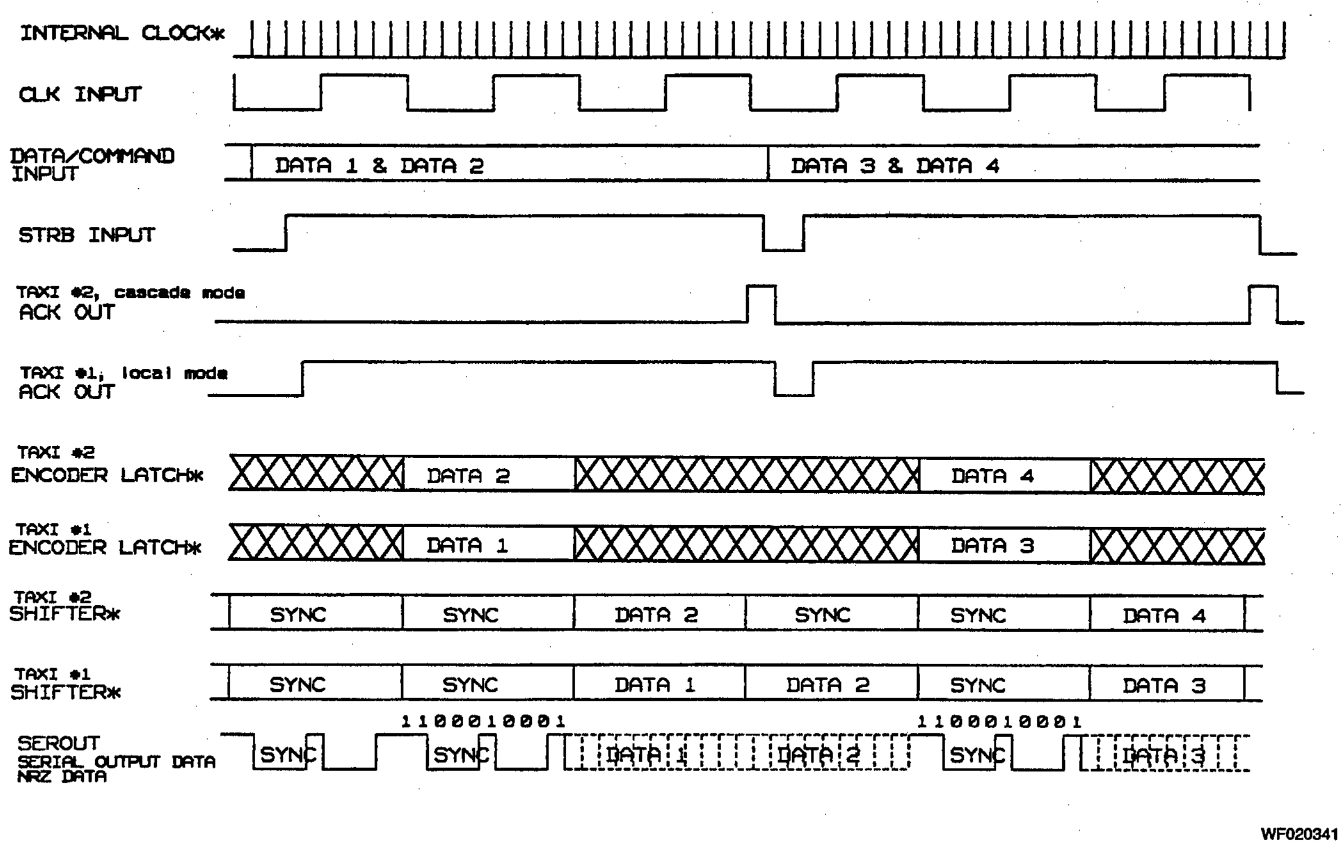



**STRB to SEROUT Timing**
**(8-Bit Local Mode)**
*Internal Signals

Notes: 1. The Input Latch is BUSY when the second STRB comes in; the Internal STRB-ACK is delayed until the next CLK window.

## SWITCHING WAVEFORMS (Cont'd.)

### TAXIchip Transmitter (Cont'd.)

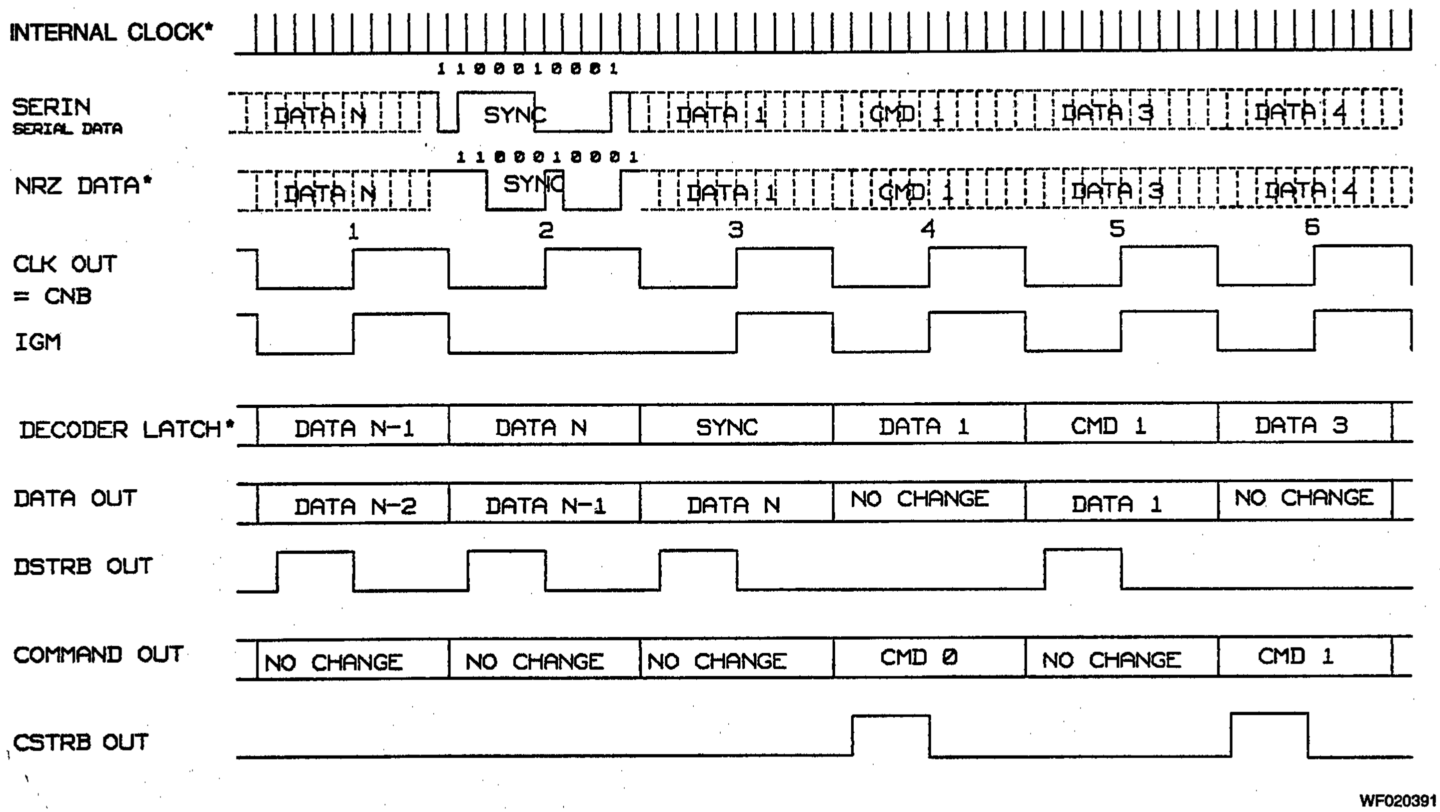



**STRB to SEROUT Timing**
**(8-Bit Cascade Mode)**

*Internal Signals

## SWITCHING WAVEFORMS (Cont'd.)

### TAXIchip Receiver

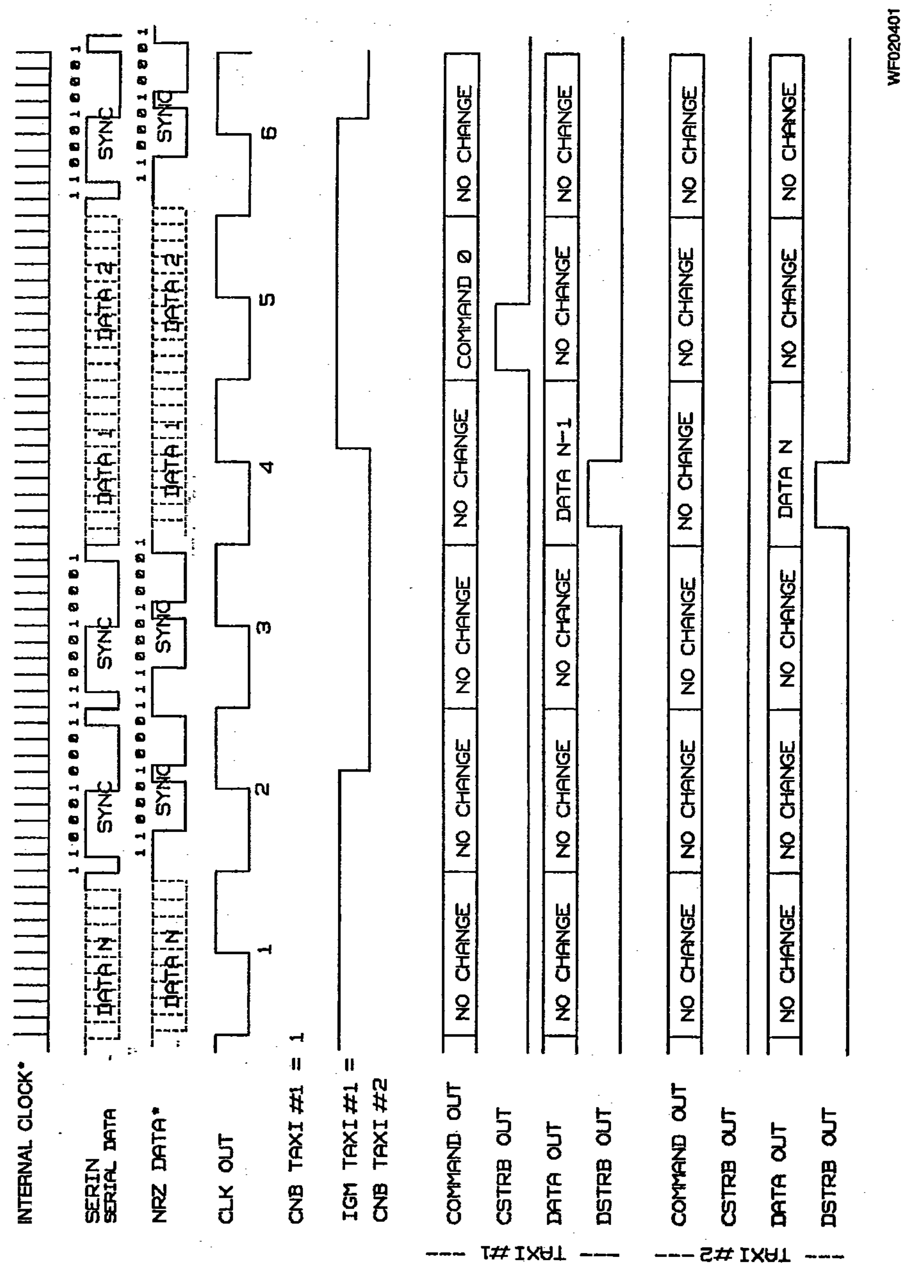



**TAXIchip Receiver Timing (8-Bit Local Mode)**

*Internal Signals

## SWITCHING WAVEFORMS (Cont'd.)

### TAXIchip Receiver

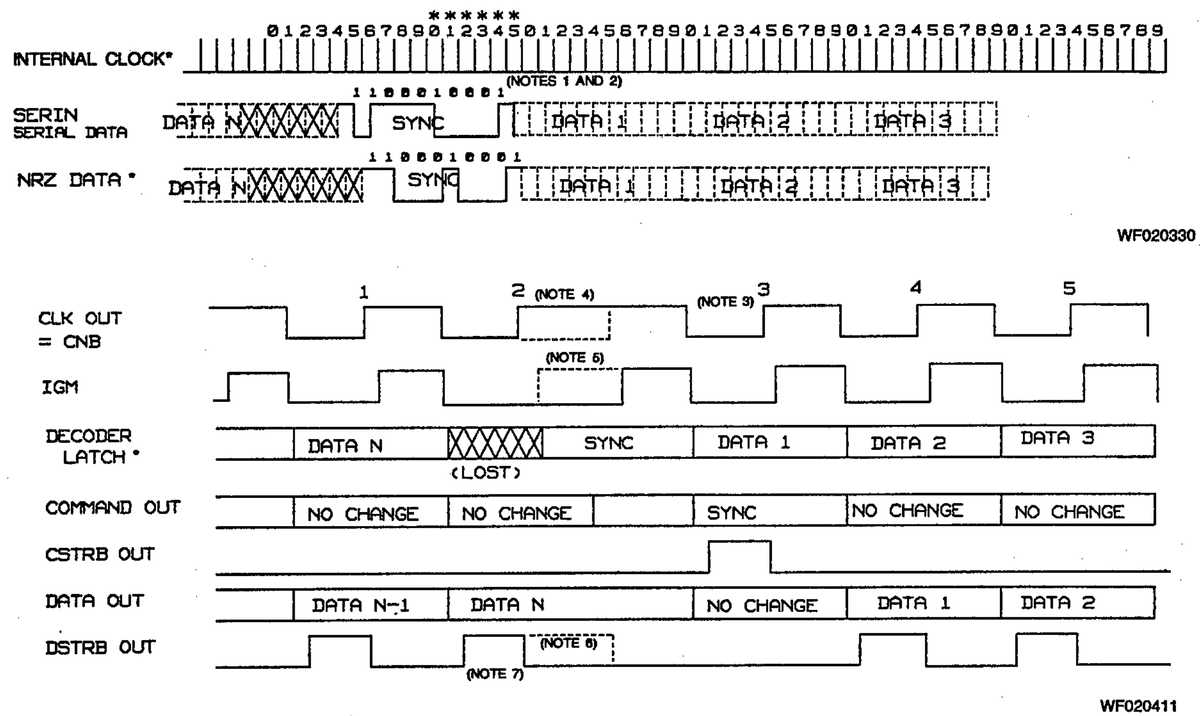



**TAXIchip Receiver Timing (8-Bit Cascade Mode)**

*Internal Signals

## SWITCHING WAVEFORMS (Cont'd.)

### TAXIchip Receiver




**Timing Showing External Effect of Sync Error (8-Bit Local Mode)**

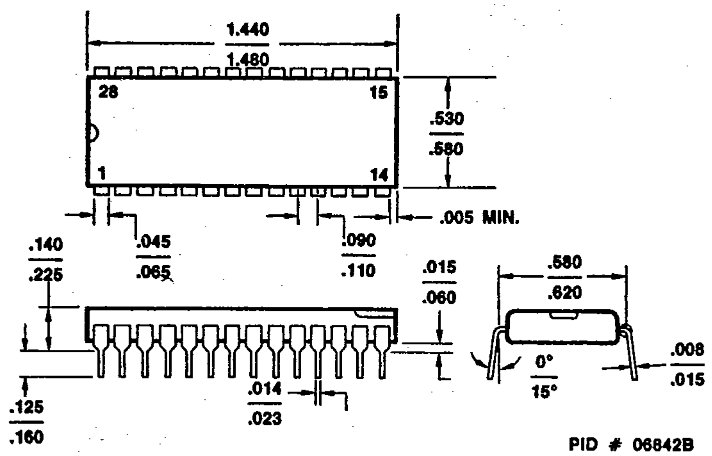
*Internal Signals

Notes:
1. Sync detected in Shifter, but not synchronized with internal state machine.
2. State machine re-synched to new sync position.
3. CLK output delayed to new position.
4. CLK LOW or HIGH time gets stretched depending on what states of the internal machine are skipped.
5. IGM rises at the 65th state of the state machine.
6. STRB falls at the rising edge of the CLK Out.
7. STRB may be shifted one bit time if the state machine is reset at state 1.

## PHYSICAL DIMENSIONS*

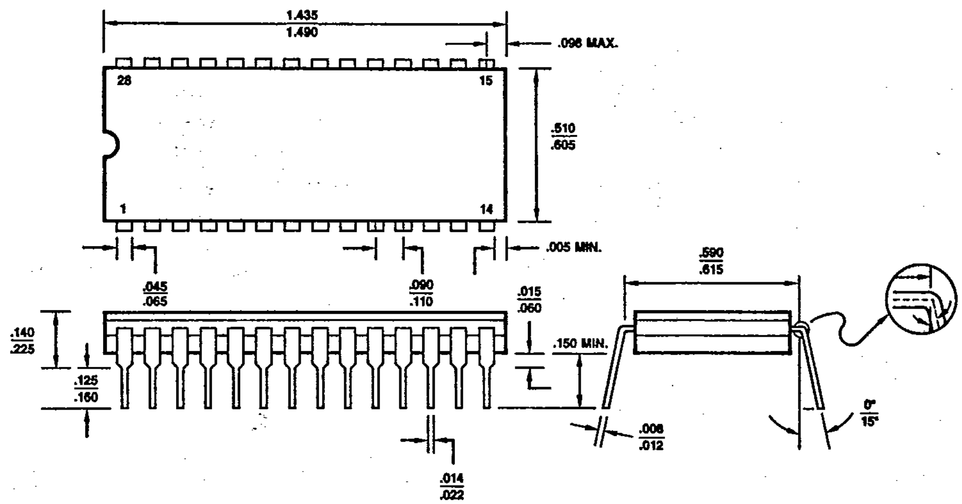
T-75-37-05

### PD 028




PID # 06842B

### CD 028



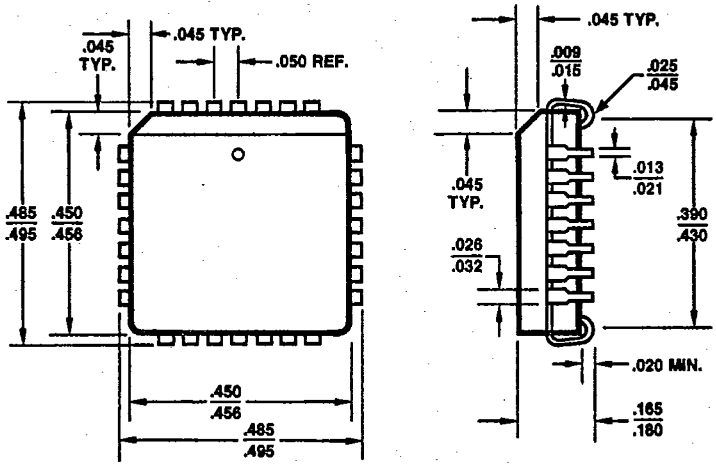

PID # 06837A

*For reference only.

## PHYSICAL DIMENSIONS (Cont'd.)

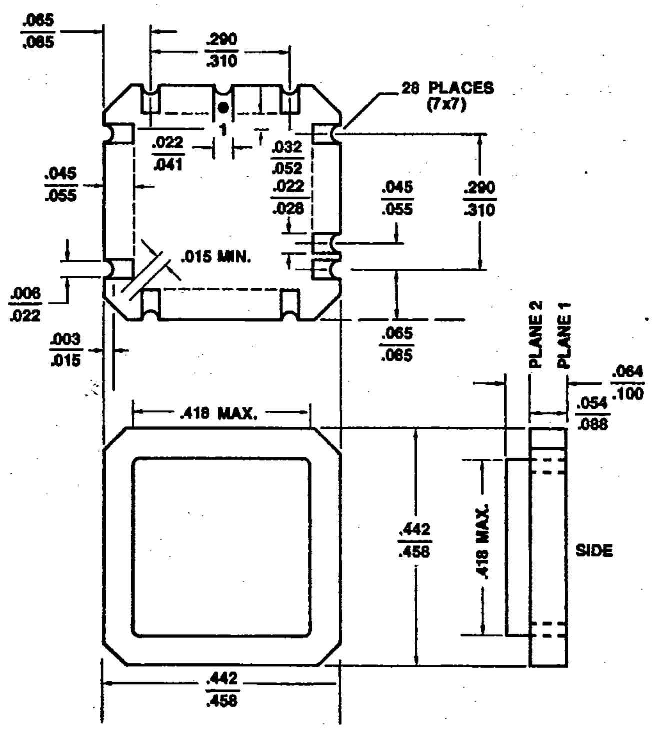
T-75-37-05

### PL 028




PID # 06751D

### CL 028

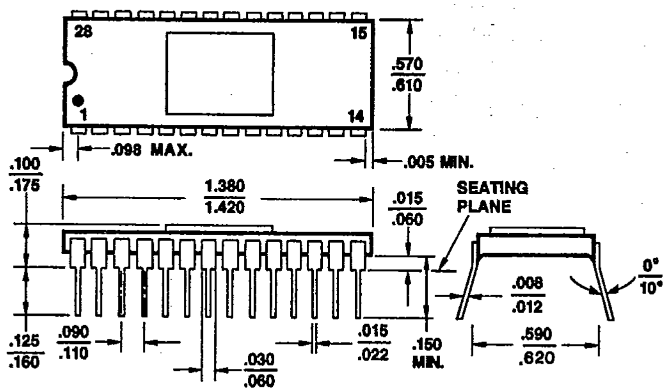



PID # 06595D

## PHYSICAL DIMENSIONS (Cont'd.)

T-75-37-05

### SD 028




PID # 07430B



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