CH9201
High Performance Graphics Clock Generator

FEATURES

- Low cost solution
- Synthesizes 32 programmable frequencies
- Frequency programmable from 5MHz to 80MHz
- Glitch free frequency transitions with strobe option
- TTL or CMOS compatible
- Provision for two external frequency inputs
- Advanced PLL design with low phase jitter
- Internal PLL remains locked while external inputs are selected
- Pin compatible with ICS 1394
- Requires fewer external components
- High performance, low power CMOS design
- Available in 20 pin plastic DIP or SO

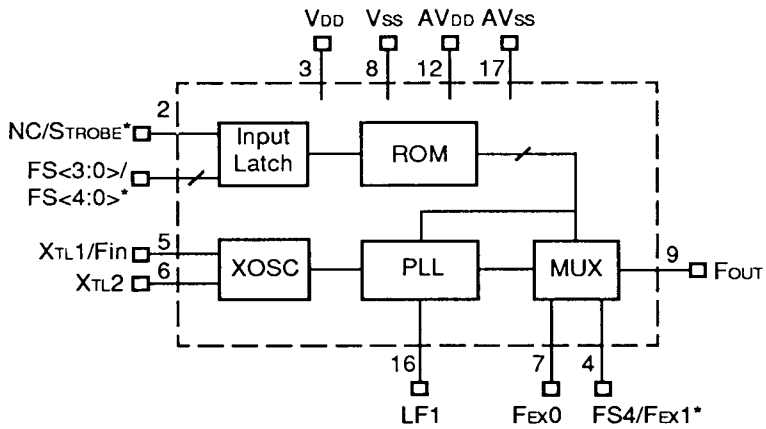
DESCRIPTION

The ***Chrontel*** CH9201 is a high performance frequency synthesizer designed specifically for use in high performance PC graphic systems and in applications where frequency programmability is desired. The output frequency can be programmed from a set of 32 frequencies by external strapping the Frequency Select pins to ground. ***Chrontel*** currently supports frequencies required by different graphics controllers and offers its customers the option to define the frequency set by mask programming the internal ROM. The CH9201 can support frequency requirements to 80MHz including graphic standards like MDA, CGA, VGA, EVGA and the 8514A.

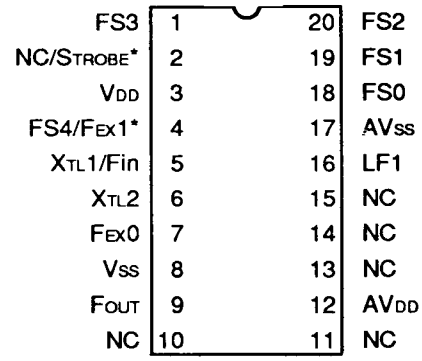
The CH9201 saves substantial system costs by eliminating multiple external clocks, reducing board space, eliminating external components and reducing inventory costs.

The CH9201 has the capability to multiplex two externally generated signal sources into the signal path. For multimedia applications, this feature allows the device to overlay text or graphics with an external VCR or frame grabber. Thus, real time images can be superimposed.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



* Refer to Customer Options

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to Ground	-0.5 to +7.0	V
T_B	Ambient Temperature under Bias	-55 to +125	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC CHARACTERISTICS (0 to + 70°C, V_{DD} = 5V ±10%)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN.	NOM.	MAX.	UNIT
V_{OH}	Output High Voltage	V_{DD}=4.5V, I_{OH}= -4.0mA	2.4			V
V_{OL}	Output Low Voltage	V_{DD}=4.5V, I_{OL}= 8.0 ma			0.4	V
V_{IH}	Input High Voltage		2.0			V
V_{IL}	Input Low Voltage				0.8	V
I_{LI}	Input Leakage	GND - V_{IN} -Vcc	-10		10	µA
I_{OH}	Output Source	V_{OH}= 2.4V			-4	mA
I_{OL}	Output Sink	V_{OL}= 0.4V			8	mA
I_{DD}	Operating Current	F_{OUT}= 20MHz		10		mA

AC CHARACTERISTICS (0 to +70°C, V_{DD}= 5V ±10%)

SYMBOL	DESCRIPTION	TEST CONDITIONS	MIN.	NOM.	MAX.	UNIT
F_{OS}	Crystal Frequency	Parallel Resonant (C_L=20pF)		14.318		MHz
F_{OUT}	Output Frequency		5		80	MHz
T_{OH}	Output Rise	C_{OUT}= 25pF, 0.4V-2.4V (TTL)			3	ns
T_{OL}	Output Fall	C_{OUT}= 25pF, 0.4V-2.4V (TTL)			3	ns
T_{DU}	Duty Cycle		40	50	60	%

OPERATION

The CH9201 is a low jitter frequency synthesizer designed for graphics applications. The reference frequency for the phase-locked loop (PLL) is generated by a Pierce oscillator which causes the crystal to oscillate at its parallel resonance and the equivalent on-chip shunt capacitance presented to the crystal is 20pF. If an external TTL or CMOS clock reference is available at 14.318MHz, the oscillator can be bypassed by removing the crystal, and connecting $X_{TL}1/F_{IN}$ to the external reference source directly; no coupling capacitor is required.

The output frequency of the PLL is controlled by the ROM which is addressed by the frequency select pins FS<4:0> directly; except when the Stobe Option is specified by customer (refer to Customer Options). ***Chrontel*** supports frequencies for the popular VGA controllers on the market and offers its customer the option to program the ROM with customized frequencies. The default frequency table is listed in the next page.

An output MUX controlled by the ROM, can multiplex an external frequency to F_{OUT}. Up to two external frequencies can be multiplexed if the "Second External Frequency Option" is specified. The PLL will remain in lock when the external frequency is chosen. By toggling between the external frequencies and the PLL output, images from different sources such as text and graphics can be overlay.

CUSTOMER OPTIONS

Under special arrangement with ***Chrontel***, the customer can specify the following options:

STROBE OPTION: Frequency Control pins FS<4:0> can be mask programmed to operate in strobe mode. In this mode, FS<4:0> are latched at the falling edge of STROBE. When STROBE is high, the phase detector of the PLL is disabled and the frequency dividers in the PLL are reset to zero count. The output frequency remains at the previous setting until a new FS<4:0> is strobed. When STROBE is returned low, the frequency dividers and the phase detector are enabled. If this option is not specified, FS<4:0> address the ROM directly.

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	FS3	Input	Frequency Select for Clock Output
2	NC	Input	No Connection
3	VDD		Digital Power Supply
4	FS4	Input	Frequency Select for Clock Output
5	XTL1/FIN	Input	External Crystal Input/External Reference Input
6	XTL2	Input	External Crystal Input
7	FEX0	Input	External Frequency Input
8	Vss		Digital Ground
9	FOUT	Output	Clock Output
10	NC		No Connection, connect to Ground
11	NC		No Connection, connect to Ground
12	AVDD		Analog Power Supply
13	NC		No Connection, connect to Ground
14	NC		No Connection, connect to Ground
15	NC		No Connection, connect to Ground
16	LF1	Input	External Loop Filter Capacitor
17	AVss		Analog Ground
18	FS0	Input	Frequency Select for Clock Output
19	FS1	Input	Frequency Select for Clock Output
20	FS2	Input	Frequency Select for Clock Output

* Refer to Customer Options

CH9201TS(1) OUTPUT FREQUENCIES

FS4	FS3	FS2	FS1	FS0	Freq (MHz)
0	0	0	0	0	14.318
0	0	0	0	1	16.257
0	0	0	1	0	Fex0
0	0	0	1	1	32.514
0	0	1	0	0	25.175
0	0	1	0	1	28.322
0	0	1	1	0	24.000
0	0	1	1	1	40.000
0	1	0	0	0	14.318
0	1	0	0	1	16.257
0	1	0	1	0	Fex0
0	1	0	1	1	36.000
0	1	1	0	0	25.175
0	1	1	0	1	28.322
0	1	1	1	0	24.000
0	1	1	1	1	40.000

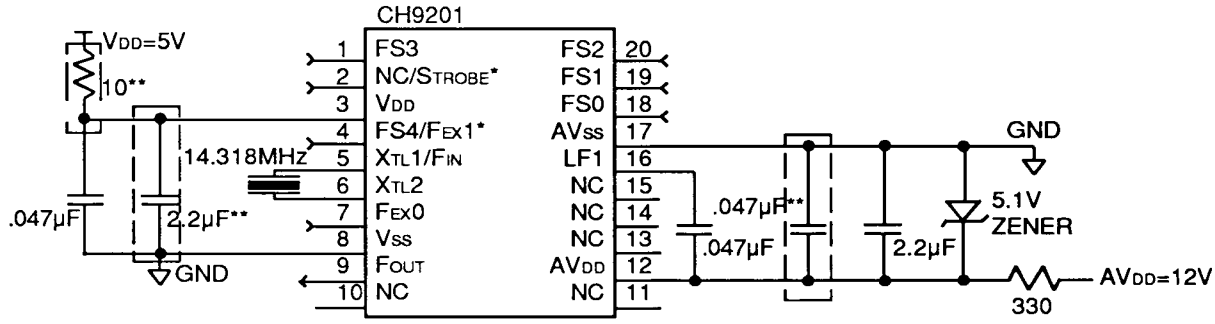
FS4	FS3	FS2	FS1	FS0	Freq (MHz)
1	0	0	0	0	25.175
1	0	0	0	1	28.322
1	0	0	1	0	32.514
1	0	0	1	1	36.100
1	0	1	0	0	40.000
1	0	1	0	1	44.900
1	0	1	1	0	50.350
1	0	1	1	1	65.000
1	1	0	0	0	50.350
1	1	0	0	1	56.644
1	1	0	1	0	63.028
1	1	0	1	1	72.200
1	1	1	0	0	80.000
1	1	1	0	1	89.800
1	1	1	1	0	100.70 (2)
1	1	1	1	1	130.00 (2)

Note: (1) For other frequency table please consult the factory
(2) TTL level output cannot be not guaranteed for frequencies higher than 90.0 MHz

SECOND EXTERNAL FREQUENCY OPTION: With this option a second external frequency input is made available by redefining the control pin FS4 (pin 4) as the second frequency input. The user can only address the first 16 frequencies in the ROM through FS<3:0>.

FREQUENCY OPTION: Customer can specify up to 32 (16 with second external frequency option) frequencies by using mask programming in the ROM. Although the frequency range of the CH9201 spans from 5MHz to 130MHz, output stage can maintain TTL levels only up to 90MHz. At frequencies above 90MHz, a ECL differential line receiver can be used to buffer output to ECL levels.

CIRCUIT CONFIGURATION



* Refer to Customer Options
** Optional external components

LAYOUT CONSIDERATIONS

The following layout rules should be followed for best phase noise performance:

1. Place all power supply bypass capacitors in close proximity to their respective power pins.
2. Use a ground plane to connect Vss, AVss and all external component grounds. Isolate this ground plane from other circuits by connecting it to ground at the card edge.
3. Use a low inductance trace to connect AVDD, loop filter capacitor, bypass capacitors for AVDD and the zener diode.
4. Place the loop filter capacitor and the reference crystal close to the device.
5. Do not run any signal line through the synthesizer section of the board.

ORDERING INFORMATION

Part Number	I/O	Package
CH9201Cx-NC	CMOS	300 mil DIP
CH9201Tx-NC	TTL	300 mil DIP
CH9201Cx-SC	CMOS	300 mil SO
CH9201Tx-SC	TTL	300 mil SO

Note: x = Alphanumeric version of the device

PACKAGE DIMENSIONS

Package outlines meet JEDEC Standards

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