CIRRUS LOGIC

FEATURES

■ AC '97 2.0 compliant

■ Quad 20-bit D/A converters and stereo 18-bit A/D converters with fixed 48 kHz sampling rate

■ Three analog line level stereo inputs from LINE IN, CD, and AUX

■ High quality pseudo-differential CD input

■ Dual stereo line level output with independent 6-bit volume control

■ 6 General Purpose I/O pins

■ Meets or exceeds Microsoft's ® PC 98 and PC 99 audio performance requirements

■ CrystalClear™ 3D Stereo Enhancement

ORDERING INFORMATION
    CS4294-KQ   48-pin TQFP   9x9x1mm
    CS4294-JQ   48-pin TQFP   9x9x1mm

SoundFusion™
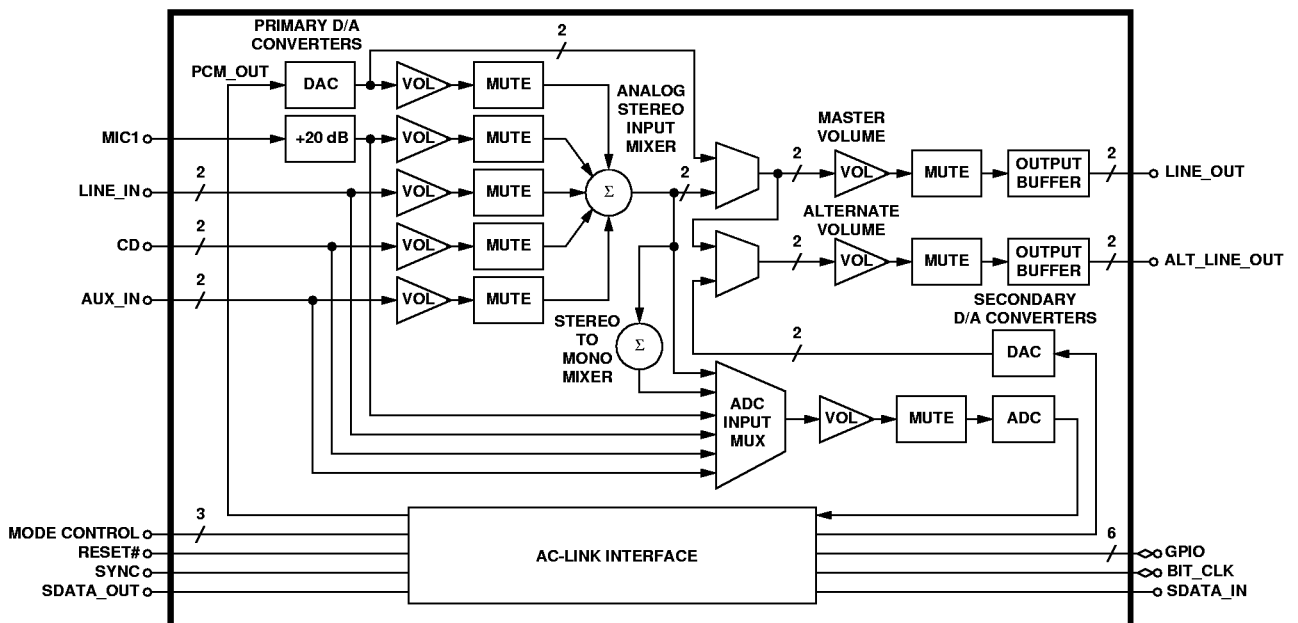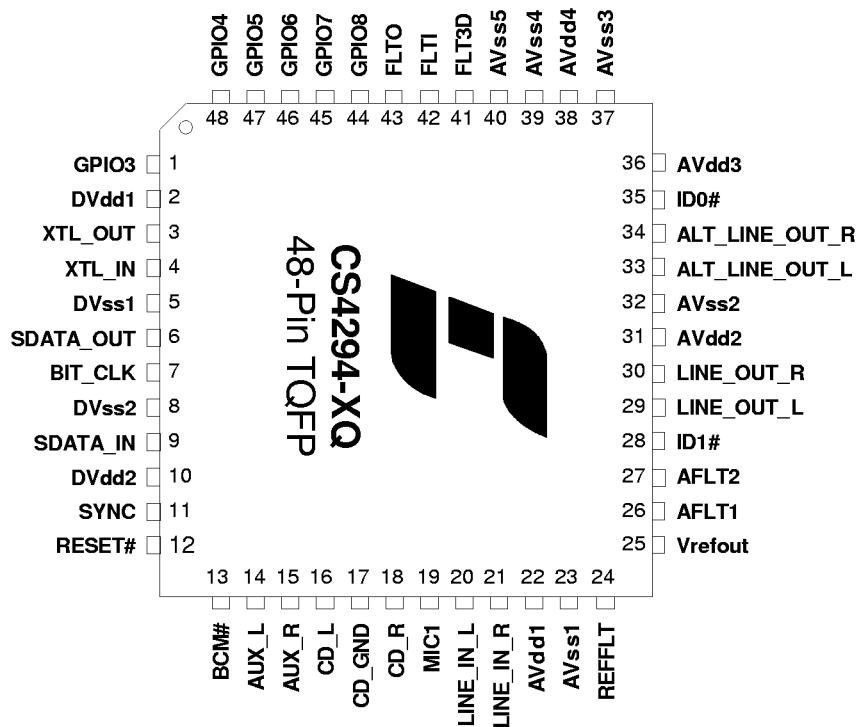*4-Channel Audio Codec '97*

DESCRIPTION

The CS4294 is an AC '97 compliant Audio Codec designed for PC multimedia systems. Using the industry leading CrystalClear delta-sigma and mixed signal technology, the CS4294 is ideal for PC 98-compliant desktop, notebook, and entertainment PCs, where high-quality audio features are required.

The CS4294 offers four channels of D/A and two-channel A/D conversion along with analog mixing and 3D processing. For multichannel audio systems, the CS4294 can provide four audio channels. The CS4294 can be used with other AC '97 codecs to provide six or eight audio channels.

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PIN DESCRIPTIONS

Digital I/O Pins

RESET# - AC '97 Chip Reset, Input

This active low signal is the asynchronous Cold Reset input to the CS4294. The CS4294 must be reset before it can enter normal operating mode. When the PR4 bit of register 26h is set, the rising edge of RESET# is interpreted as an AC '97 2.1 Warm Reset, preserving register values.

SYNC - AC-link Serial Port Sync pulse, Input

This signal is the serial port timing signal for the AC-link of the CS4294. Its period is the reciprocal of the sample rate of the CS4294, 48 kHz. This signal is generated by the AC '97 Controller and is synchronous to BIT_CLK. SYNC is also an asynchronous input when the CS4294 is in a PR4 powerdown state and is configured as a primary codec. A series terminating resistor of 47 Ω should be connected on this signal close to the device driving the signal.

BIT_CLK - AC-link Serial Port Master Clock, Input/Output

This input/output signal controls the master clock timing for the AC-link. In codec primary mode, this signal is an output 12.288 MHz clock signal which is divided down by two from the XTL_IN input clock pin. In codec secondary mode, this signal is an input which controls the AC-link serial interface. In BIT_CLK mode, this signal generates all internal clocking including the AC-link serial interface timing. A series terminating resistor of 47 Ω should be connected on this signal close to the CS4294 in primary mode or close to the BIT_CLK source if in secondary mode.

SDATA_OUT - AC-link Serial Data Input Stream to AC '97, Input

This input signal transmits the control information and digital audio output streams to be sent to the DACs. The data is clocked into the CS4294 on the falling edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal close to the device driving the input.

SDATA_IN - AC-link Serial Data Output Stream from AC '97, Output

This output signal transmits the status information and digital audio input streams from the ADCs. The data is clocked out of the CS4294 on the rising edge of BIT_CLK. A series terminating resistor of 47 Ω should be connected on this signal as close to the CS4294 as possible.

XTL_IN - Crystal Input

This pin accepts either a crystal, with the other pin attached to XTL_OUT, or an external CMOS clock. XTL_IN must have a crystal or clock source attached for proper operation except when operating in BIT_CLK mode. The crystal frequency must be 24.576 MHz and designed for fundamental mode, parallel resonance operation.

XTL_OUT - Crystal Output

This pin is used for a crystal placed between this pin and XLT_IN. If an external clock is used on XTL_IN or the codec is in BIT_CLK mode, this pin must be left floating with no traces or components connected to it.

ID1#, ID0# - Codec ID, Inputs

These pins select the codec ID and mode of operation for the CS4294. They are sampled after the rising edge of RESET# and not used after. These inputs use the analog supply bus for their value and as such they require an external 100 kΩ pull-up or pull-down resistor to the analog supply bus rail. The pins utilize inverted logic, so a value of '1:1' sets the codec to primary mode while any other combination sets the codec to secondary mode. In primary mode, the codec is always clocked from an external crystal or an external oscillator connected to the XTL_IN and/or XTL_OUT pins with BIT_CLK as an output. In secondary mode, the clocking mechanism is determined by the state of the BCM# pin with BIT_CLK always being an input.

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BCM# - BIT_CLK Mode, Input

This pin selects the secondary mode clocking mechanism. BCM# is sampled after the rising edge of RESET# and not used after. If this pin is externally pulled-down by a 100 kΩ resistor, BIT_CLK mode will be in effect. In this case all internal timing is derived from the BIT_CLK input and no connections should be made to the XTL_IN and XTL_OUT pins. If this pin is externally pulled-up by a 100 kΩ resistor, normal clock generation will occur through XTL_IN. In codec primary mode, BCM# must be pulled high for normal operation.

GPIO[8:3] - General Purpose Input/Output

These GPIO pins are used to control modem DAAs and other discrete digital functions. When a GPIO pin is configured as an input, it behaves as a Schmitt trigger input with 350 mV of hysteresis at 5 V and 220 mV of hysteresis at 3.3 V. When a GPIO pin in configured as an output, it may function as a normal CMOS output (4 mA drive) or as an open drain output. GPIO pins power up in the high impedance state (tri-state).

Analog I/O Pins

MIC1 - Analog Mono Source, Input

This analog input is a monophonic source to the analog output mixer. It is intended to be used as a desktop microphone connection to the audio subsystem. The maximum allowable input is 1 V_{RMS} (sinusoidal). If the 20 dB internal boost is enabled, the maximum allowable input is 100 mV_{RMS} (sinusoidal). This input is internally biased at the Vrefout voltage reference and requires AC coupling to external circuitry. If this input is not used, it should be AC coupled to analog ground.

LINE_IN_L and LINE_IN_R- Analog Line Source, Inputs

These inputs form a stereo input pair to the CS4294. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

AUX_IN_L and AUX_IN_R- Analog Line Source, Inputs

These inputs form a stereo input pair to the CS4294. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

CD_L and CD_R - Analog CD Source, Inputs

These inputs form a stereo input pair to the CS4294. It is intended to be used for the Red Book CD audio connection to the audio subsystem. The maximum allowable input is 1 V_{RMS} (sinusoidal). These inputs are internally biased at the Vrefout voltage reference. AC coupling to external circuitry is required. If these inputs are not used, they should both be connected to the Vrefout pin or both AC coupled, with separate AC coupling caps, to analog ground.

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CD_GND - Analog CD Common Source, Input

This analog input is used to remove common mode noise from Red Book CD audio signals. The impedance on the input signal path should be one half the impedance on the CD_L and CD_R input paths. This pin requires AC coupling to external circuitry. If this input is not used, it should be connected to the Vrefout pin or AC coupled to analog ground.

LINE_OUT_L and LINE_OUT_R - Analog Line Level Outputs

These signals are analog outputs from the primary stereo output mux. This allows either the output of the stereo input mixer, or the output of the primary D/A converters to be routed to these pins. The full scale output voltage for output is nominally 1 V_{RMS} and is internally biased at the Vrefout voltage reference. It is required to either AC couple these pins to external circuitry or DC couple them to a buffer op-amp biased at the Vrefout voltage. These pins need a 680 pF NPO capacitor attached to analog ground.

ALT_LINE_OUT_L and ALT_LINE_OUT_R - Analog Alternate Line Level Outputs

These signals are analog outputs from the secondary stereo output mux. This allows either the output of the primary stereo output mux or the output of the secondary D/A converters to be routed to these pins. The full scale output voltage for each output is nominally 1 V_{RMS} and is internally biased at the Vrefout voltage reference. It is required to either AC couple these pins to external circuitry or DC couple them to a buffer op-amp biased at the Vrefout voltage. These pins need a 680 pF NPO capacitor attached to analog ground.

Filter and Reference Pins

REFFLT - Internal Reference Voltage, Input

This is the voltage reference used internal to the part. A 0.1 μF and a 1 μF (must not be larger than 1 μF) capacitor with short, wide traces must be connected to this pin. No other connections should be made to this pin.

Vrefout - Voltage Reference, Output

All analog inputs and outputs are centered around Vrefout which is nominally 2.2 Volts. This pin may be used to level shift external circuitry, however any external loading should be buffered.

AFLT1 - Left Channel Antialiasing Filter Input

This pin needs a 1000 pF NPO capacitor attached to analog ground.

AFLT2 - Right Channel Antialiasing Filter Input

This pin needs a 1000 pF NPO capacitor attached to analog ground.

FLTI - 3D Filter Input

A 1000 pF capacitor must be attached between this pin and FLTO if the 3D function is used.

FLTO - 3D Filter Output

A 1000 pF capacitor must be attached between this pin and FLTI if the 3D function is used.

FLT3D - 3D Filter

A 0.01 µF capacitor must be attached from this pin to AGND if the 3D function is used.

Power Supplies

DVdd1, DVdd2 - Digital Supply Voltage

These pins provide the digital supply voltage for the AC-link section of the CS4294. These pins may be tied to +5 V digital or to +3.3 V digital. The CS4294 and digital controller's AC-link should share a common digital supply.

DVss1, DVss2 - Digital Ground

These pins are the digital ground connection for the AC-link section of the CS4294. These pins should be isolated from analog ground currents.

AVdd1, AVdd2, AVdd3, AVdd4 - Analog Supply Voltage

These pins provide the analog supply voltage for the analog and mixed signal sections of the CS4294. These pins must be tied to +5 V analog supply. It is strongly recommended that +5 V be generated from a voltage regulator to ensure proper supply currents and noise immunity from the rest of the system.

AVss1, AVss2, AVss3, AVss4, AVss5 - Analog Ground

These pins are the ground connection for the analog, mixed signal, and substrate sections of the CS4294. These pins should be isolated from digital ground currents.

PACKAGE DIMENSIONS

48L TQFP PACKAGE DRAWING
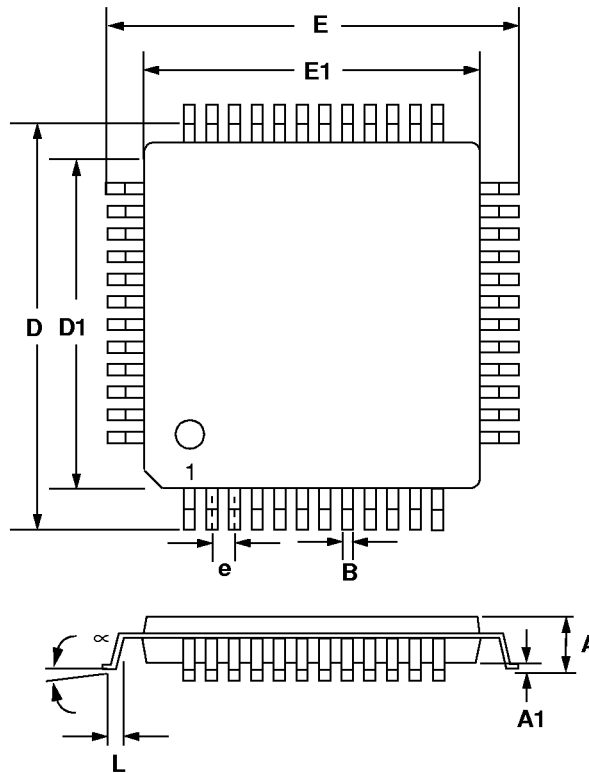
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.063	----	1.600
A1	0.002	0.006	0.050	0.150
B	0.007	0.011	0.170	0.270
D	0.343	0.366	8.700	9.300
D1	0.272	0.280	6.900	7.100
E	0.343	0.366	8.700	9.300
E1	0.272	0.280	6.900	7.100
e*	0.016	0.024	0.400	0.600
L	0.018	0.030	0.450	0.750
∝	0.000°	7.000°	0.000°	7.000°

* Nominal pin pitch is 0.50 mm

Controlling dimension is mm.
JEDEC Designation: MS026

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