Preliminary Product Brief
August 2000

microelectronics group

Lucent Technologies
Bell Labs Innovations

HW3100/HW2000 *Home Wire*™ Home Phoneline Networking Chip Set

Chip Set Features

- Turnkey solution for PCI adapter cards
- Support for the *HomePNA** Interface Specification 2.0:
  — Adaptive rate selection: 1 Mbit/s to 16 Mbits/s
- Compliant with *HomePNA* PHY Specification Revision 1.1:
  — Integrated 1 Mbit/s PHY on the HW3100
  — Automatically selects between *HomePNA* 1.1/2.0 modulation and protocol based on capabilities of partner station on the network
- Highly integrated home phoneline networking chip set with an *IEEE*† 802.3-compliant 10/100 Mbits/s media access controller (MAC):
  — HW3100 *HomePNA*/modem controller
  — HW2000 analog front end (AFE)
- Support for multimedia and real-time applications using priority-based queuing quality of service (QoS):
  — Implements eight levels of packet priority
- Compatible with existing services:
  — Voice
  — V.90 and emerging V.92 analog modems
  — G.Lite splitterless DSL (G.992.2)
  — Full-rate DSL (G.992.1)
  — ISDN
- Highly integrated HW2000 AFE:
  — Support for all *HomePNA* 2.0 front-end transmit and receive operations
  — Minimal additional components required
  — 10-bit ADC and DAC
  — Integrated crystal oscillator: 28 MHz fundamental mode crystal
  — On-chip filtering
- *IEEE* 802.3 (Ethernet)-compliant media access controller (MAC):
  — Address filtering: unicast, multicast, broadcast, and promiscuous mode
  — Tx and Rx packet status information
- Bus mastering architecture with integrated Tx and Rx direct memory access (DMA) controllers and buffer management for efficient CPU utilization
- Independent transmit and receive FIFOs with programmable thresholds
  — Buffer can accommodate 3.5 maximum size Ethernet packets
  — User-programmable Tx and Rx buffer sizes
- Low-power, 3.3 V, 0.20 µm technology

PCI Features

- Glueless peripheral component interconnect (PCI) interfaces:
  — 5.0 V and 3.3 V signaling
- Compliant with PCI Bus Specification, Revision 2.2

Power Management Features

- Compliant with the Network Device Class Power Management Specification, Revision 1.0a, as defined in the PC99 Hardware Design Guide
- Compliant with PCI Bus Power Management Interface Specification, Revision 1.1
- Supports the Advanced Configuration and Power Interface (ACPI) Specification, Revision 1.0

* *HomePNA* is an acronym for Home Phoneline Networking Alliance. It is a trademark of HomePNA, Inc.
† *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.

Chip Set Features (continued)

Modem Interface Features

- Provides line serial input/output (LSIO) interface for V.90/V92 host-controlled modem support:
  — Silicon DAA interface
- Compliant with the Device Class Specification as defined in the PC99 Hardware Design Guide:
  — Wake-on-ring support

Additional Chip Set Features

- Serial EEPROM interface
- LED support:
  — Link activity
  — Tx activity
  — Rx activity
  — Collision detect
  — Carrier sense
- *Microsoft Windows** 9x, *Windows* 2000, and *Windows NT** 5.0 driver support
- *IEEE* 1149.1 compliant JTAG test access port

Description

The Lucent Technologies Microelectronics Group's HW3100/HW2000 *Home Wire* home phoneline networking chip set is a fully integrated, turnkey solution designed to provide high-speed networking over existing residential telephone wiring.

The *Home Wire* chip set provides automatic rate adaptation, instantaneously adjusting to the changing electrical characteristics of the home phoneline communications channel, in order to select the optimal speed which can reach a maximum of 16 Mbits/s.

The two-device HW3100/HW2000 *Home Wire* chip set fully supports the *HomePNA* Interface Specification 2.0. The *HomePNA* was formed to develop specifications for interoperable, home-networked devices that use the already-in-place residential telephone wiring, regardless of the topology. The chip set is also fully compliant with the *HomePNA* PHY Specification Revision 1.1, in order to provide backwards compatibility with existing applications and home networks built around the *HomePNA* 1.1 technology.

In order to provide a robust, cost-effective, and simple-to-use home phoneline networking solution, the *Home Wire* chip set leverages the existing *IEEE* 802.3 MAC protocol and existing Plug and Play TCP/IP based networking software stacks used in the *Windows* 95, 98, and *Windows NT* operating systems. Up to 25 PCs, peripherals, or network devices can be installed on a single home phoneline network that can span up to 1000 feet between the two farthest points.

The HW3100/HW2000 *Home Wire* chip set is fully compatible with existing phone services such as voice, facsimile, V.90/V.92 modem connections, ISDN voice and data, and ADSL. Products based on the *Home Wire* chip set will not compromise or interrupt any of these services. Frequency division multiplexing (FDM) technology is used to simultaneously support existing and emerging telephone services along with networked *HomePNA* data traffic. The frequency ranges for *HomePNA* based products have been carefully selected to avoid interference from these various services that may be encountered in a typical home. As shown in Figure 1, signals from the *Home Wire* chip set are centered at 7 MHz, with the signal ranging from 4.25 MHz to 9.75 MHz. This frequency range is well above the frequencies used for existing phone services.

* *Microsoft, Windows,* and *Windows NT* are registered trademarks of Microsoft Corporation.

Description (continued)

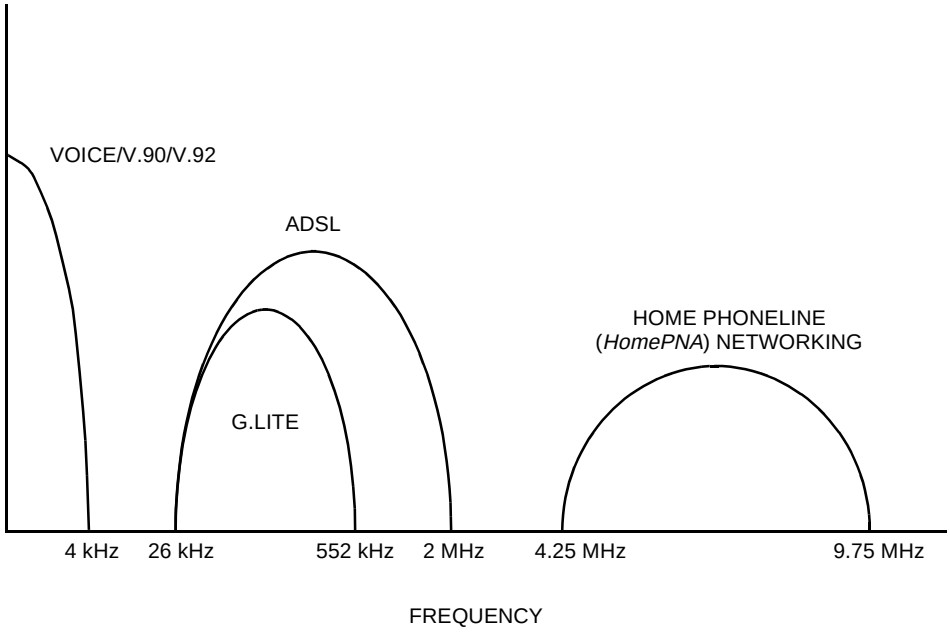

Figure 1*. Home Wire* Chip Set Compatibility with Existing Services

The *Home Wire* chip set unleashes the power of networking in the home by enabling a host of applications, allowing users to maximize their investment in peripheral devices, and take full advantage of existing narrowband or future broadband connections. The *Home Wire* chip set supports multimedia and real-time applications using priority-based queuing to ensure quality of service (QoS), enabling such applications as voice and video over IP in the home. The *Home Wire* chip set provides the core technology for the following:

- Internet connection sharing
- Peripheral sharing (i.e., printers, scanners, etc.)
- File and application sharing
- Entertainment (i.e., multiplayer gaming)
- Home automation
- IP telephony
- Video over IP
- PC-to-PC intercom
- Residential gateways

The HW3100/HW2000 *Home Wire* chip set also has provisions to support either a line codec or silicon DAA enabling the use of V.90/V.92 host-controlled modem technology.

V.90/V.92 host-controlled modem technology has been enabled by the availability of ample processing power in today's PCs. V.90/V.92 host-controlled modem technology eliminates the need for a dedicated digital signal processor to perform the specialized telephone line signal processing functions; the host processor assumes this function.

With the *Home Wire* chip set, V.90/V.92 modem functionality can be easily added to the design, eliminating the need for a separate PCI-based modem. A precious PCI slot is also freed up and the overall system cost is significantly reduced. In addition, the use of a silicon DAA with the *Home Wire* chip set reduces the overall cost, since a significant number of discrete components can be eliminated.

The *Home Wire* chip set is also compliant with the PC99 specification and the PCI Bus Power Management Interface Specification.

Functional Description

The HW3100/HW2000 *Home Wire* chip set consists of the Lucent HW3100 *HomePNA*/modem controller and the HW2000 analog front end (AFE). The HW3100 integrates the following functional blocks: an *IEEE* 802.3 media access controller (MAC), a *HomePNA* 1.1 PHY, a PCI interface, independent transmit and receive FIFOs, separate Tx and Rx bus mastering DMA controllers, a serial EEPROM interface, and a line serial I/O (LSIO) interface for V.90/V.92 host-controlled modem applications. The HW2000 provides the line interface, on-chip Tx and Rx filtering, an analog-to-digital converter (ADC), and a digital-to-analog converter (DAC).

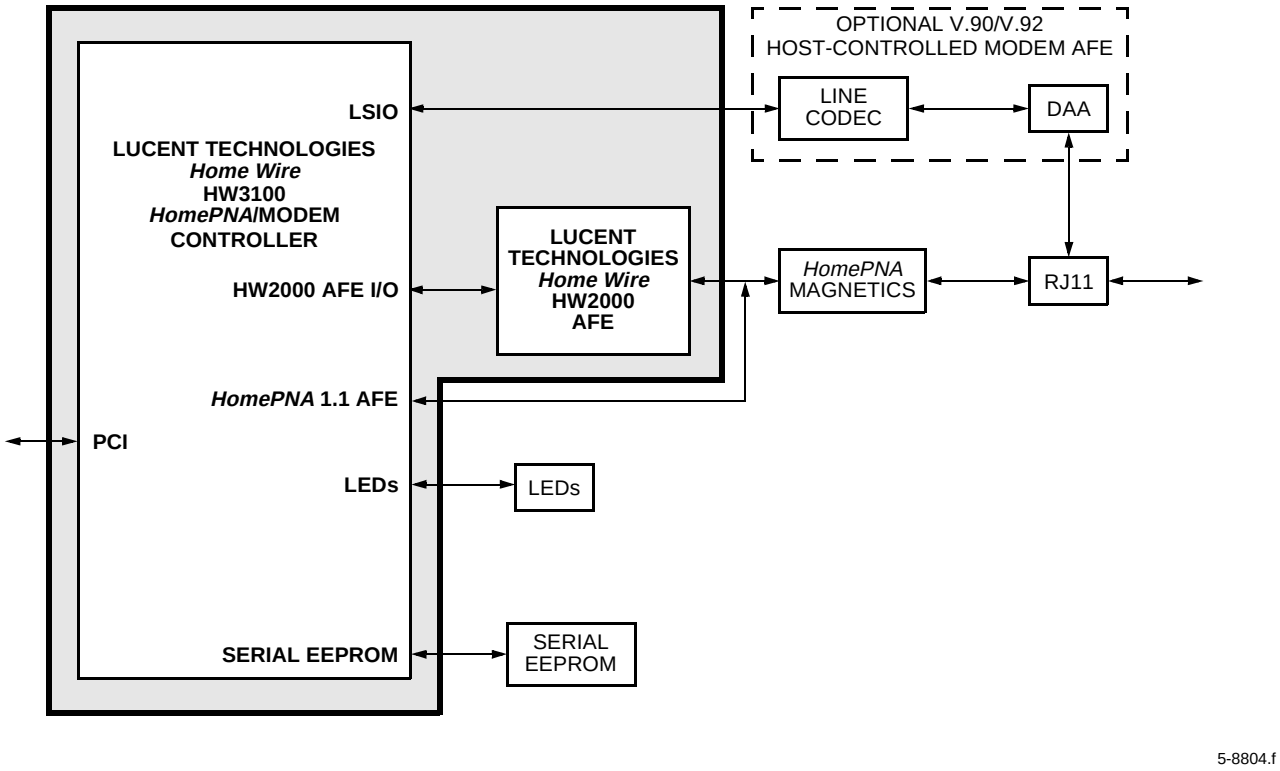

Figure 2. *Home Wire* Chip Set PCI with V.90/V.92 Host-Controlled Modem System Block Diagram

Figure 2 is a block diagram of a PCI-based *Home Wire* solution that provides *HomePNA* 2.0 functionality and a V.90/V.92 host-controlled modem.

Interactions between the host system and the *Home Wire* chip set occur in two modes: programmed I/O (PIO) and bus master modes. In the PIO mode, the host can read and write to the HW3130's control and status registers using either direct or memory mapped I/O transactions. When operating as a bus master, the HW3130 performs DMA transactions, automatically transferring packet data between its internal FIFOs and the host memory using efficient burst transactions.

Functional Description (continued)

PCI

The HW3100 PCI interface is fully compliant with PCI Local Bus Specification Revision 2.2 and the PCI Power Management Interface Specification. PCI subsystem ID, subvendor ID, and vendor ID are automatically read from the serial EEPROM. The PCI bus supports a 32-bit interface with an operating clock rate between dc and 33 MHz.

HW2000 AFE Interface

The HW3100 supports a 17-pin interface to the HW2000 AFE. The interface consists of a two-phase, multiplexed data converter interface with control logic used to control the positioning of the MSB of the data as well as the internal gain or attenuation of the HW2000 receiver and transmitter paths.

Serial EEPROM Interface

The HW3100 supports a 4-pin serial interface to external EEPROM. The minimum serial EEPROM size is 512 bytes.

Integrated *HomePNA* 1.1 PHY

In order to provide backwards compatibility with existing applications and home phoneline networks based on *HomePNA* 1.1 technology, the HW3100 supports an on-chip *HomePNA* 1.1 PHY.

The HW3100 supports a 4-pin 1M8 interface from the integrated PHY port to the external resistive hybrid.

Media Access Controller (MAC)

The HW3100 supports an *IEEE* 802.3-compliant media access controller. The MAC offloads the host CPU and manages packet transmission, packet reception, and destination address filtering.

JTAG Interface

The HW3100 supports an *IEEE* 1149.1 compliant JTAG boundary-scan test access port interface.

LSIO Interface

The HW3100 chip set supports direct connection to either a line codec or the *Silicon Labs** line codec/universal DAA.

HW2000 Overview

The HW2000 is the analog front-end for the *Home Wire* chip set and provides the Home PNA 2.0 line interface functionality. The HW2000 is composed of the following functional blocks:

- Integrated crystal oscillator
- 10-bit ADC and DAC
- Variable gain amplifiers
- Line drivers
- Filtering

Only minimal additional components (i.e., resistive hybrid, magnetics) are required to implement the *HomePNA* 2.0 line interface functionality.

Home Wire Chip Set: Support Tools

The primary HW3100/HW2000 *Home Wire* chip set evaluation tool is the HW3100/HW2000 *Home Wire* chip set PCI Reference Design. The *Home Wire* PCI Reference Design, bundled with drivers and installation software, will allow quick evaluation of the *Home Wire* chip set and support evaluation of interoperability.

* *Silicon Labs* is a registered trademark of Silicon Laboratories, Inc.

Home Wire Chip Set Product Family Overview

Table 1. Product Feature Matrix

Feature	HW3130	HW3100	HW3000S	HW3000M
PCI Interface, Revision 2.2	✓	✓	—	—
Host-Controlled Modem Interface	✓	✓	—	—
Microprocessor-Slave Interface	—	—	✓	—
MII	✓	—	—	✓
Serial EEPROM Interface	✓	✓	✓	—
LED Interface	✓	✓	✓	✓
Integrated *HomePNA* Revision 1.1 PHY	✓	✓	✓	✓
HW2000 *HomePNA* 2.0 AFE Interface	✓	✓	✓	✓
Device Package	160-pin MQFP	144-pin TQFP	100-pin TQFP	100-pin TQFP

Key:
✓: Supported.
— : Not supported.

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