



# STK22N6F3

N-channel 60 V, 0.0055  $\Omega$ , 22 A, PolarPAK<sup>®</sup>  
STripFET<sup>™</sup> Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max
STK22N6F3	60 V	< 0.006 $\Omega$

- Ultra low top and bottom junction to case thermal resistance
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- Fully encapsulated die
- 100% matte tin finish (in compliance with the 2002/95/EC european directive)
- High avalanche ruggedness
- PolarPAK<sup>®</sup> is a trademark of VISHAY

## Application

- Switching applications

## Description

This STripFET<sup>™</sup> III Power MOSFET technology is among the latest improvements, which have been especially tailored to minimize on-state resistance providing superior switching performances.

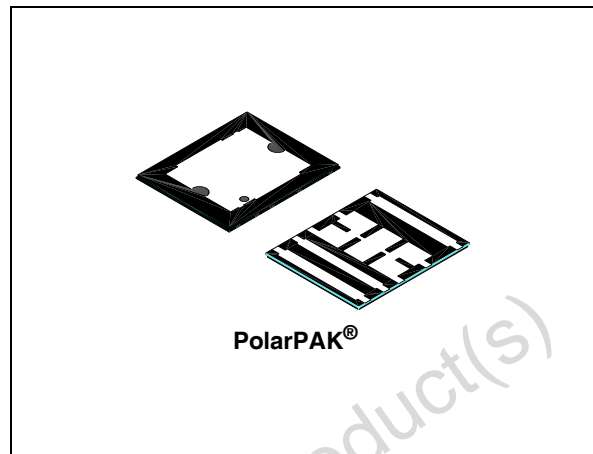


Figure 1. Internal schematic diagram

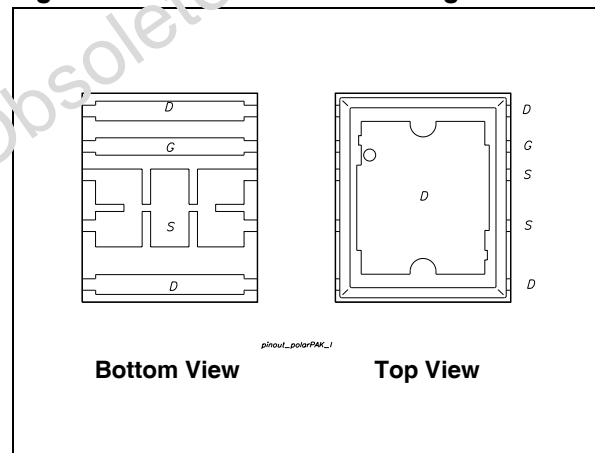


Table 1. Device summary

Order code	Marking	Package	Packaging
STK22N6F3	2263	PolarPAK <sup>®</sup>	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	22	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	13.7	A
$I_{DM}^{(2)}$	Drain current (pulsed)	88	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25^\circ\text{C}$	5.2	W
	Derating factor	0.0416	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single pulse avalanche energy	800	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 150	$^\circ\text{C}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2 oz Cu and  $\leq 10$  sec
2. Pulse width limited by package
3. Starting  $T_J = 25^\circ\text{C}$ ,  $I_D = 11$  A,  $V_{DD} = 48$  V

**Table 3. Thermal data**

Symbol	Parameter	Typ.	Max.	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	20	24	$^\circ\text{C}/\text{W}$
$R_{thj-c}^{(2)}$	Thermal resistance junction-case (top drain)	0.8	1	$^\circ\text{C}/\text{W}$
$R_{thj-c}^{(3)}$	Thermal resistance junction-case (source)	2.2	2.7	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2 oz Cu and  $\leq 10$ sec
2. Steady state
3. Measured at source pin when the device is mounted on FR-4 board in steady state

## 2 Electrical characteristics

( $T_{CASE}=25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	60	-	-	V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating}$ , $T_c = 125\text{ }^{\circ}\text{C}$	-	-	10 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$	-	-	$\pm 200$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	-	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 11\text{ A}$	-	0.0055	0.006	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	2500	-	pF
$C_{oss}$	Output capacitance			536		pF
$C_{rss}$	Reverse transfer capacitance			44		pF
$Q_g$	Total gate charge	$V_{DD} = 48\text{ V}$ , $I_D = 22\text{ A}$	-	41	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{ V}$		12		nC
$Q_{gd}$	Gate-drain charge	<a href="#">Figure 14</a>		10		nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 Test signal level = 20 mV open drain	-	0.9	-	$\Omega$

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 11\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ <a href="#">Figure 13</a>	-	16	-	ns
$t_r$	Rise time			14		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 30\text{ V}$ , $I_D = 11\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ <a href="#">Figure 13</a>	-	28	-	ns
$t_f$	Fall time			5		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-	-	22 88	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 22 \text{ A}$ , $V_{GS} = 0$	-	-	1.2	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 22 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 30 \text{ V}$ , $T_j = 150^\circ\text{C}$ <i>Figure 18</i>	-	49 91 3.7	-	ns nC A

1. Pulse width limited by package
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

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## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

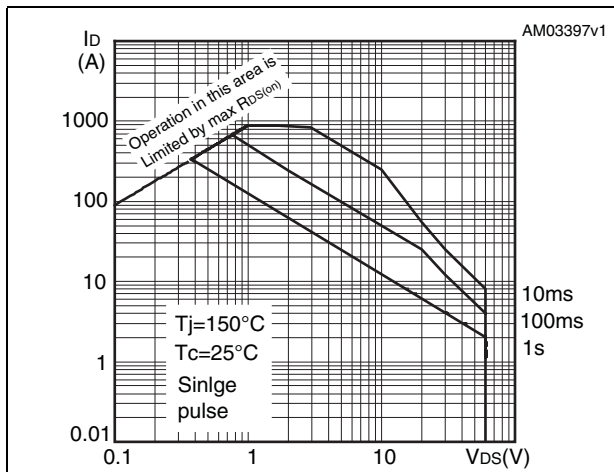


Figure 3. Thermal impedance

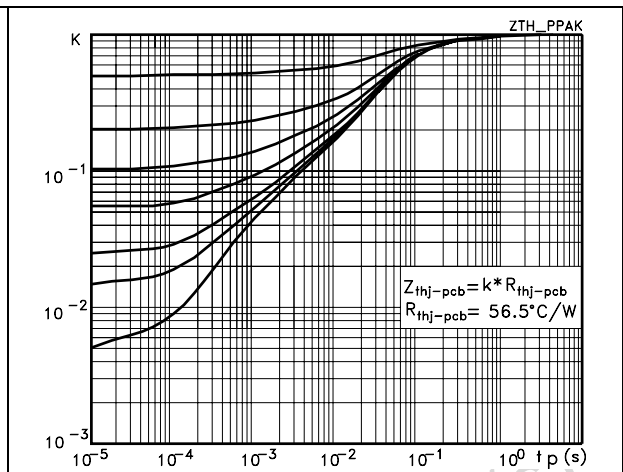


Figure 4. Output characteristics

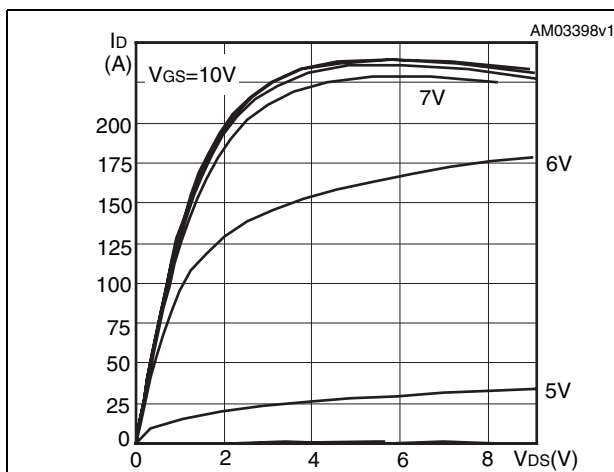


Figure 5. Transfer characteristics

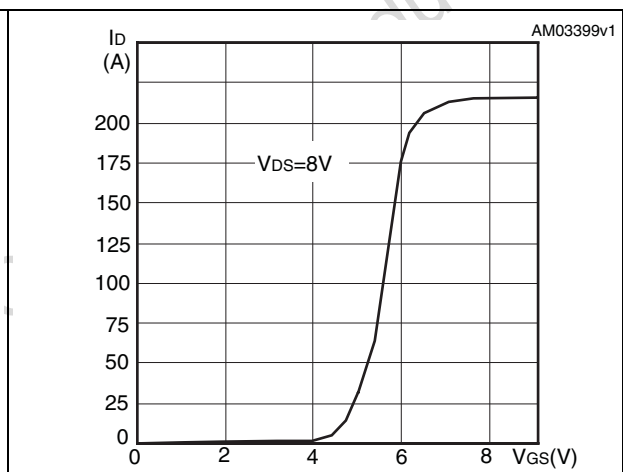


Figure 6. Normalized  $BV_{DSS}$  vs temperature

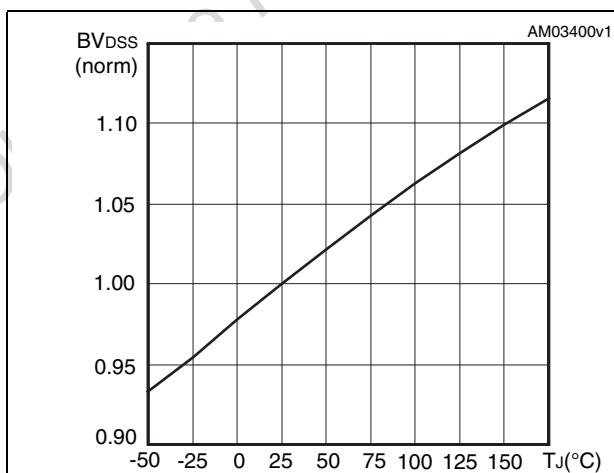


Figure 7. Static drain-source on resistance

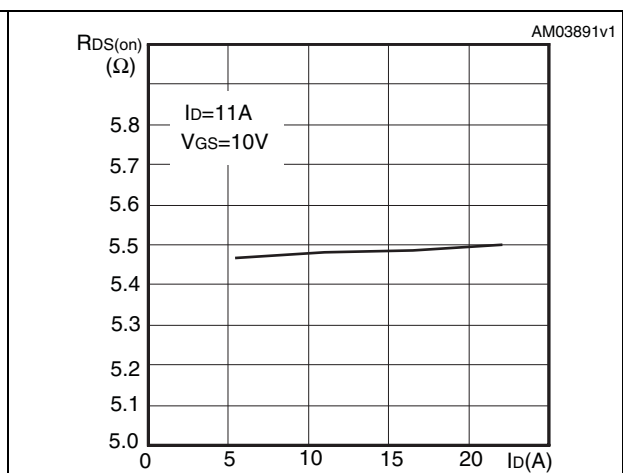


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

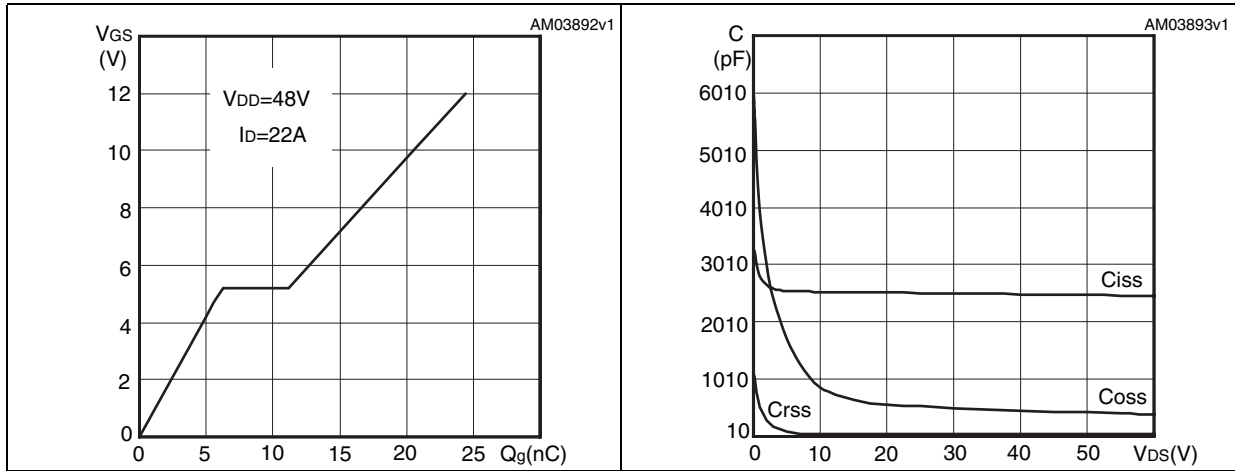


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

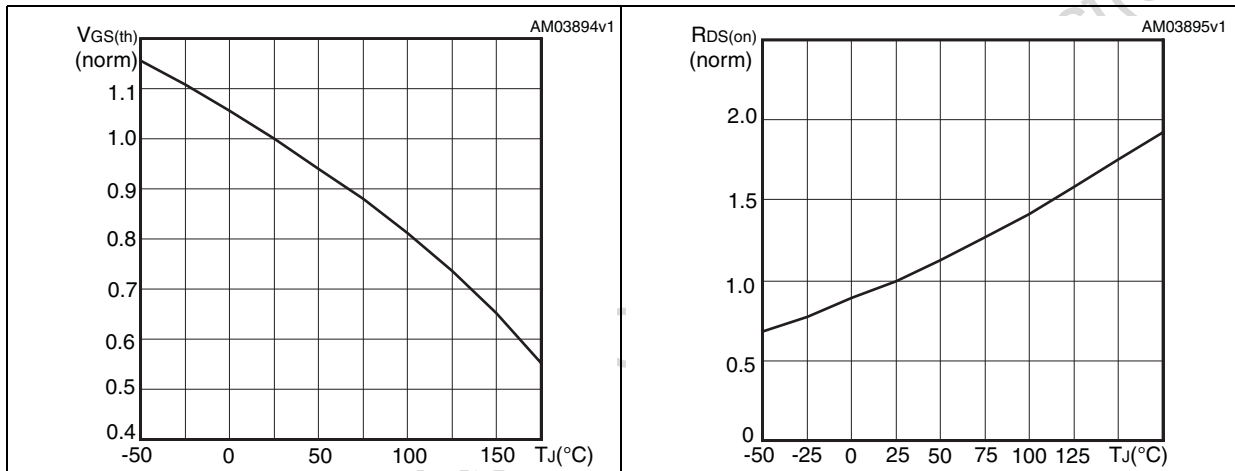
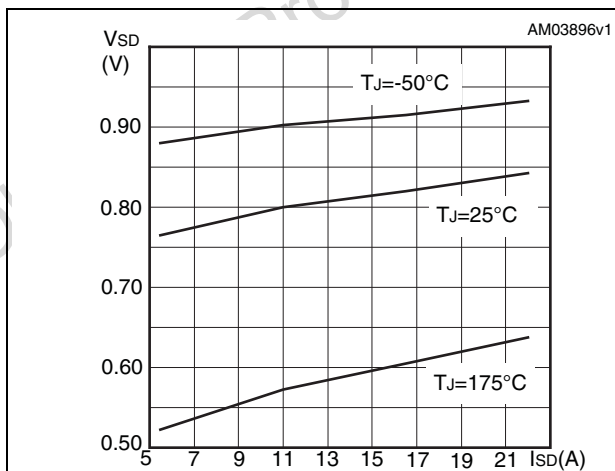
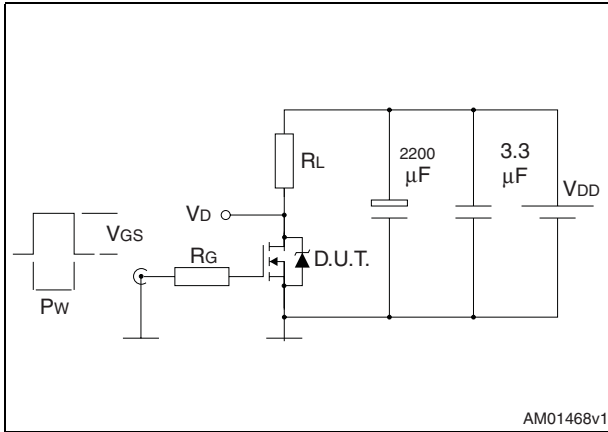


Figure 12. Source-drain diode forward characteristics



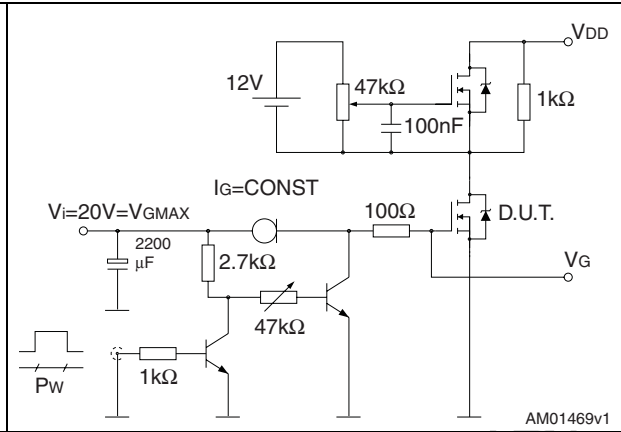
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



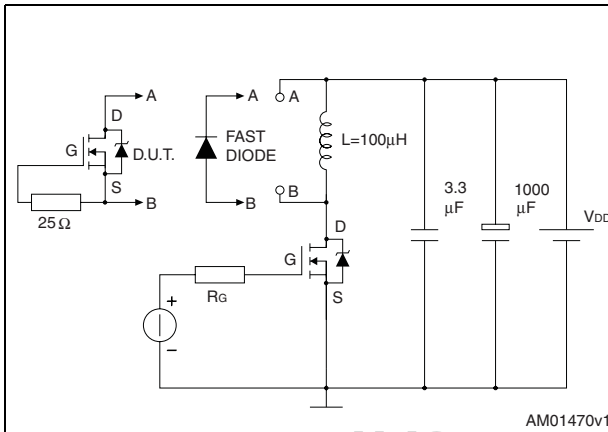
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**Figure 14. Gate charge test circuit**



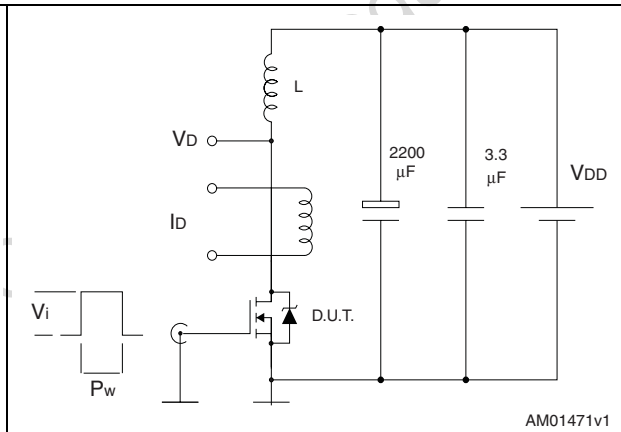
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



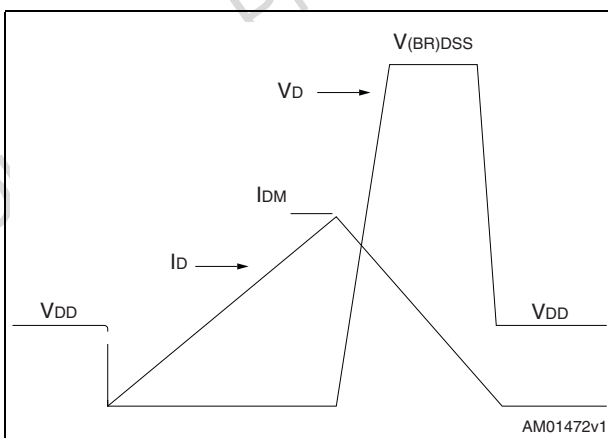
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**Figure 16. Unclamped inductive load test circuit**



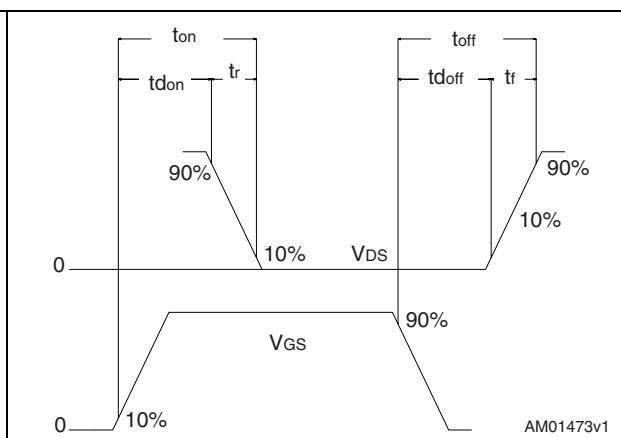
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**Figure 17. Unclamped inductive waveform**



AM01472v1

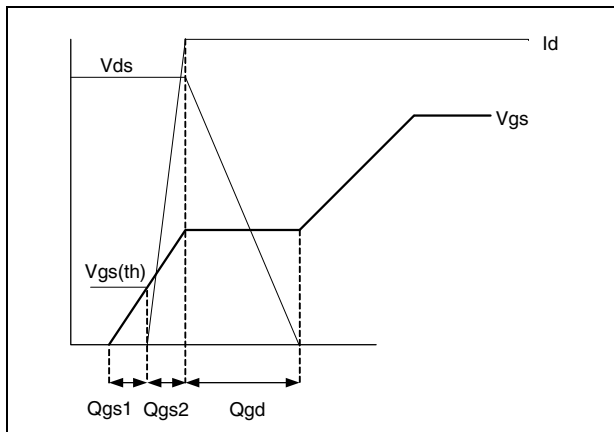
**Figure 18. Switching time waveform**



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Figure 19. Gate charge waveform



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## 4 Package mechanical data

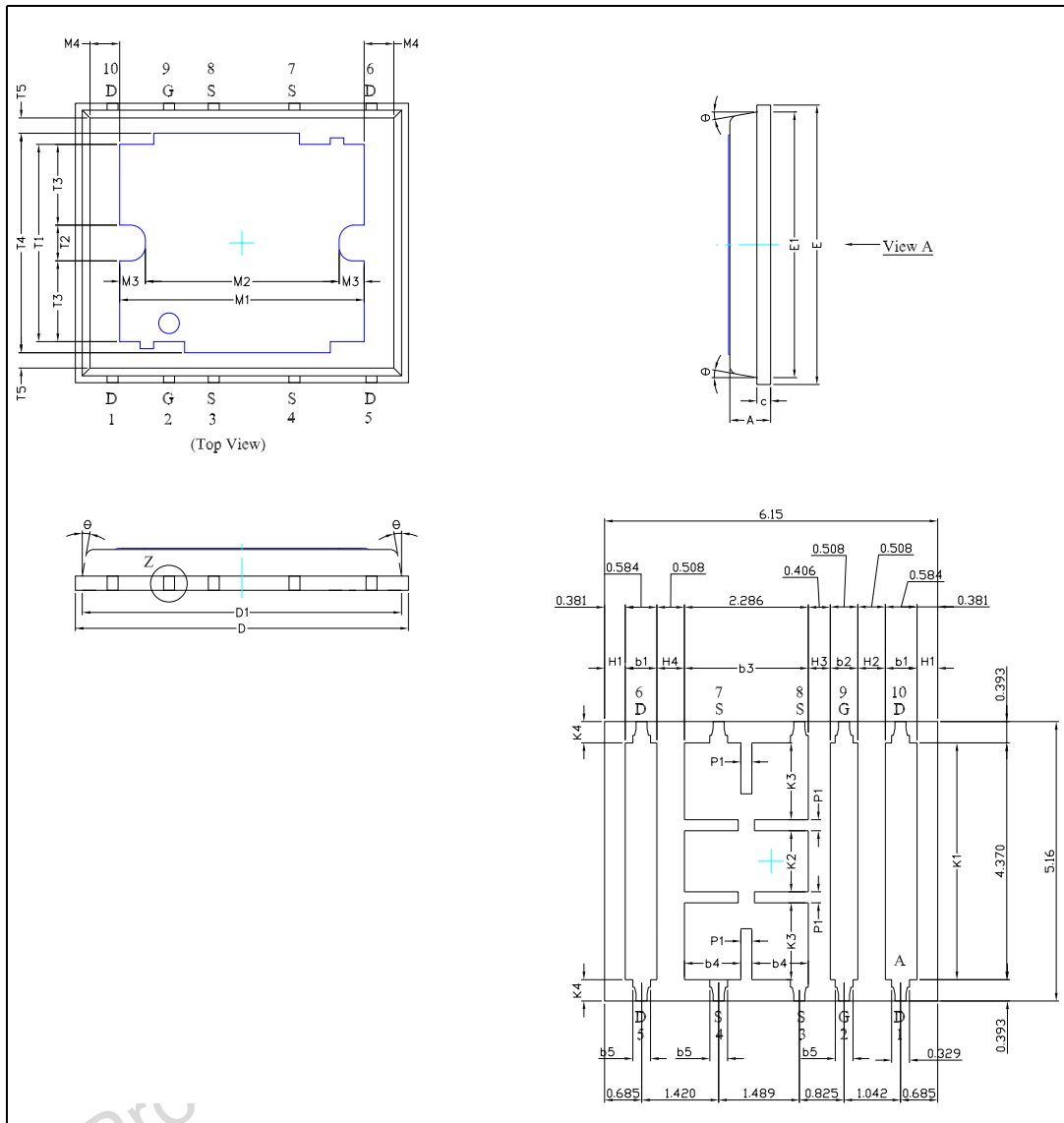
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Table 8. PolarPAK® (option "L") mechanical data

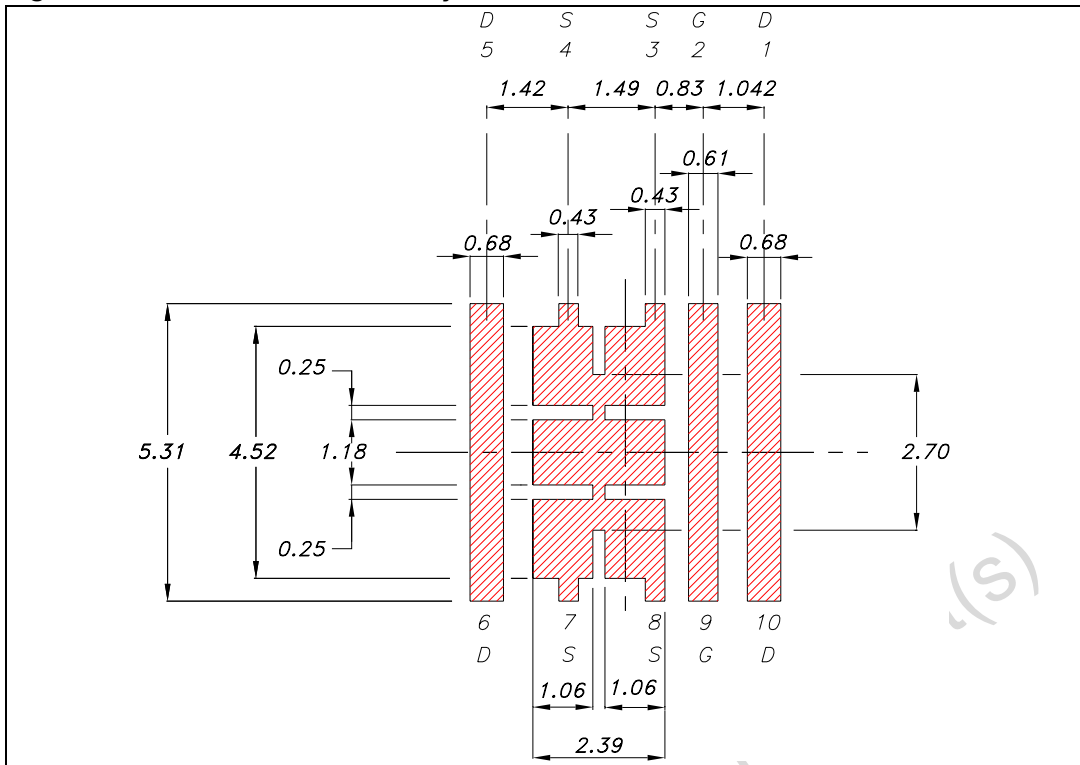
Ref.	mm			inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.75	0.80	0.85	0.030	0.031	0.033
A1			0.05			0.002
b1	0.48	0.58	0.68	0.019	0.023	0.027
b2	0.41	0.51	0.61	0.016	0.020	0.024
b3	2.19	2.29	2.39	0.086	0.090	0.094
b4	0.89	1.04	1.19	0.035	0.041	0.047
b5	0.23	0.33	0.43	0.009	0.013	0.017
c	0.20	0.25	0.30	0.008	0.010	0.012
D	6	6.15	6.30	0.236	0.242	0.248
D1	5.74	5.89	6.04	0.226	0.232	0.238
E	5.01	5.16	5.31	0.197	0.203	0.209
E1	4.75	4.90	5.05	0.187	0.193	0.199
H1	0.23			0.009		
H2	0.45		0.56	0.018		0.022
H3	0.31	0.41	0.51	0.012	0.016	0.020
H4	0.45		0.56	0.018		0.022
K1	4.22	4.37	4.52	0.166	0.172	0.178
K2	1.08	1.13	1.18	0.043	0.044	0.046
K3	1.37			0.054		
K4	0.24			0.009		
M1	4.30	4.50	4.70	0.169	0.177	0.185
M2	3.43	3.58	3.73	0.135	0.141	0.147
M3	0.22			0.009		
M4	0.05			0.002		
P1	0.15	0.20	0.25	0.006	0.008	0.010
T1	3.48	3.64	4.10	0.137	0.143	0.161
T2	0.56	0.76	0.95	0.022	0.030	0.037
T3	1.20			0.047		
T4	3.90			0.154		
T5		0.18	0.36		0.007	0.014
<	0°	10°	12°	0°	10°	12°

Figure 20. PolarPAK® (option “L”) drawings



Obsolete Proc

Figure 21. Recommended PAD layout



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## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
01-Jul-2008	1	First release
16-Apr-2009	2	Document status promoted from preliminary data to datasheet

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