National Semiconductor

54F/74F657 Octal Bidirectional Transceiver with 8-Bit Parity Generator/Checker and TRI-STATE® Outputs

General Description

The 'F657 contains eight non-inverting buffers with TRI-STATE® outputs and an 8-bit parity generator/checker. It is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24 mA (20 mA mil) at the A port and 64 mA (48 mA mil) at the B port.

Features

- 300 Mil 24-pin slimline DIP
- Combines 'F245 and 'F280A functions in one package
- TRI-STATE outputs
- B Outputs sink 64 mA (48 mA mil)
- 12 mA source current, B side
- Input diodes for termination effects

Ordering Code: See Section 11

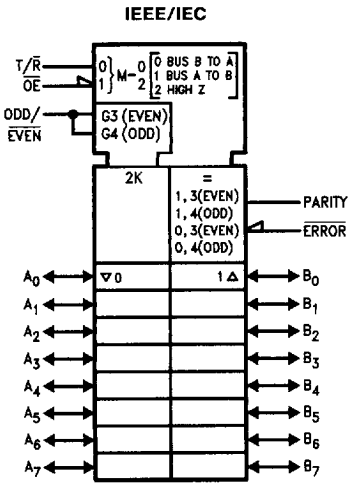
Commercial	Military	Package Number	Package Description
74F657SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F657SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
75F657SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F657FM (Note 2)	W24C	24-Lead Cerpack
	54F657LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

IEEE/IEC



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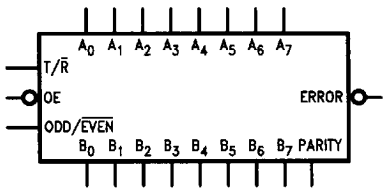

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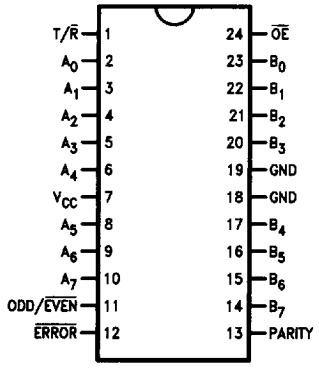
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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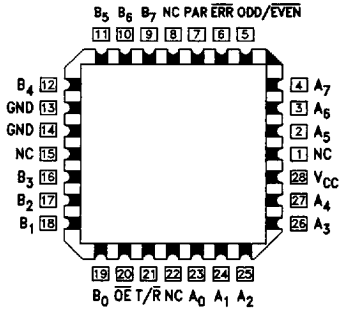
Pin Assignment for LCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_7	Data Inputs/	4.5/0.15	90 μA/ − 90 μA
	TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)
B_0–B_7	Data Inputs/	3.5/0.117	70 μA/ −70 μA
	TRI-STATE Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)
T/R	Transmit/Receive Input	2.0/0.067	40 μA/ −40 μA
OE	Enable Input	2.0/0.067	40 μA/ −40 μA
PARITY	Parity Input/	3.5/0.117	70 μA/ −70μA
	TRI-STATE Output	600/106.6 (80)	−12 mA/64 mA (48 mA)
ODD/EVEN	ODD/EVEN Parity Input	1.0/0.033	20 μA/ −20 μA
ERROR	Error Output	600/106.6 (80)	−12 mA/64 mA (48 mA)

Functional Description

The Transmit/Receive (T/R) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from the A port to the B port; Receive (active LOW) enables data from the B port to the A port.

The Output Enable (OE) input disables the parity and ERROR outputs and both the A and B ports by placing them in a HIGH-Z condition when the Output Enable input is HIGH.

When transmitting (T/R HIGH), the parity generator detects whether an even or odd number of bits on the A port are HIGH and compares these with the condition of the parity select (ODD/EVEN). If the Parity Select is HIGH and an even number of A inputs are HIGH, the Parity output is HIGH.

In receiving mode (T/R LOW), the parity select and number of HIGH inputs on port B are compared to the condition of the Parity input. If an even number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, then ERROR will be HIGH to indicate no error. If an odd number of bits on the B port are HIGH, the parity select is HIGH, and the PARITY input is HIGH, the ERROR will be LOW indicating an error.

Function Table

Number of Inputs That Are High	Inputs			Input/ Output	Outputs	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	Parity	$\overline{ERROR}$	Outputs Mode
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Immaterial	H	X	X	Z	Z	Z

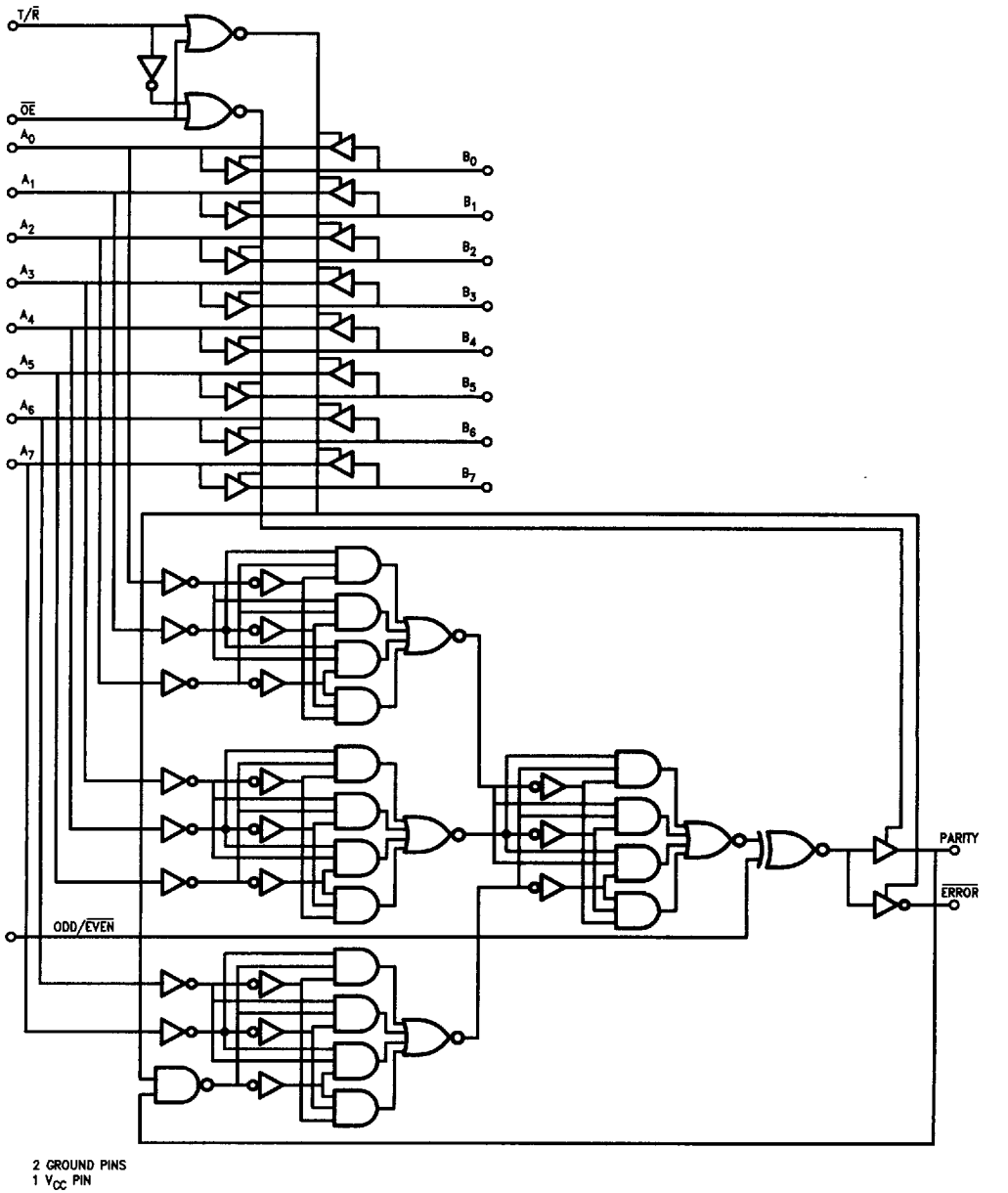
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Function Table

Inputs		Outputs
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High-Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Functional Block Diagram



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage 54F 10%V_{CC}	2.5			V	Min	I_{OH} = −1 mA (A_n)
	54F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n, B_n, Parity, $\overline{ERROR}$)
	54F 10% V_{CC}	2.0					I_{OH} = −12 mA (B_n, Parity, $\overline{ERROR}$)
	74F 10% V_{CC}	2.5					I_{OH} = −1 mA (A_n)
	74F 10% V_{CC}	2.4					I_{OH} = −3 mA (A_n B_n, Parity, $\overline{ERROR}$)
	74F 10% V_{CC}	2.0					I_{OH} = −15 mA (B_n, Parity, $\overline{ERROR}$)
	74F 5% V_{CC}	2.7					I_{OH} = −1 mA (A_n)
	74F 5% V_{CC}	2.7					I_{OH} = −3 mA (A_n, B_n, Parity, $\overline{ERROR}$)
V_{OL}	Output LOW Voltage 54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA (A_n)
	54F 10% V_{CC}			0.55			I_{OL} = 48 mA (B_n, Parity, $\overline{ERROR}$)
	74F 10% V_{CC}			0.5			I_{OL} = 24 mA (A_n)
	74F 10% V_{CC}			0.55			I_{OL} = 64 mA (B_n Parity, $\overline{ERROR}$)
I_{IH}	Input HIGH Current			20	μA	Max	V_{IN} = 2.7V (ODD/$\overline{EVEN}$)
				40			V_{IN} 2.7V (T/$\overline{R}$, $\overline{OE}$)
I_{BVI}	Input HIGH Current Breakdown Test			100	μA	V_{CC} = 0	V_{IN} = 7.0V (T/$\overline{R}$, $\overline{OE}$, ODD/$\overline{EVEN}$)
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)			1.0	mA	Max	V_{IN} = 5.5V (Parity, B_n)
				2.0			V_{IN} = 5.5V (A_n)
I_{IL}	Input LOW Current			−20	μA	Max	V_{IN} = 0.5V (ODD/$\overline{EVEN}$)
				−40			V_{IN} = 0.5V (T/$\overline{R}$, $\overline{OE}$)
I_{OZH}	Output Leakage Current			50	μA	Max	V_{OUT} = 2.7V ($\overline{ERROR}$)
I_{OZL}	Output Leakage Current			−50	μA	Max	V_{OUT} = 0.5V ($\overline{ERROR}$)
I_{IH} + I_{OZH}	Output Leakage Current			70	μA	Max	$V_{I/O}$ = 2.7V (B_n, Parity)
				90			$V_{I/O}$ = 2.7V (A_n)
I_{IL} + I_{OZL}	Output Leakage Current			−70	μA	Max	$V_{I/O}$ = 0.5V (B_n, Parity)
				−90			$V_{I/O}$ = 0.5V (A_n)
I_{OS}	Output Short-Circuit Current	−60		−150	mA	Max	V_{OUT} = 0V (A_n)
		−100		−225			V_{OUT} = 0V (B_n, Parity, $\overline{ERROR}$)
I_{CEX}	Output HIGH Leakage Current			250	μA	Max	V_{OUT} = V_{CC} ($\overline{ERROR}$)
				1.0	mA	Max	V_{OUT} = V_{CC} (B_n, Parity)
				2.0	mA	Max	V_{OUT} = V_{CC} (A_n)
I_{ZZ}	Bus Drainage Test			500	μA	0.0V	V_{OUT} = 5.25V (A_n, B_n, Parity, $\overline{ERROR}$)
I_{CCH}	Power Supply Current		101	125	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		112	150	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		109	145	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			54F $T_A, V_{CC} = Mil$ $C_L = 50\ pF$		74F $T_A, V_{CC} = Com$ $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n, B_n to A_n	2.5 3.0	4.5 4..9	8.0 7.5	2.5 3.0	9.5 8.5	2.5 3.0	9.0 8.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay A_n to Parity	6.5 7.0	10.1 10.9	14.0 15.0	5.5 5.5	18.0 20.5	6.0 6.0	16.0 16.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to PARITY	4.5 4.5	7.8 8.8	11.0 12.0	4.0 4.5	14.0 16.5	4.0 4.5	13.0 13.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay ODD/$\overline{EVEN}$ to $\overline{ERROR}$	4.5 4.5	7.5 8.2	11.0 12.0	4.0 4.5	14.0 16.5	4.0 4.5	13.0 13.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay B_n to $\overline{ERROR}$	8.0 8.0	14.0 15.0	20.5 21.5	7.5 7.5	27.0 28.5	7.5 7.5	23.0 23.5	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay PARITY to $\overline{ERROR}$	7.0 7.5	10.8 11.8	15.5 16.5	6.0 6.5	20.0 22.0	6.0 7.5	17.0 18.5	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to A_n/B_n	3.0 4.0	5.0 6.5	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to A_n/B_n	1.0 1.0	4.5 4.9	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns	2–5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to $\overline{ERROR}$ (Note 1)	3.0 4.0	5.0 7.7	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to $\overline{ERROR}$	1.0 1.0	4.5 4.9	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns	2–5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to PARITY	3.0 4.0	5.0 7.7	8.0 10.0	2.5 3.5	11.0 13.5	2.5 3.5	9.5 11.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to PARITY	1.0 1.0	4.6 5.1	8.0 7.5	1.0 1.0	9.5 8.5	1.0 1.0	9.0 8.0	ns	2–5

Note 1: These delay times reflect the TRI-STATE recovery time only and not the signal time through the buffers or the parity check circuity. To assure VALID information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output after the $\overline{ERROR}$ pin has been enabled (Output Enable times). VALID data at the $\overline{ERROR}$ pin ≥ (A to PARITY) + (Output Enable Time).