AZT71

Programmable Capacitive Tuning IC

www.azmicrotek.com

DESCRIPTION

The AZT71 is a digitally programmed capacitor specifically designed to tune a crystal or SAW based oscillator to a desired center frequency. The desired capacitance value for production trimming is set by a serial data stream when placed into a programming mode. The AZT71 is designed to be a labor and cost saving device within the oscillator production process.

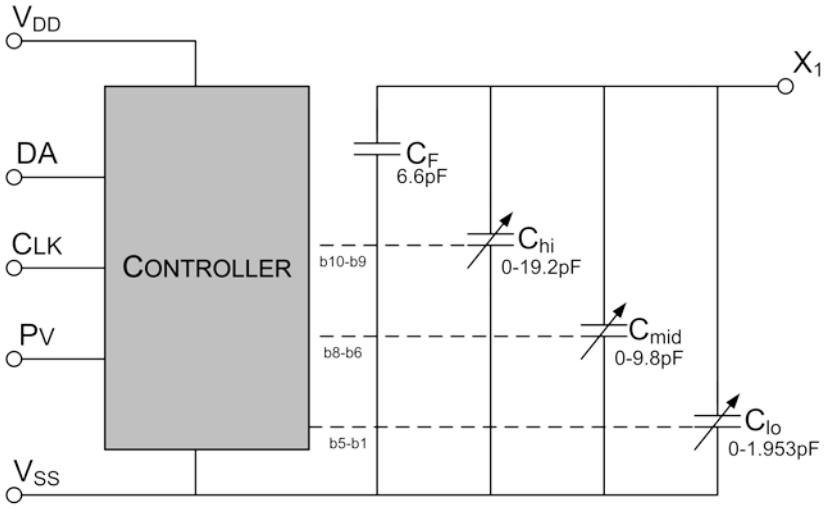
Using EEPROM technology, the capacitance can be re-tuned as needed during the production process by repeating the programming steps thereby increasing production yield.

The AZT71 is available in an SON8 package (1.5mm x 1.0mm) for very small form factor oscillators. Also available in MLP6 and TSOT6.

FEATURES

- Capacitive tuning range of 6.6pF to 37.553pF
  (See AZT70 for different values)
- 0.063pF minimum step size
- Reprogrammable through nonvolatile EEPROM storage
- May be placed in parallel for greater capacitance values
- Very low supply current
- 2.5V to 3.6V supply voltage

BLOCK DIAGRAM



APPLICATIONS

- Fast production tuning of crystal or SAW oscillators
- Filters requiring capacitive tuning

PACKAGE AVAILABILITY

- SON8
- MLP6
- TSOT6
- All are Green/RoHS/Pb-Free

Order Number	Package	Marking
AZT71QG[1]	SON8	Y <Date Code>[2]
AZT71HG[1]	TSOT6	Y1G<Date Code>[2]
AZT71MG[1]	MLP6	Y1G<Date Code>[2]

[1] Tape & Reel - Add 'R1' at end of order number for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description SON8 Package (1.5mm x 1.0mm)

Pin	Name	Type	Function
1	X_1	Output	Capacitance
2	NC	n/a	not connected
3	V_{SS}	Power	Negative Supply (GND)
4	V_{DD}	Power	Positive Supply
5	DA	Input	Programming Data Input
6	CLK	Input	Programming Clock Input
7	NC	n/a	not connected
8	PV	Input	Programming Voltage

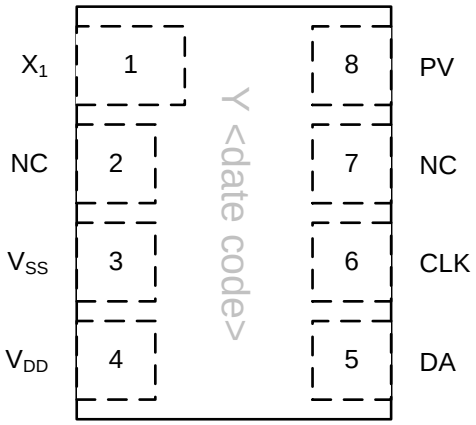


Figure 1 - Pin Configuration SON8

Table 2 - Pin Description TSOT6 Package

Pin	Name	Type	Function
1	X_1	Output	Capacitance
2	V_{SS}	Power	Negative Supply (GND)
3	PV	Input	Programming Voltage
4	CLK	Input	Programming Clock Input
5	DA	Input	Programming Data Input
6	V_{DD}	Power	Positive Supply

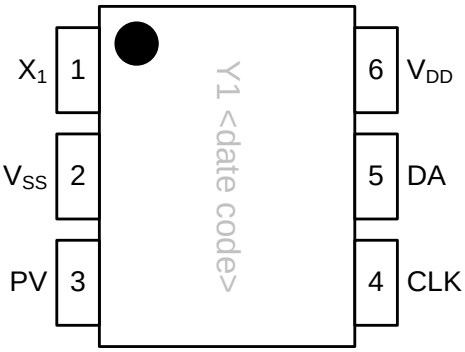


Figure 2 - Pin Configuration TSOT6

Table 3 - Pin Description 6MLP Package (2.0mm x 2.0mm)

Pin	Name	Type	Function
1	X_1	Output	Capacitance
2	V_{SS}	Power	Negative Supply (GND)
3	V_{DD}	Power	Positive Supply
4	DA	Input	Programming Data Input
5	CLK	Input	Programming Clock Input
6	PV	Input	Programming Voltage

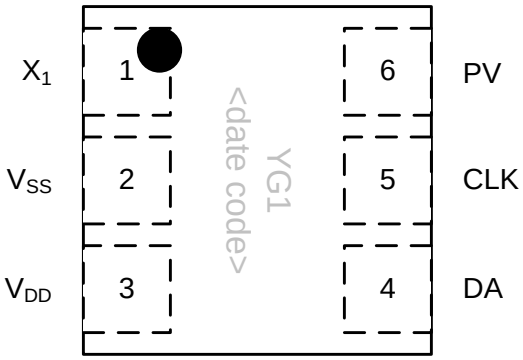


Figure 3 - Pin Configuration 6MLP

ENGINEERING NOTES

CAPACITOR STRUCTURE

The AZT71 capacitance value is composed of four parallel capacitors banks, C_F is a fixed capacitor value of 6.6pF and C_{hi}, C_{mid} & C_{lo} are variable capacitors of differing ranges and resolutions as seen in Table 4. Capacitors composing C_{hi}, C_{mid} and C_{lo} are set with a binary control word through an 11-bit shift register described in **PROGRAMMING THE AZT71**. The values of each C_{hi}, C_{mid} and C_{lo} stepping are detailed in the complete Nominal Capacitance Binary Mapping spreadsheet.

$$C_{Total} = C_F + C_{hi} + C_{mid} + C_{lo}$$

Table 4 - AZT71 Capacitor Structure

Internal Capacitor	Min Value (pF)	Max Value (pF)	Step Size (pF)
C_F	6.6	6.6	n/a
C_{hi}	0	19.2	6.4
C_{mid}	0	9.8	1.4
C_{lo}	0	1.953	0.063
Total	6.6	37.553	

PROGRAMMING THE AZT71

CONTROL WORD

The capacitance in the AZT71 is controlled by an 11-bit shift register with the data input bit definitions shown in Table 5. The control word data is inputted serially on the rising edge of the CLK signal with bit0 first and bit10 last.

Table 5 - AZT71 Control Word Definition

11-bit Control Word										
bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
C_{hi}		C_{mid}			C_{lo}					Not Used
MSB	LSB	MSB	---	LSB	MSB	---	---	---	LSB	

The control word mapping is a binary word for each of C_{hi}, C_{mid} and C_{lo} where higher number bits are more significant. Figure 4 shows the capacitance value mapping for the AZT71. The detailed Nominal Capacitance Binary Mapping can be located on the AZM website.

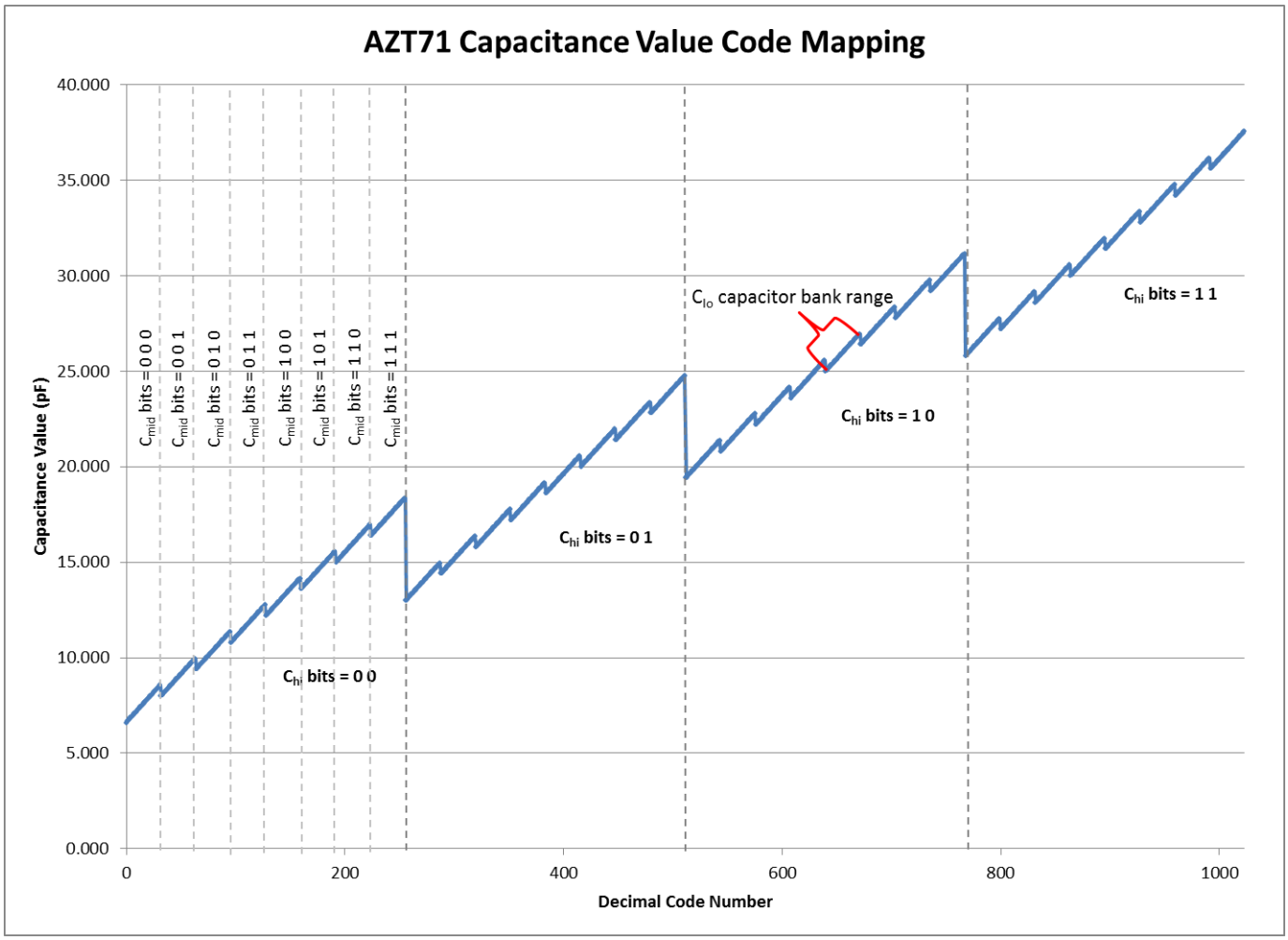


Figure 4 – AZT71 Capacitance Value Mapping

AZT71 FUNCTIONAL MODES

The AZT71 is designed to be used in 2 functional modes, Programming and Operational.

In the *Programming mode*, the AZT71 is used by the manufacturer to set the capacitance value to control the desired center frequency of the oscillator. The programming mode uses either the shift registers or EEPROM (detailed later) and gives the manufacturer access to pins DA, CLK, and PV which allow the AZT71 to be programmed with an accompanying programming board (Figure 5). Arizona Microtek can provide this board (AZPB70) along with software that works through all the programming steps/functions described in the next sections.

In the *Operational mode*, the EEPROM internal to the AZT71 has already been programmed with the desired factory settings. Pins DA, CLK, and PV are to be disconnected, thereby allowing the AZT71's internal pull-downs to place the pins at ground potential. In the operational mode, only 3 pins are necessary for hookup (Figure 6).

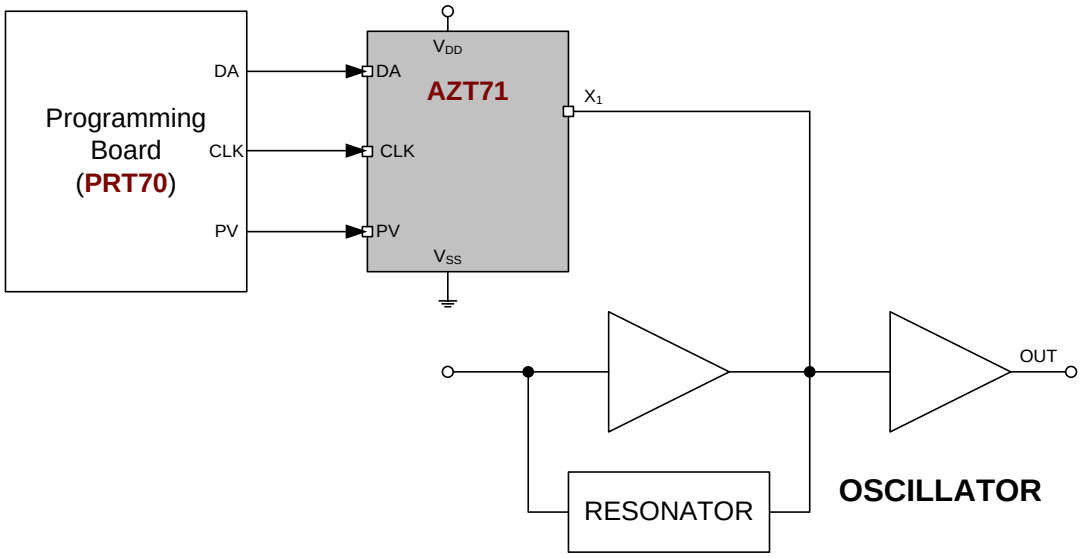


Figure 5 – AZT71 in Programming Mode

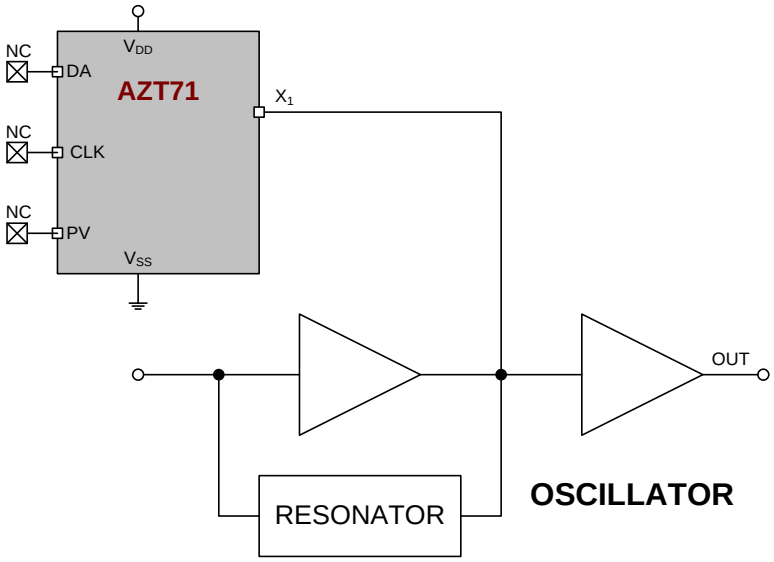


Figure 6 – AZT71 in Operational Mode

PROGRAMMING MODES

The AZT71 has two capacitance setting modes from which bits are set and the matching capacitors are selected.

- **Reading directly from the shift register**
  - This is useful for testing the capacitance and subsequent oscillator frequency. This mode is active after the last bit is shifted in and when the CLK pin is left logic high. *For the shift register, capacitors are selected when bits are active HIGH.*

- **Reading from the value contained in the EEPROM**
  - Prevents customer adjustment and retains factory programming and is active when the CLK pin is at logic low or not connected. *For the EEPROM, capacitors are selected when bits are active LOW.*

PROGRAMMING FROM THE SHIFT REGISTER

To initially determine the capacitance value for the desired center frequency of the oscillator one should set the capacitance of the AZT71 directly from the active shift register bits. To accomplish this, the CLK pin is left high after the last control word bit has been shifted in. Figure 7 shows the control word 11001100100 has been serially entered into the register. Note that bit0 is the 1st bit to enter and bit10 is the last. In the AZT71, bit0 does not affect the capacitance value but still must be included in the serial bit stream. For the shift register, capacitors are selected when bits are active HIGH.

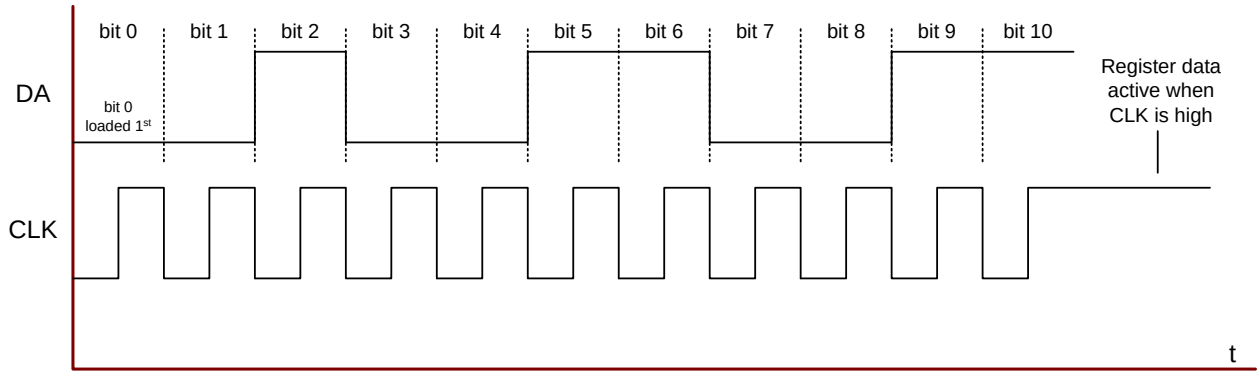


Figure 7 - Shift register programming

WRITING DATA TO THE EEPROM

Once the desired capacitance value has been determined, the digital control word can be written or re-written into the EEPROM. By storing the control word in the EEPROM, the customer is prevented from making adjustments from the factory set programming data. This is accomplished within the AZT71 with internal pull-downs on the DA, PV, and CLK pins. The detailed sequence for writing data to the EEPROM within the AZT71 is described in Table 6. Note that with EEPROM, capacitors are selected when bits are active LOW.

Table 6 – Data writing sequence for EEPROM

Step	Action
1	Determine the desired capacitor control word with the operational power supply voltage and desired oscillator conditions
2	Set the V_{DD} supply voltage to +5.0V
3	If EEPROM is not already erased, erase EEPROM (see **ERASING THE** EEPROM)
4	Read the current state of the EEPROM bits (see **READING BACK FROM THE EEPROM**)
5	Compare the desired control word to the stored EEPROM control word. Count the number of differences so as to prevent double/redundant writing
6	One bit at a time, load the first desired control word bit (bit selection for EEPROM is active LOW)
7	Set the PV pin to +6V (≥5.6V, ≤6.1V) with the pulse and idle shown in timing diagram (Figure 10)
8	Progress through all necessary control word bits by repeating steps 5 & 6 until all bits are set to the desired control word.
9	Verify the correct EEPROM contents by reading back the individual bits

For an example of writing bits into the EEPROM, suppose the desired capacitance is 7.23pF. The control word becomes '00000010100' (Figure 8). Also suppose the EEPROM bits have been erased and therefore logic high (The AZT71 is initially shipped in this condition). Since bit0 is the first bit to be loaded, the bit sequence becomes 0-0-1-0-1-0-0-0-0-0-0. However, as described before, selecting bits for the EEPROM are active LOW, which will invert the logical values in the sequence to 1-1-0-1-0-1-1-1-1-1-1 (Figure 9). Note the differences between the EEPROM bits and the converted control word. Since there are 2 differences, two write cycles are required as only 1 bit should be written at a time. Figure 10 shows the timing for bit2 while Figure 11 shows the timing for bit4.

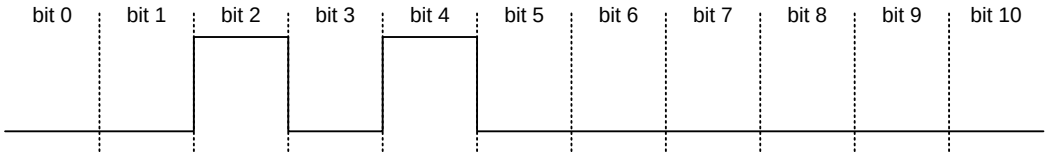


Figure 8 – Desired control word

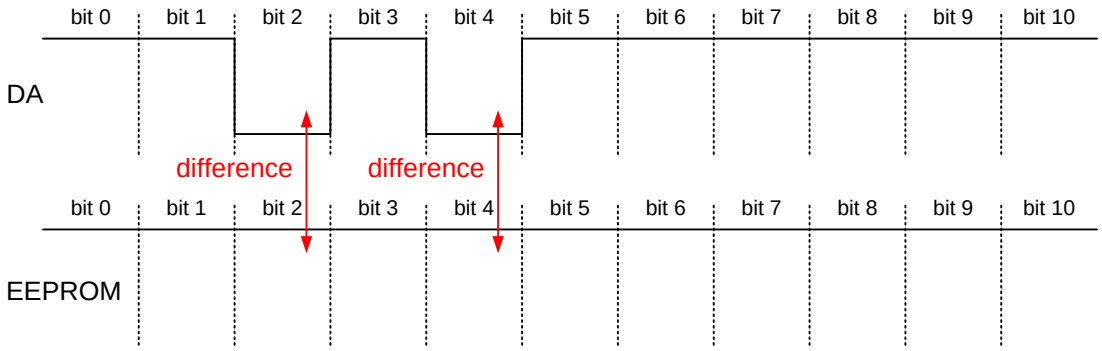


Figure 9 – Converted control word and differences from known EEPROM states

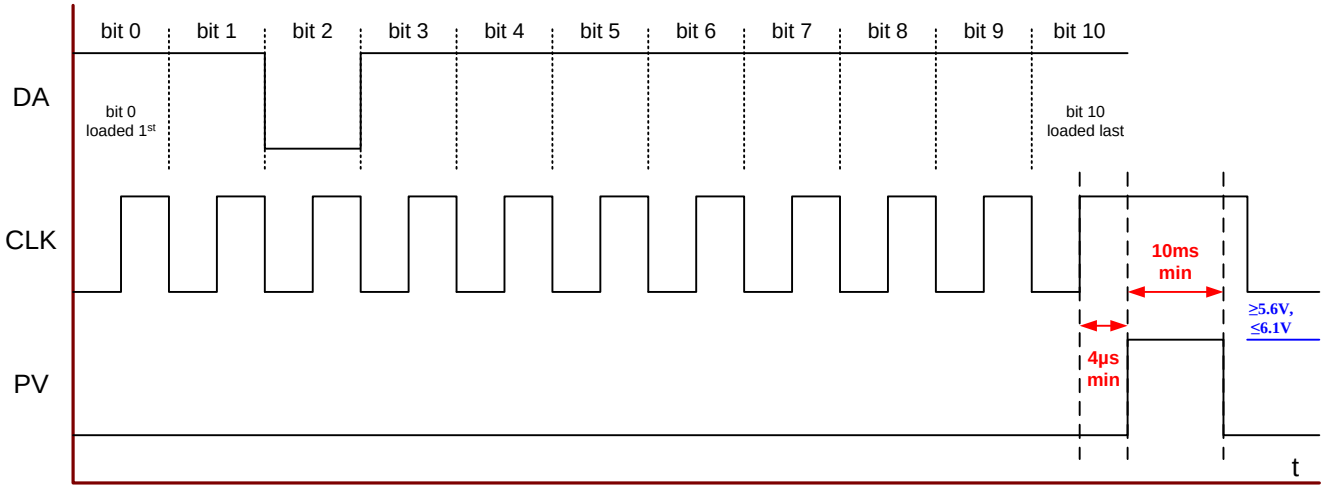


Figure 10 – First programming cycle to program bit2 into the EEPROM

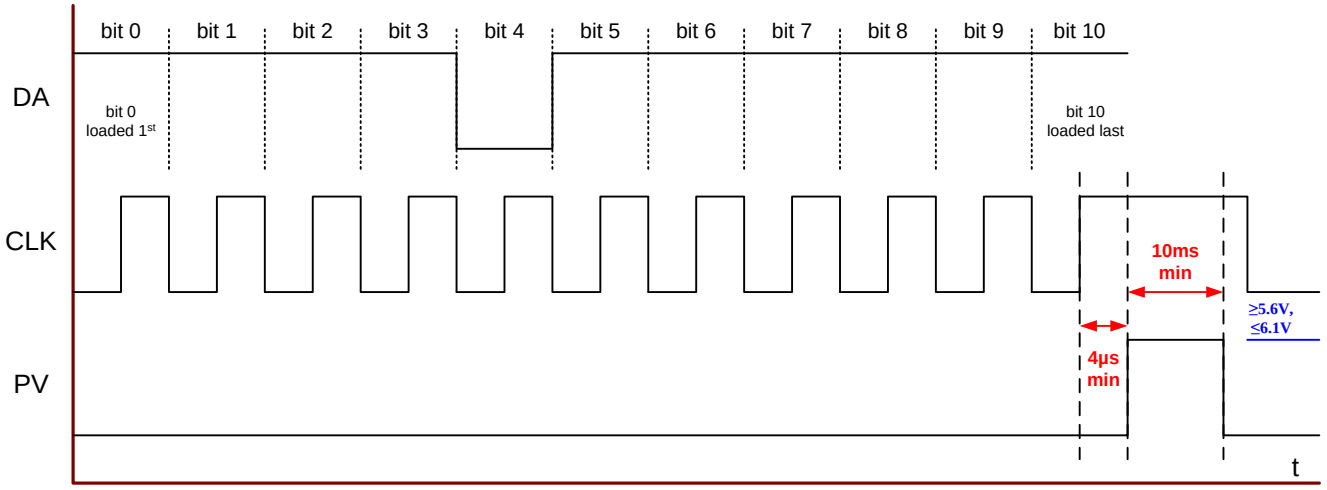


Figure 11 – Second programming cycle to program bit4 into the EEPROM

READING BACK FROM THE EEPROM

During programming, the PV pin is used to program the necessary control bits into the EEPROM. However, it is also used to read the bits currently programmed into the EEPROM. When the PV pin is not used during programming, the AZT71 provides a weak pull-up and pull-down on the pin. This allows the EEPROM data to be shifted out to the PV pin and read after the CLK sequence is complete and when the DA & CLK pins are high (Figure 12). Each EEPROM bit is selected by setting the DA signal low (EEPROM selection is active low) during the CLK sequence. With an external 68kΩ resistor pull-up to V_{DD} on the PV pin, a low EEPROM bit produces ≤ 0.4V level while a high EEPROM bit produces a ≥ 0.6*V_{DD} level.

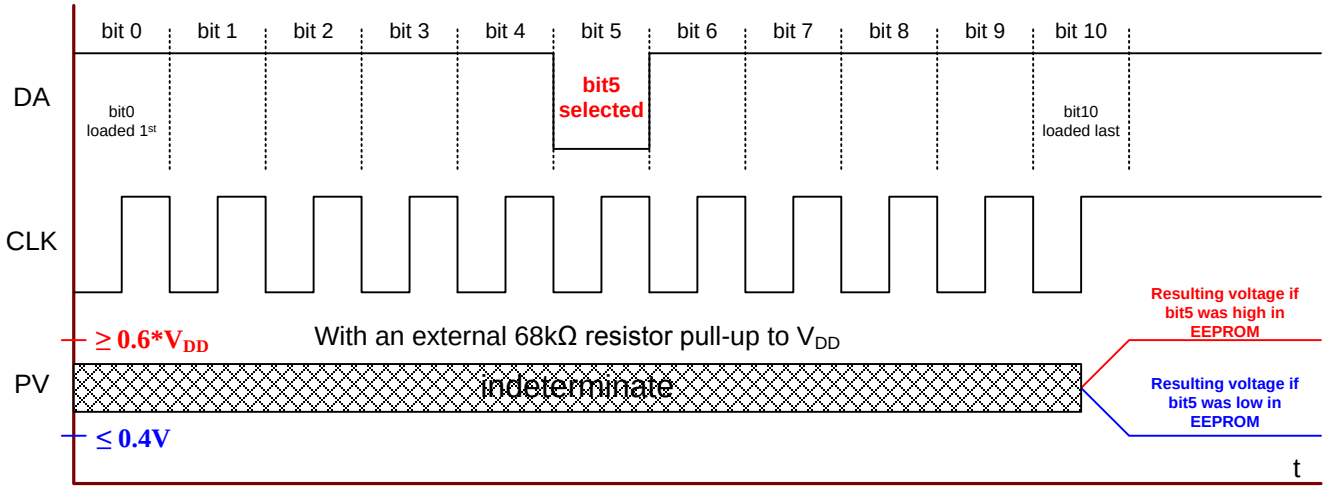


Figure 12 – Timing diagram to read bits from EEPROM

ERASING THE EEPROM

The EEPROM can be erased by initiating a programming cycle with all DA bits set high, including bit9 and bit10. After the programming cycle, all the EEPROM bits are set low (logical high) except for the check bit (bit0), which remains high.

Table 7 – Erase sequence for EEPROM

Step	Action
1	Set the V_{DD} supply voltage to +5.0V
2	Load the programming word bits all high.
3	Set the PV pin to +6V (≥5.6V, ≤6.1V) with the pulse and idle shown in timing diagram (Figure 13)
4	Verify the correct EEPROM contents by reading back the individual bits

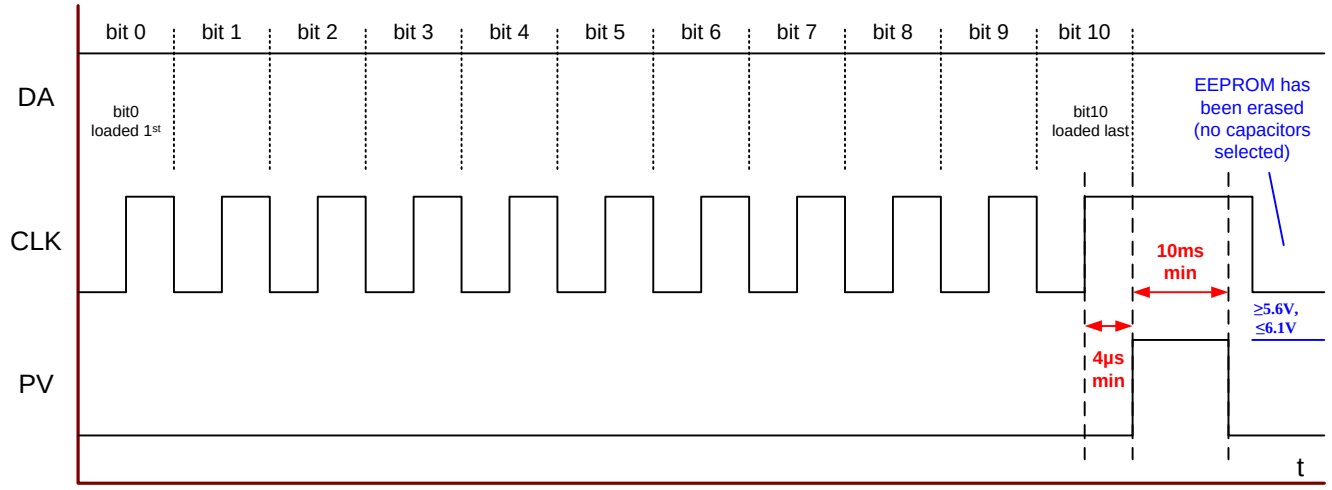


Figure 13 – Programming Sequence for erasing the EEPROM

PROGRAMMING VOLTAGE LIMIT CIRCUIT

Some existing programming circuits use a current source connected to a 6.5 – 8.0 V supply. That circuit produces an excessive voltage on the PV pin, which can damage the AZT71. A simple modification eliminates the issue and maintains full programming compatibility with existing programming methods. A 5.6 V, ½ watt Zener, 1N5232B or equivalent, placed between the PV pin and ground will limit the voltage while still allowing the programming circuit to generate the current required for programming fuse link type parts.

PERFORMANCE DATA

Table 8 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Rating	Unit
V_{DD}	Power Supply	0 to +6.5	V
V_I[1]	Input Voltage	-0.5 to V_{DD} + 0.5	V
T_A	Operating Temperature Range	-40 to +85	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
ESD_{HBM}	Human Body Model	TBD	V
ESD_{MM}	Machine Model	TBD	V
ESD_{CDM}	Charged Device Model	TBD	V

[1] PV Pin can exceed V_{DD} by 1.2V during the programming interval

Table 9 – DC Characteristics

DC Characteristics (V_{DD} = 2.375V to 3.6V unless otherwise specified, T_A = -40 to 85 °C)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
C_{PV}	Nominal capacitance variation across process		-15		+15	%
C_{VV}	Capacitance variation across output voltage	Voltage variation at X_1 pin, 100MHz			±150	ppm/V
C_{TV}	Capacitance variation across temperature	100MHz - Zero Code		325		ppm/°C
		100MHz - Mid Code[1]		40		
		100MHz - Full Scale		130		
V_{IH}	Input HIGH Voltage	DA, CLK	0.8 * V_{DD}			V
V_{IL}	Input LOW Voltage	DA, CLK	0.2 * V_{DD}			V
$R_{PD,D}$	Pull-down Resistor	DA		75k		Ω
$R_{PD,CLK}$	Pull-down Resistor	CLK		75k		Ω
$R_{PD,PV}$	Pull-down Resistor	PV		170k		Ω
V_{OH}	Output High Voltage	PV Pin when reading EEPROM bits 68kΩ external pull-up resistor to V_{DD}		0.6 * V_{DD}		V
V_{OL}	Output Low Voltage			0.4		V
V_{PP}	Programming Voltage (V_{DD}=5.0V)	PV pin when programming EEPROM	5.6	6.0	6.1	V
I_{DD}	Power Supply Current	Normal Operation		7.0	50	µA
I_{DDPROG}	Power Supply Current	Programming Mode			20	µA
t_{MEM}	EEPROM Data Retention			20		yrs
T_{prog}	Programming Temperature			25		°C
Cy_{prog}	Programming Cycle		10			k

[1] Bit4, Bit7 High

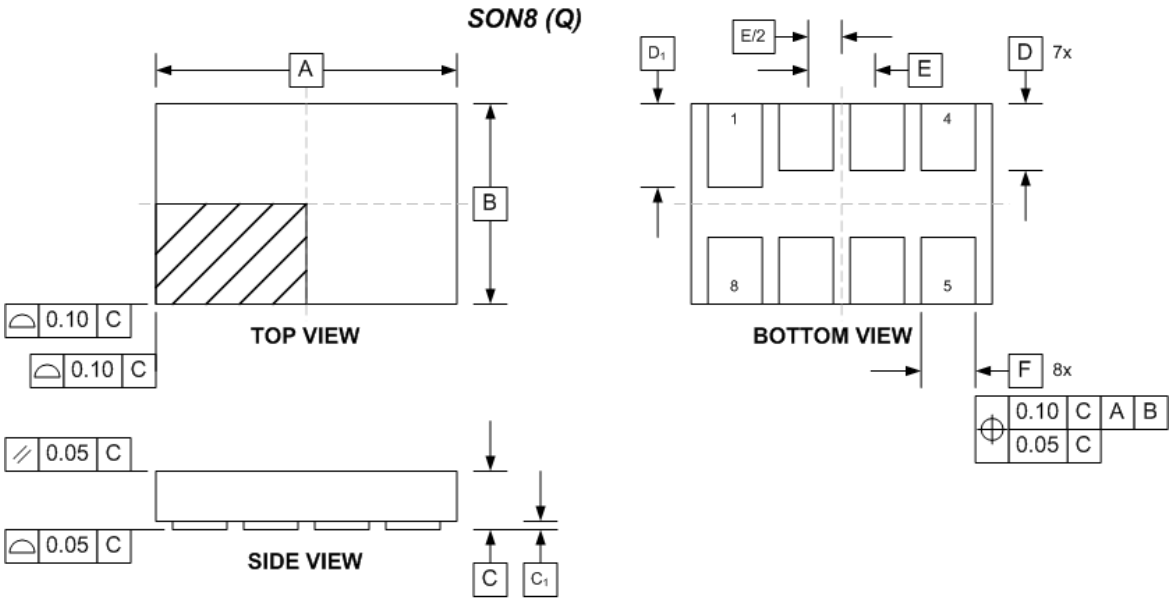
Table 10 – AC Characteristics

AC Characteristics (V_{DD} = 2.375V to 3.6V unless otherwise specified, T_A = -40 to 85 °C)

Symbol	Characteristic	Conditions	Min	Typ	Max	Unit
C_F	Fixed Capacitance			6.6		pF
C_{hi}	Step Size			6.4		pF
	Max Value			19.2		pF
C_{mid}	Step Size			1.4		pF
	Max Value			9.8		pF
C_{lo}	Step Size			0.063		pF
	Max Value			1.953		pF
CLK	Max CLK rate	50% duty cycle			5	MHz
T_{prog}	Programming Time (V_{DD}=5.0V, PV=6.0V)	per bit programmed			10	ms
Q	Q Value	20MHz - Full Scale	150	300		
		20MHz - Mid Scale	100	200		
		80MHz - Full Scale	40	80		
		80MHz - Mid Scale	40	80		
		155MHz - Full Scale	25	50		
		155MHz - Mid Scale	25	50		

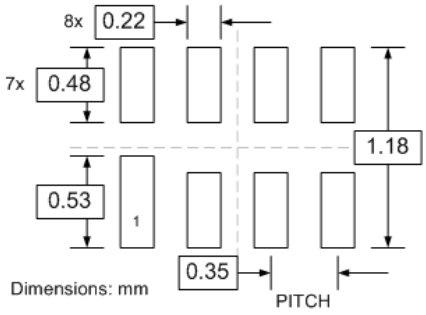
PACKAGE DIAGRAM

SON8 (1.5x1.0x0.4mm)
Green/RoHS compliant/Pb-Free
MSL=1



	MILLIMETERS	
DIM	MIN	MAX
A	1.50 BSC	
B	1.00 BSC	
C	---	0.40
C_1	0.00	0.05
D	0.25	0.35
D_1	0.30	0.40
E	0.35 BSC	
F	0.15	0.25

PCB LAND PATTERN/FOOTPRINT

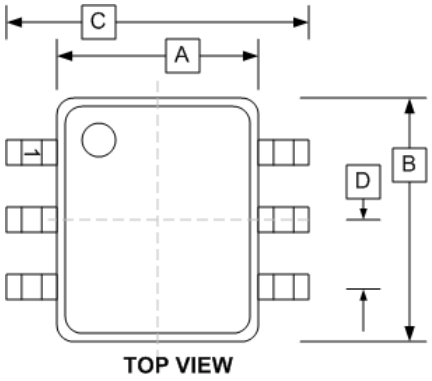


PACKAGE DIAGRAM

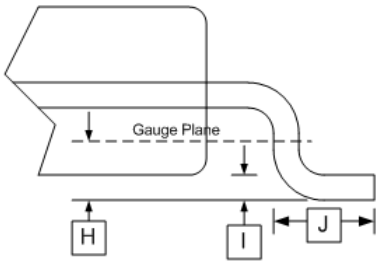
TSOT6

Green/RoHS compliant/Pb-Free

MSL=1

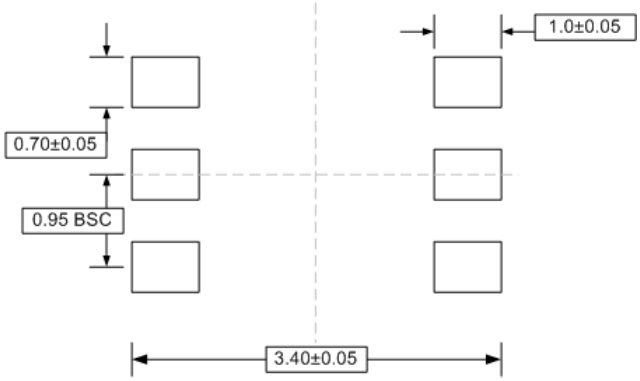


TSOT6 (H)



PCB LAND PATTERN/FOOTPRINT

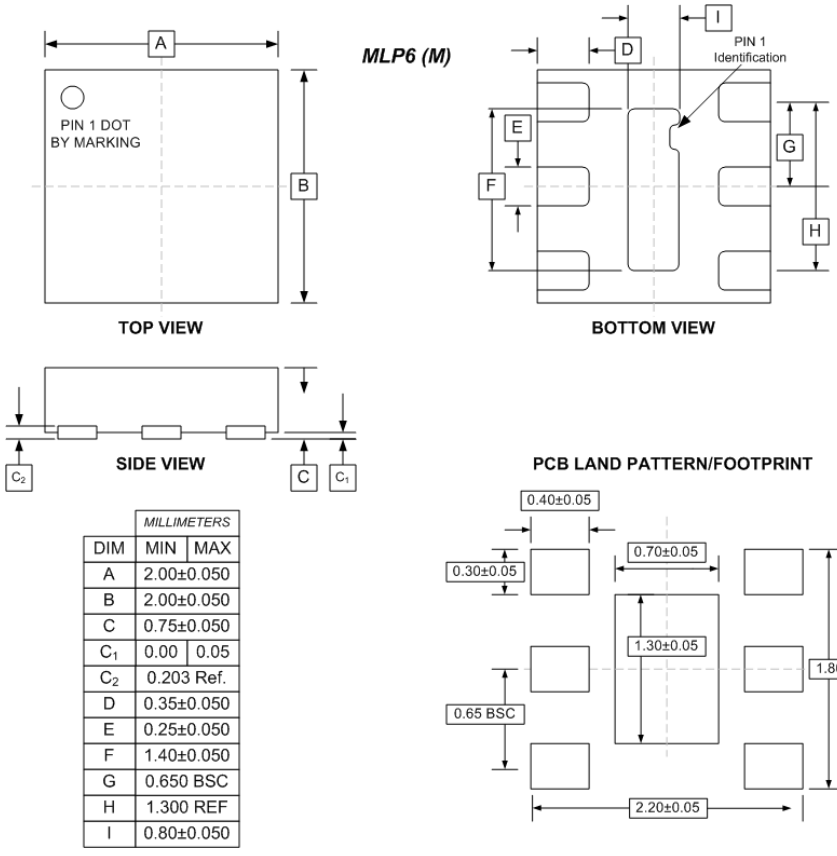
Dimensions in mm



	MILLIMETERS	
DIM	MIN	MAX
A	1.60 BSC	
B	2.90 BSC	
C	2.80 BSC	
D	0.950 TYP	
E	0.00	0.10
F	0.87±0.03	
G	0.30	0.50
H	0.25 BSC	
I	0.127	
J	0.40±0.100	

PACKAGE DIAGRAM

MLP6 (2.0mm x 2.0mm)
Green/RoHS compliant/Pb-Free
MSL=1



	MILLIMETERS	
DIM	MIN	MAX
A	2.00±0.050	
B	2.00±0.050	
C	0.75±0.050	
C_1	0.00	0.05
C_2	0.203 Ref.	
D	0.35±0.050	
E	0.25±0.050	
F	1.40±0.050	
G	0.650 BSC	
H	1.300 REF	
I	0.80±0.050	