

32-Channel Serial to Parallel Converter With High Voltage Push-Pull Outputs

Features

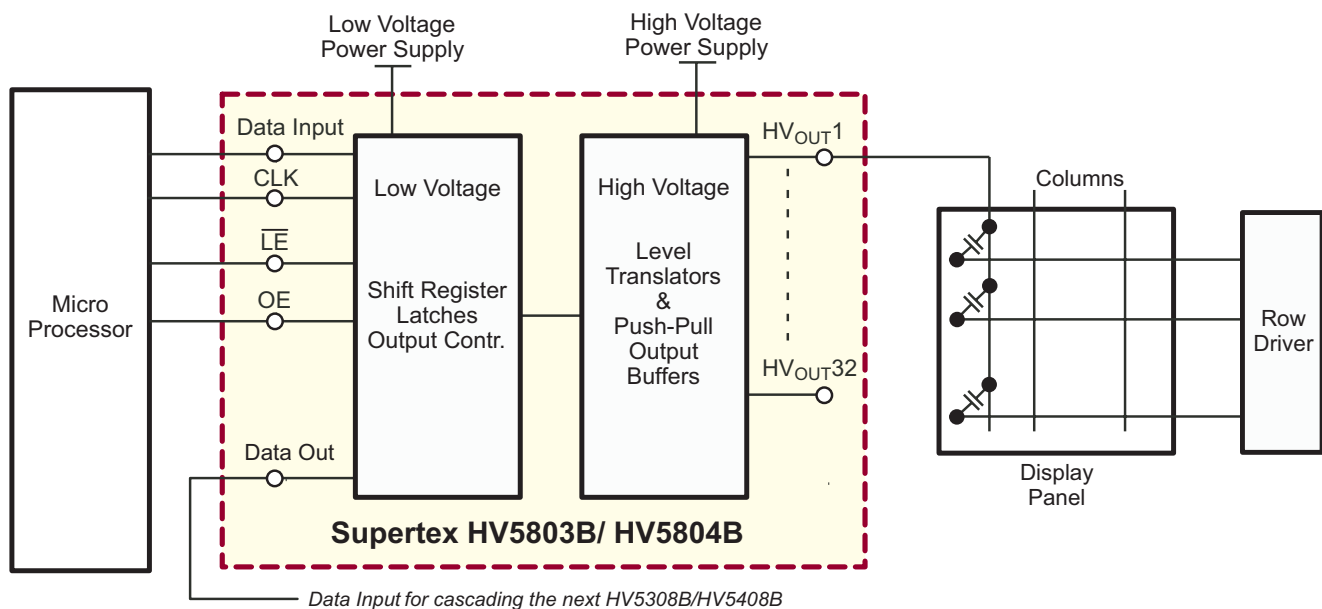
- ▶ Processed with HVCMOS® technology
- ▶ Low power level shifting
- ▶ Source/sink current minimum 20mA
- ▶ Shift register speed 8MHz
- ▶ Latched data outputs
- ▶ CMOS compatible inputs
- ▶ Forward and reverse shifting options
- ▶ Diode to V_{pp} allows efficient power recovery

General Description

The HV5308B and HV5408B are low voltage serial to high voltage parallel converters with push-pull outputs. These devices have been designed for use as drivers for AC-electroluminescent displays. They can also be used in any application requiring multiple output high voltage current sourcing and sinking capabilities, such as driving plasma panels, vacuum fluorescent, or large matrix LCD displays.

These devices consist of a 32-bit shift register, 32 latches, and control logic to enable outputs. Q1 is connected to the first stage of the shift register through the Output Enable logic. Data is shifted through the shift register on the low to high transition of the clock. The HV5408B shifts in the counterclockwise direction when viewed from the top of the package, while the HV5308B shifts in the clockwise direction. A data output buffer is provided for cascading devices. This output reflects the current status of the last bit of the shift register (32). Operation of the shift register is not affected by the \overline{LE} (latch enable) or the OE (output enable) inputs. Transfer of data from the shift register to the latch occurs when the \overline{LE} input is high. The data in the latch is retained when \overline{LE} is low.

Typical Application Circuit



Ordering Information

| Device | Package Options | | | |
|---------|-------------------------------------|-------------------------------------------------------------|-------------------------------------|-------------------------------|
| | 44-J Lead Quad Ceramic Chip Carrier | 44-J Lead Quad Ceramic Chip Carrier (MIL-STD-883 Processed) | 44-J Lead Quad Plastic Chip Carrier | 44-Lead Quad Plastic Gullwing |
| HV5308B | HV5308DJ-B | HV5308DJ-B | HV5308PJ-B | HV5308PG-B |
| | - | - | HV5308BPJ-B-G | HV5308PG-B-G |
| HV5408B | HV5408DJ-B | HV5408DJ-B | HV5408PJ-B | HV5408PG-B |
| | - | - | HV5408PJ-B-G | HV5408PG-B-G |

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

| Parameter | Value | |
|-------------------------------------------------------------|--------------------------|-----------------|
| Supply voltage, V_{DD}^2 | -0.5V to +16V | |
| Supply voltage, V_{PP} | -0.5V to +90V | |
| Logic input levels ² | -0.5V to $V_{DD} + 0.5V$ | |
| Ground current ³ | 1.5A | |
| Continuous total power dissipation ¹ | Plastic | 1200W |
| | Ceramic | 1500W |
| Operating temperature range | Plastic | -40°C to +85°C |
| | Ceramic | -55°C to +125°C |
| Storage temperature range | -65°C to +150°C | |
| Lead temperature 1.6mm (1/16 inch) from case for 10 seconds | 260°C | |

Notes:

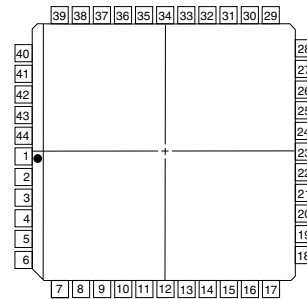
1. Device will survive (but operation may not be specified or guaranteed) at these extremes.
2. All voltages are referenced to GND.
3. Duty cycle is limited by the total power dissipated in the package.
4. For operation above 25°C ambient derate linearly to maximum operating temperature at 20mW/°C for plastic and at 15mW/°C for ceramic.

Recommended Operating Conditions

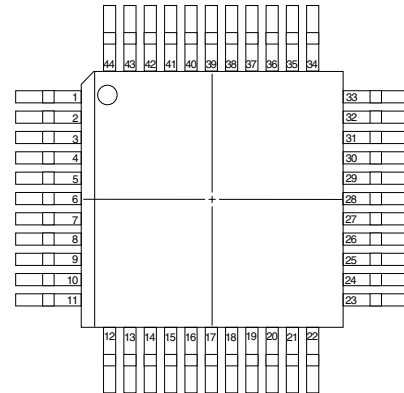
(Over -40°C to 85°C for plastic and -55°C to 125°C for ceramic)

| Symbol | Parameter | Min | Max | Units |
|-----------|----------------------|--------------|----------|-------|
| V_{DD} | Logic voltage supply | 10.8 | 13.2 | V |
| V_{PP} | High voltage supply | 8.0 | 80 | V |
| V_{IH} | Input HIGH voltage | $V_{DD} - 2$ | V_{DD} | V |
| V_{IL} | Input Low voltage | 0 | 2 | V |
| f_{CLK} | Clock frequency | 0 | 8 | MHz |

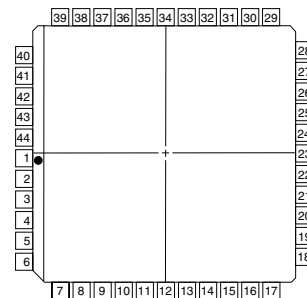
Pin Configurations



44-J Lead Quad Ceramic Chip Carrier (DJ)



44-Lead Quad Plastic Gullwing (PG)



44-J Lead Quad Plastic Chip Carrier (PJ)

Power-Up Sequence

1. Connect ground
2. Apply V_{DD}
3. Set all inputs (Data, CLK, \overline{LE} , etc.) to a known state
4. Apply V_{PP}

Power-down sequence should be the reverse of the above.

Electrical Characteristics ($V_{PP} = 60V$, $V_{DD} = 12V$, $T_A = 25^\circ C$)

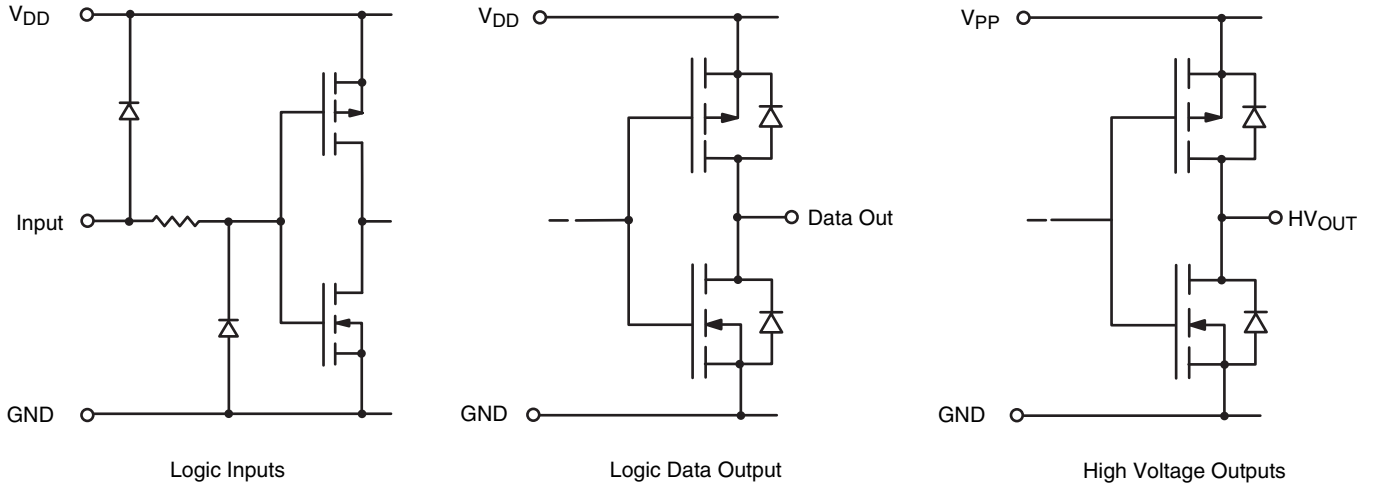
DC Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
|-----------------|-------------------------------------|------|------|---------|-----------------------------------------------------------|
| I_{PP} | V_{PP} supply current | - | 0.5 | mA | HV _{OUTPUTS} HIGH to LOW |
| I_{DDQ} | I_{DD} supply current (quiescent) | - | 100 | μA | All inputs = V_{DD} or GND |
| I_{DD} | I_{DD} supply current (operating) | - | 15 | mA | $V_{DD} = V_{DD} \text{ max}$, $f_{CLK} = 8 \text{ MHz}$ |
| V_{OH} (Data) | Shift register output voltage | 10.5 | - | V | $I_O = 100\mu A$ |
| V_{OL} (Data) | Shift register output voltage | - | 1 | V | $I_O = 100\mu A$ |
| I_{IH} | Current leakage, any input | - | 1 | μA | $V_{IN} = V_{DD}$ |
| I_{IL} | Current leakage, any input | - | -1 | μA | $V_{IN} = 0$ |
| V_{OC} | HV output clamp diode voltage | - | -1.5 | V | $I_{OL} = -100mA$ |
| V_{OH} | HV output when sourcing | 52 | - | V | $I_{OH} = -20mA$, -40 to 85°C |
| V_{OL} | HV output when sinking | - | 8 | V | $I_{OL} = 20mA$, -40 to 85°C |
| V_{OH} | HV output when sourcing | 52 | - | V | $I_{OH} = -15mA$, -55 to 125°C |
| V_{OL} | HV output when sinking | - | 8 | V | $I_{OL} = 15mA$, -55 to 125°C |

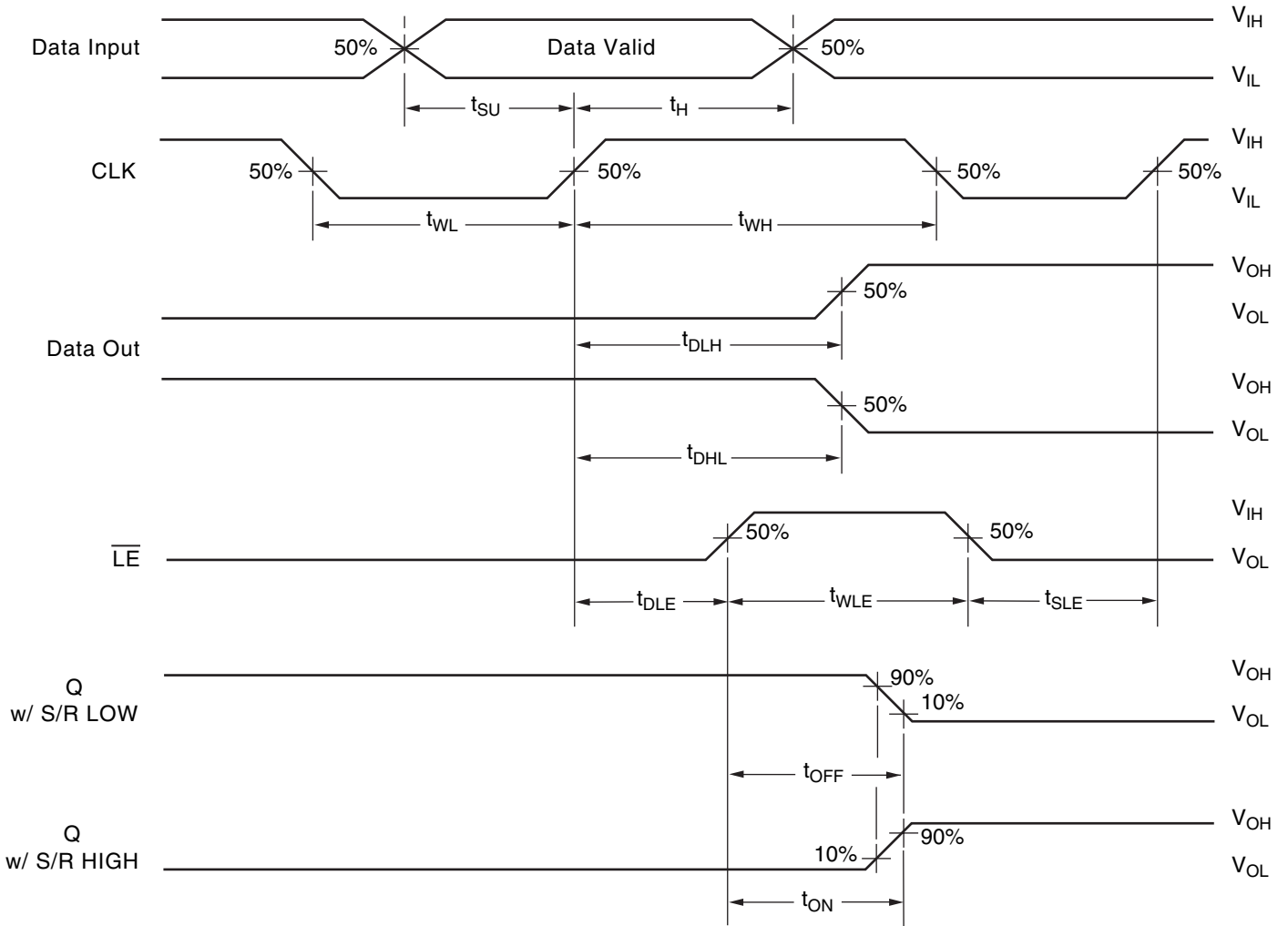
AC Characteristics

| Symbol | Parameter | Min | Max | Units | Conditions |
|----------------------|--------------------------------------------------------------------|-----|-----|-------|------------|
| f_{CLK} | Clock frequency | - | 8 | MHz | --- |
| t_{WL} or t_{WH} | Clock width, HIGH or LOW | 62 | - | ns | --- |
| t_{SU} | Setup time before CLK rises | 25 | - | ns | --- |
| t_H | Hold time after CLK rises | 10 | - | ns | --- |
| t_{DLH} (Data) | Data output delay after L to H CLK | - | 110 | ns | CL = 15pF |
| t_{DHL} (Data) | Data output delay after H to L CLK | - | 110 | ns | CL = 15pF |
| t_{DLE} | \overline{LE} delay after L to H CLK | 50 | - | ns | --- |
| t_{WLE} | Width of \overline{LE} pulse | 50 | - | ns | --- |
| t_{SLE} | \overline{LE} setup time before L to H CLK | 50 | - | ns | --- |
| t_{ON} | Delay from \overline{LE} to HV _{OUT₁} L to H | - | 500 | ns | --- |
| t_{OFF} | Delay from \overline{LE} to HV _{OUT₁} H to L | - | 500 | ns | --- |

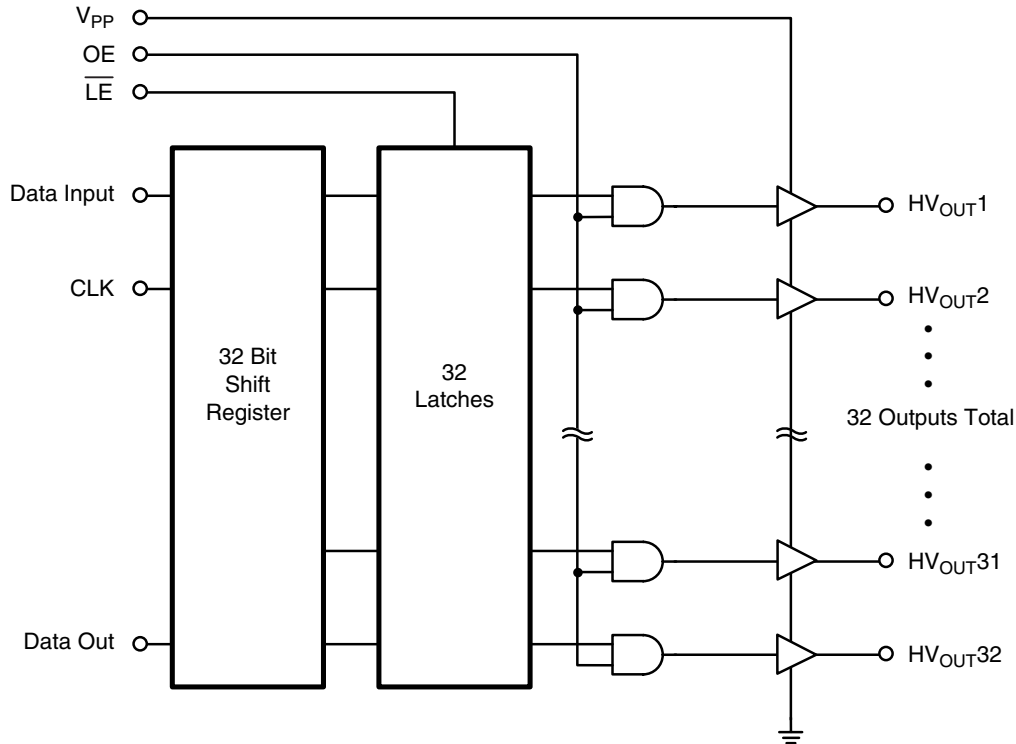
Input and Output Equivalent Circuits



Switching Waveforms



Functional Block Diagram



Function Tables

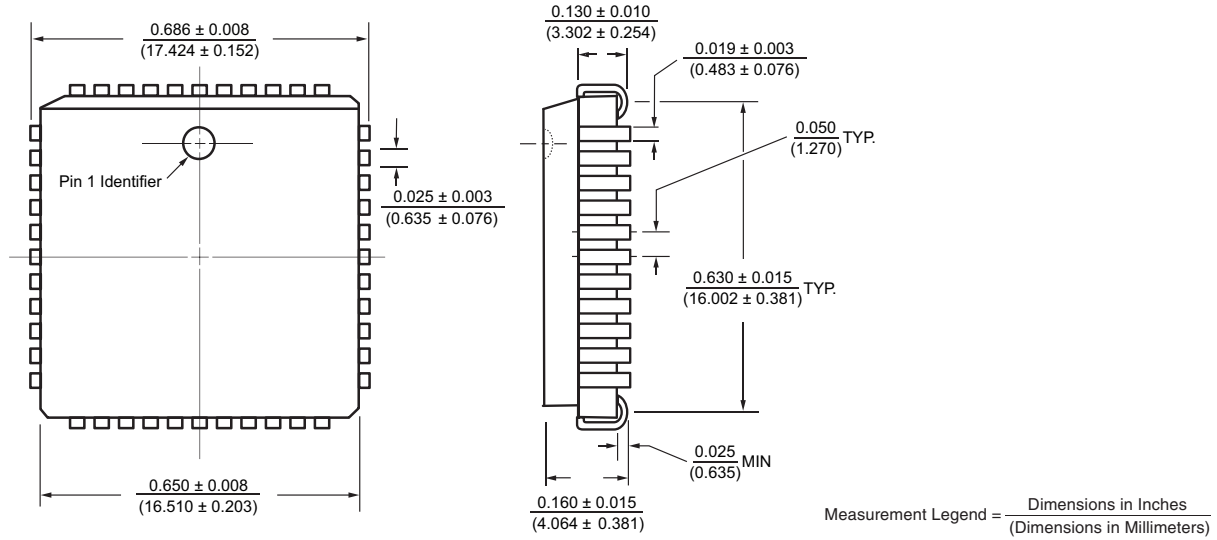
| Data Input | CLK | Data Output |
|------------|-----|-------------|
| X | | H |
| X | | L |
| H | No | No change |

| Data Input | \overline{LE} | OE | HV Output |
|------------|-----------------|----|-----------------------------|
| X | X | L | All HV _{OUT} = LOW |
| X | L | H | Previous latched data |
| H | H | H | H |
| L | H | H | L |

Pin Description

| Pin Name | Function | Description |
|--------------------------|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLK | Data shift register clock | Input are shifted into the shift register on the positive edge of the clock. |
| \overline{LE} | Latch enable input | When \overline{LE} is HIGH, shift register data is transferred into a data latch. When \overline{LE} is LOW, data is latched, and new data can be clocked into the shift register. |
| OE | Output enable input | When OE is LOW, all HV outputs are forced into a LOW state, regardless of data in each channel. When OE is HIGH, all HV outputs reflect data latched. |
| Data input | Serial data input | Data needs to be present before each rising edge of the clock. |
| Data output | Serial data output | Data output for cascading to the data input of the next device. |
| HV _{OUT} (1-32) | High voltage outputs | High voltage push-pull outputs, which, depending on controlling low voltage data, can drive loads either to a GND, or to V _{PP} rail levels. |
| GND | Logic and high voltage ground | --- |
| V _{DD} | Low voltage logic power rail | --- |
| V _{PP} | High voltage power rail | --- |

44-J Lead Quad Ceramic Chip Carrier (DJ)

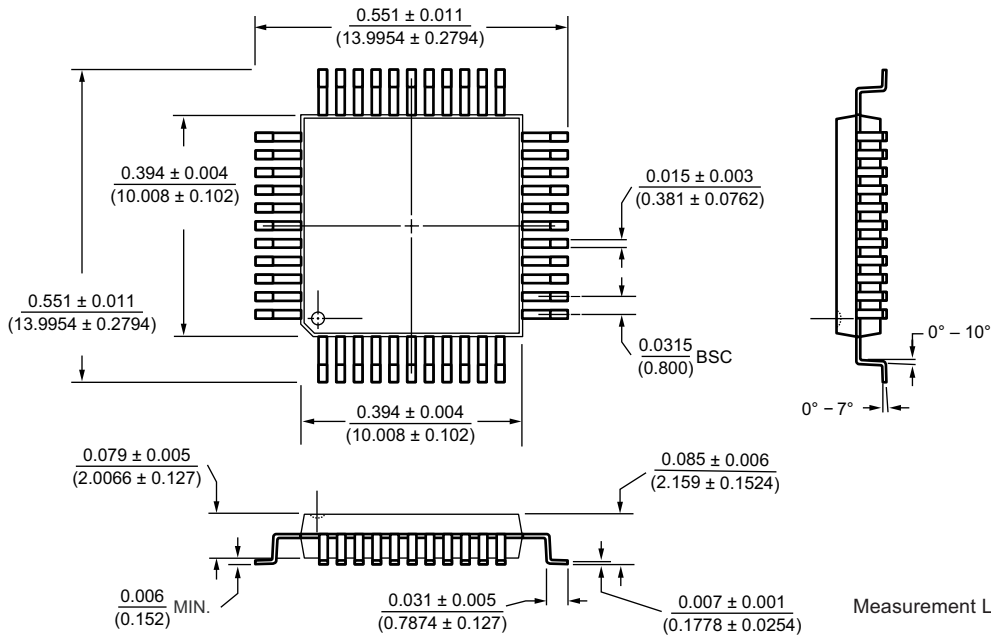


Pin Assignment

| HV5308DJ-B | | | |
|------------|----------------------|-----|----------------------|
| Pin | Function | Pin | Function |
| 1 | HV _{OUT} 17 | 23 | GND |
| 2 | HV _{OUT} 16 | 24 | V _{PP} |
| 3 | HV _{OUT} 15 | 25 | V _{DD} |
| 4 | HV _{OUT} 14 | 26 | \overline{LE} |
| 5 | HV _{OUT} 13 | 27 | Data In |
| 6 | HV _{OUT} 12 | 28 | OE |
| 7 | HV _{OUT} 11 | 29 | NC |
| 8 | HV _{OUT} 10 | 30 | HV _{OUT} 32 |
| 9 | HV _{OUT} 9 | 31 | HV _{OUT} 31 |
| 10 | HV _{OUT} 8 | 32 | HV _{OUT} 30 |
| 11 | HV _{OUT} 7 | 33 | HV _{OUT} 29 |
| 12 | HV _{OUT} 6 | 34 | HV _{OUT} 28 |
| 13 | HV _{OUT} 5 | 35 | HV _{OUT} 27 |
| 14 | HV _{OUT} 4 | 36 | HV _{OUT} 26 |
| 15 | HV _{OUT} 3 | 37 | HV _{OUT} 25 |
| 16 | HV _{OUT} 2 | 38 | HV _{OUT} 24 |
| 17 | HV _{OUT} 1 | 39 | HV _{OUT} 23 |
| 18 | Data Out | 40 | HV _{OUT} 22 |
| 19 | N/C | 41 | HV _{OUT} 21 |
| 20 | N/C | 42 | HV _{OUT} 20 |
| 21 | N/C | 43 | HV _{OUT} 19 |
| 22 | CLK | 44 | HV _{OUT} 18 |

| HV5408DJ-B | | | |
|------------|----------------------|-----|----------------------|
| Pin | Function | Pin | Function |
| 1 | HV _{OUT} 16 | 23 | GND |
| 2 | HV _{OUT} 17 | 24 | V _{PP} |
| 3 | HV _{OUT} 18 | 25 | V _{DD} |
| 4 | HV _{OUT} 19 | 26 | \overline{LE} |
| 5 | HV _{OUT} 20 | 27 | Data In |
| 6 | HV _{OUT} 21 | 28 | OE |
| 7 | HV _{OUT} 22 | 29 | NC |
| 8 | HV _{OUT} 23 | 30 | HV _{OUT} 1 |
| 9 | HV _{OUT} 24 | 31 | HV _{OUT} 2 |
| 10 | HV _{OUT} 25 | 32 | HV _{OUT} 3 |
| 11 | HV _{OUT} 26 | 33 | HV _{OUT} 4 |
| 12 | HV _{OUT} 27 | 34 | HV _{OUT} 5 |
| 13 | HV _{OUT} 28 | 35 | HV _{OUT} 6 |
| 14 | HV _{OUT} 29 | 36 | HV _{OUT} 7 |
| 15 | HV _{OUT} 30 | 37 | HV _{OUT} 8 |
| 16 | HV _{OUT} 31 | 38 | HV _{OUT} 9 |
| 17 | HV _{OUT} 32 | 39 | HV _{OUT} 10 |
| 18 | Data Out | 40 | HV _{OUT} 11 |
| 19 | N/C | 41 | HV _{OUT} 12 |
| 20 | N/C | 42 | HV _{OUT} 13 |
| 21 | N/C | 43 | HV _{OUT} 14 |
| 22 | CLK | 44 | HV _{OUT} 15 |

44-Lead Quad Plastic Gullwing (PG)

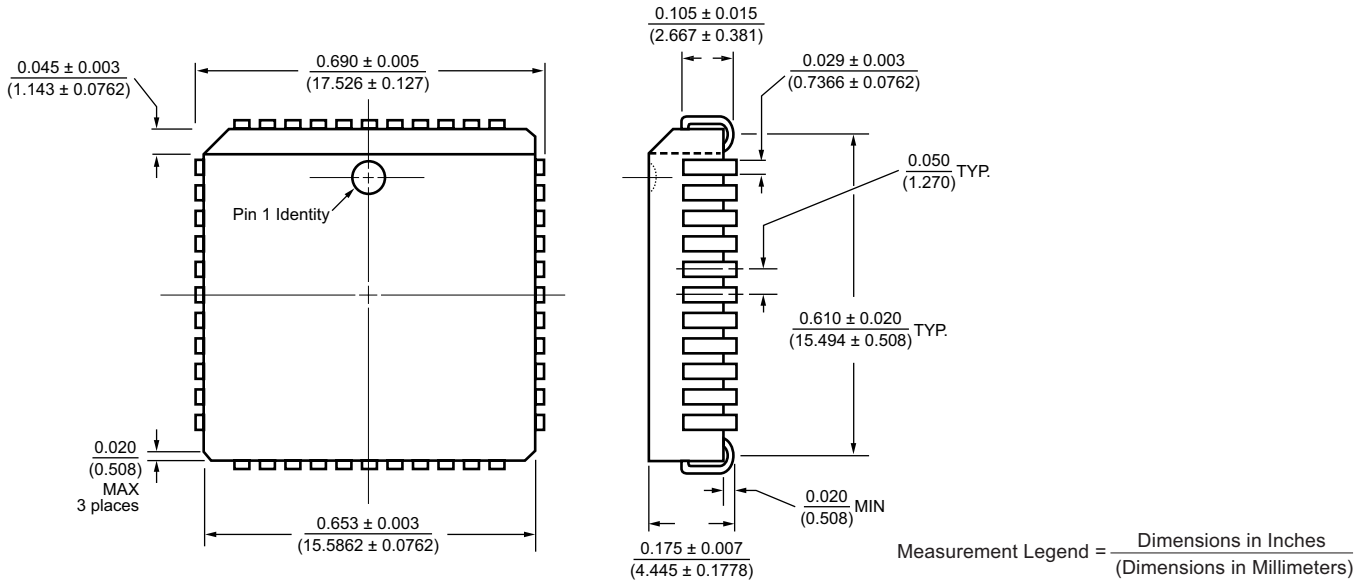


Pin Assignment

| HV5308PG-B | | | |
|------------|----------------------|-----|----------------------|
| Pin | Function | Pin | Function |
| 1 | HV _{OUT} 22 | 23 | Data Out |
| 2 | HV _{OUT} 21 | 24 | N/C |
| 3 | HV _{OUT} 20 | 25 | N/C |
| 4 | HV _{OUT} 19 | 26 | N/C |
| 5 | HV _{OUT} 18 | 27 | CLK |
| 6 | HV _{OUT} 17 | 28 | GND |
| 7 | HV _{OUT} 16 | 29 | V _{PP} |
| 8 | HV _{OUT} 15 | 30 | V _{DD} |
| 9 | HV _{OUT} 14 | 31 | LE |
| 10 | HV _{OUT} 13 | 32 | Data In |
| 11 | HV _{OUT} 12 | 33 | OE |
| 12 | HV _{OUT} 11 | 34 | N/C |
| 13 | HV _{OUT} 10 | 35 | HV _{OUT} 32 |
| 14 | HV _{OUT} 9 | 36 | HV _{OUT} 31 |
| 15 | HV _{OUT} 8 | 37 | HV _{OUT} 30 |
| 16 | HV _{OUT} 7 | 38 | HV _{OUT} 29 |
| 17 | HV _{OUT} 6 | 39 | HV _{OUT} 28 |
| 18 | HV _{OUT} 5 | 40 | HV _{OUT} 27 |
| 19 | HV _{OUT} 4 | 41 | HV _{OUT} 26 |
| 20 | HV _{OUT} 3 | 42 | HV _{OUT} 25 |
| 21 | HV _{OUT} 2 | 43 | HV _{OUT} 24 |
| 22 | HV _{OUT} 1 | 44 | HV _{OUT} 23 |

| HV5408PG-B | | | |
|------------|----------------------|-----|----------------------|
| Pin | Function | Pin | Function |
| 1 | HV _{OUT} 11 | 23 | Data Out |
| 2 | HV _{OUT} 12 | 24 | N/C |
| 3 | HV _{OUT} 13 | 25 | N/C |
| 4 | HV _{OUT} 14 | 26 | N/C |
| 5 | HV _{OUT} 15 | 27 | CLK |
| 6 | HV _{OUT} 16 | 28 | GND |
| 7 | HV _{OUT} 17 | 29 | V _{PP} |
| 8 | HV _{OUT} 18 | 30 | V _{DD} |
| 9 | HV _{OUT} 19 | 31 | LE |
| 10 | HV _{OUT} 20 | 32 | Data In |
| 11 | HV _{OUT} 21 | 33 | OE |
| 12 | HV _{OUT} 22 | 34 | N/C |
| 13 | HV _{OUT} 23 | 35 | HV _{OUT} 1 |
| 14 | HV _{OUT} 24 | 36 | HV _{OUT} 2 |
| 15 | HV _{OUT} 25 | 37 | HV _{OUT} 3 |
| 16 | HV _{OUT} 26 | 38 | HV _{OUT} 4 |
| 17 | HV _{OUT} 27 | 39 | HV _{OUT} 5 |
| 18 | HV _{OUT} 28 | 40 | HV _{OUT} 6 |
| 19 | HV _{OUT} 29 | 41 | HV _{OUT} 7 |
| 20 | HV _{OUT} 30 | 42 | HV _{OUT} 8 |
| 21 | HV _{OUT} 31 | 43 | HV _{OUT} 9 |
| 22 | HV _{OUT} 32 | 44 | HV _{OUT} 10 |

44-J Lead Quad Plastic Chip Carrier (PJ)



Pin Assignment

| HV5308PJ-B | | | |
|------------|----------------------|-----|----------------------|
| Pin | Function | Pin | Function |
| 1 | HV _{OUT} 17 | 23 | GND |
| 2 | HV _{OUT} 16 | 24 | V _{PP} |
| 3 | HV _{OUT} 15 | 25 | V _{DD} |
| 4 | HV _{OUT} 14 | 26 | \overline{LE} |
| 5 | HV _{OUT} 13 | 27 | Data In |
| 6 | HV _{OUT} 12 | 28 | OE |
| 7 | HV _{OUT} 11 | 29 | NC |
| 8 | HV _{OUT} 10 | 30 | HV _{OUT} 32 |
| 9 | HV _{OUT} 9 | 31 | HV _{OUT} 31 |
| 10 | HV _{OUT} 8 | 32 | HV _{OUT} 30 |
| 11 | HV _{OUT} 7 | 33 | HV _{OUT} 29 |
| 12 | HV _{OUT} 6 | 34 | HV _{OUT} 28 |
| 13 | HV _{OUT} 5 | 35 | HV _{OUT} 27 |
| 14 | HV _{OUT} 4 | 36 | HV _{OUT} 26 |
| 15 | HV _{OUT} 3 | 37 | HV _{OUT} 25 |
| 16 | HV _{OUT} 2 | 38 | HV _{OUT} 24 |
| 17 | HV _{OUT} 1 | 39 | HV _{OUT} 23 |
| 18 | Data Out | 40 | HV _{OUT} 22 |
| 19 | N/C | 41 | HV _{OUT} 21 |
| 20 | N/C | 42 | HV _{OUT} 20 |
| 21 | N/C | 43 | HV _{OUT} 19 |
| 22 | CLK | 44 | HV _{OUT} 18 |

| HV5408PJ-B | | | |
|------------|----------------------|-----|----------------------|
| Pin | Function | Pin | Function |
| 1 | HV _{OUT} 16 | 23 | GND |
| 2 | HV _{OUT} 17 | 24 | V _{PP} |
| 3 | HV _{OUT} 18 | 25 | V _{DD} |
| 4 | HV _{OUT} 19 | 26 | \overline{CE} |
| 5 | HV _{OUT} 20 | 27 | Data In |
| 6 | HV _{OUT} 21 | 28 | OE |
| 7 | HV _{OUT} 22 | 29 | NC |
| 8 | HV _{OUT} 23 | 30 | HV _{OUT} 1 |
| 9 | HV _{OUT} 24 | 31 | HV _{OUT} 2 |
| 10 | HV _{OUT} 25 | 32 | HV _{OUT} 3 |
| 11 | HV _{OUT} 26 | 33 | HV _{OUT} 4 |
| 12 | HV _{OUT} 27 | 34 | HV _{OUT} 5 |
| 13 | HV _{OUT} 28 | 35 | HV _{OUT} 6 |
| 14 | HV _{OUT} 29 | 36 | HV _{OUT} 7 |
| 15 | HV _{OUT} 30 | 37 | HV _{OUT} 8 |
| 16 | HV _{OUT} 31 | 38 | HV _{OUT} 9 |
| 17 | HV _{OUT} 32 | 39 | HV _{OUT} 10 |
| 18 | Data Out | 40 | HV _{OUT} 11 |
| 19 | N/C | 41 | HV _{OUT} 12 |
| 20 | N/C | 42 | HV _{OUT} 13 |
| 21 | N/C | 43 | HV _{OUT} 14 |
| 22 | CLK | 44 | HV _{OUT} 15 |

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