



# SPP9434 P-Channel Enhancement Mode MOSFET

## DESCRIPTION

The SPP9434 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits, and low in-line power loss are needed in a very small outline surface mount package.

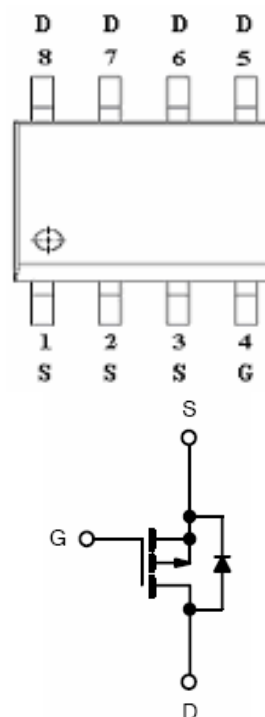
## FEATURES

- ◆ -20V/-7.2 A,  $R_{DS(ON)} = 40m\Omega @ V_{GS} = -4.5V$
- ◆ -20V/-5.2 A,  $R_{DS(ON)} = 52m\Omega @ V_{GS} = -2.5V$
- ◆ -20V/-3.6 A,  $R_{DS(ON)} = 62m\Omega @ V_{GS} = -1.8V$
- ◆ Super high density cell design for extremely low  $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP-8P package design

## APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

## PIN CONFIGURATION(SOP – 8P)



## PART MARKING





# SPP9434

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### PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

### ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9434S8RG	SOP- 8P	SPP9434
SPP9434S8RGB	SOP- 8P	SPP9434

※ SPP9434S8RG : 13" Tape Reel ; Pb – Free

※ SPP9434S8RGB : 13" Tape Reel ; Pb – Free ; Halogen - Free

### ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V <sub>DSS</sub>	-20	V
Gate –Source Voltage	V <sub>GSS</sub>	±12	V
Continuous Drain Current(T <sub>J</sub> =150°C)	I <sub>D</sub>	TA=25°C	-7.6
		TA=70°C	-5.4
Pulsed Drain Current	I <sub>DM</sub>	-30	A
Continuous Source Current(Diode Conduction)	I <sub>S</sub>	-2.3	A
Power Dissipation	P <sub>D</sub>	TA=25°C	2.8
		TA=70°C	1.8
Operating Junction Temperature	T <sub>J</sub>	-55/150	°C
Storage Temperature Range	T <sub>STG</sub>	-55/150	°C
Thermal Resistance-Junction to Ambient	R <sub>θJA</sub>	70	°C/W



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### ELECTRICAL CHARACTERISTICS

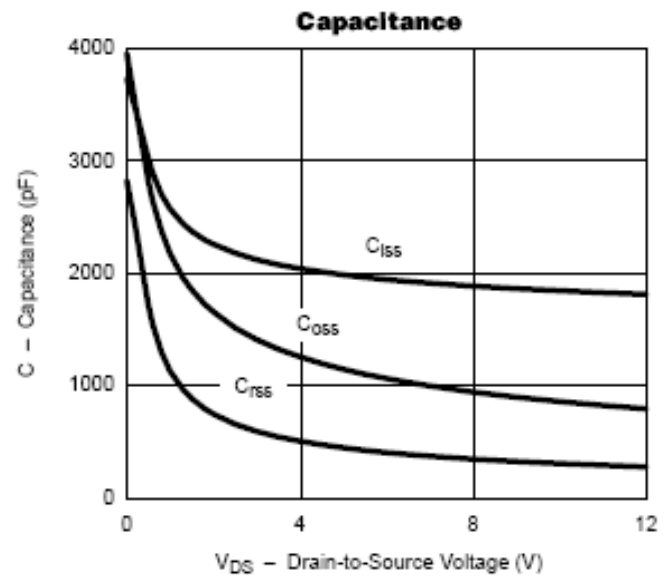
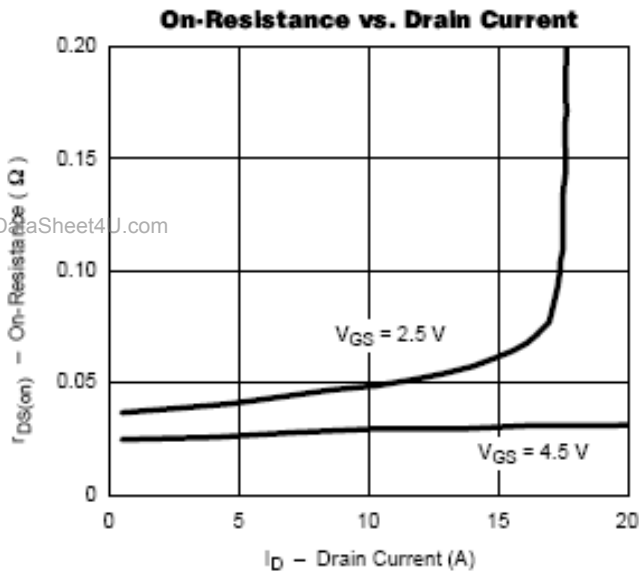
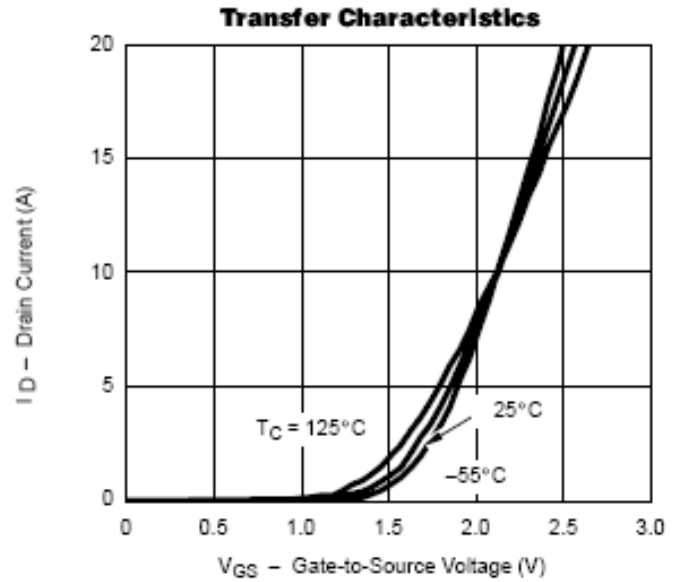
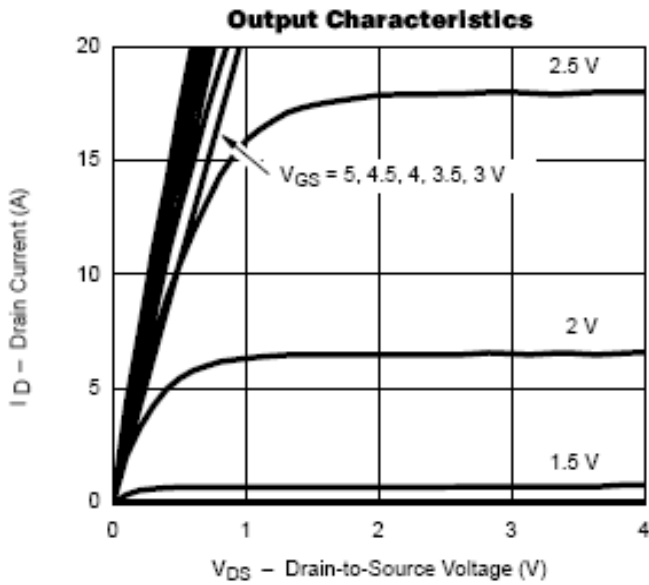
(TA=25°C Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =-250uA	-20			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =-250uA	-0.35		-0.9	
Gate Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V			-1	uA
		V <sub>DS</sub> =-20V, V <sub>GS</sub> =0V T <sub>J</sub> =55°C			-10	
On-State Drain Current	I <sub>D(on)</sub>	V <sub>DS</sub> ≤ -5V, V <sub>GS</sub> =-4.5V	-10			A
Drain-Source On-Resistance	R <sub>DSS(on)</sub>	V <sub>GS</sub> =-4.5V, I <sub>D</sub> =-7.2A		0.030	0.040	Ω
		V <sub>GS</sub> =-2.5V, I <sub>D</sub> =-5.2A		0.040	0.052	
		V <sub>GS</sub> =-1.8V, I <sub>D</sub> =-3.6A		0.050	0.062	
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> =-5.0V, I <sub>D</sub> =-6.2A		14		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> =-2.5A, V <sub>GS</sub> =0V		-0.8	-1.2	V
<b>Dynamic</b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =-4.5V I <sub>D</sub> =-6.4A		20	25	nC
Gate-Source Charge	Q <sub>gs</sub>			4.5		
Gate-Drain Charge	Q <sub>gd</sub>			8.0		
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =-10V, V <sub>GS</sub> =0V f=1MHz		700		pF
Output Capacitance	C <sub>oss</sub>			160		
Reverse Transfer Capacitance	C <sub>rss</sub>			120		
Turn-On Time	t <sub>d(on)</sub>	V <sub>DD</sub> =-10V, R <sub>L</sub> =6Ω I <sub>D</sub> =-1.0A, V <sub>GEN</sub> =-4.5V R <sub>G</sub> =6Ω		20	30	ns
	t <sub>r</sub>			40	65	
Turn-Off Time	t <sub>d(off)</sub>			90	120	
	t <sub>f</sub>			70	90	



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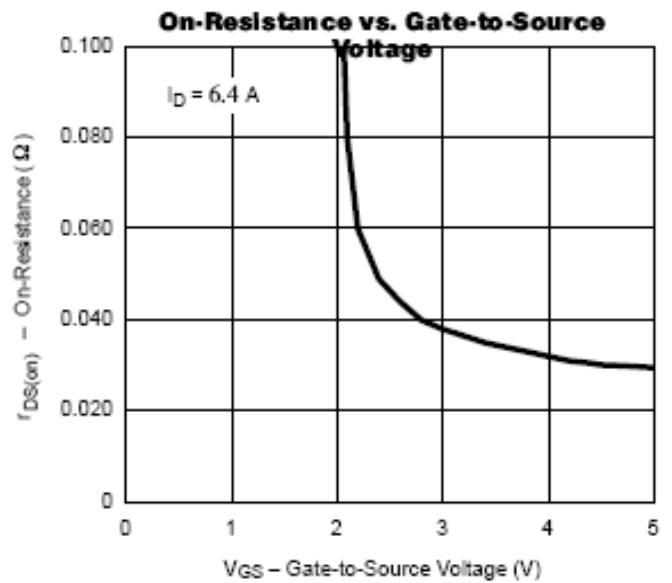
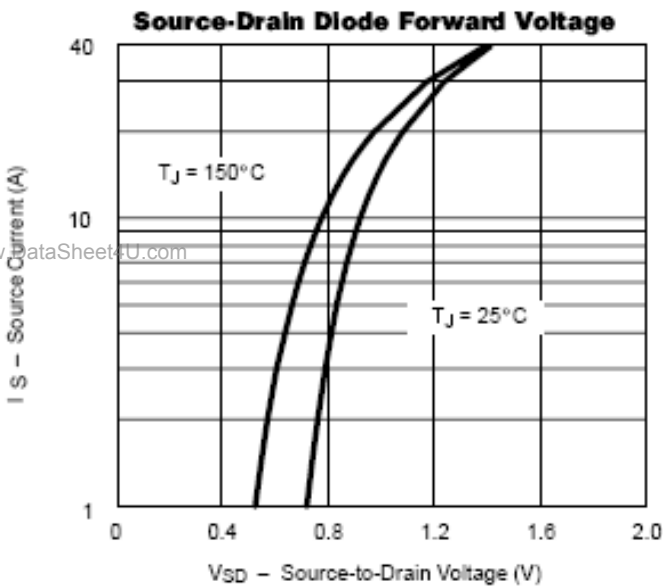
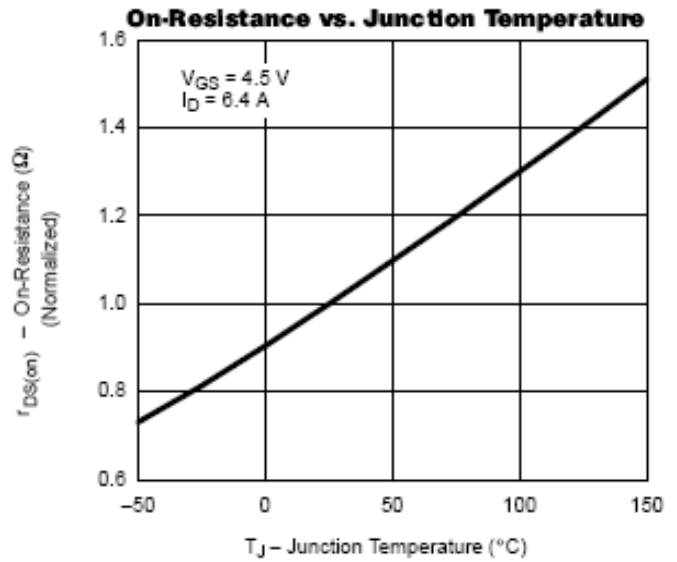
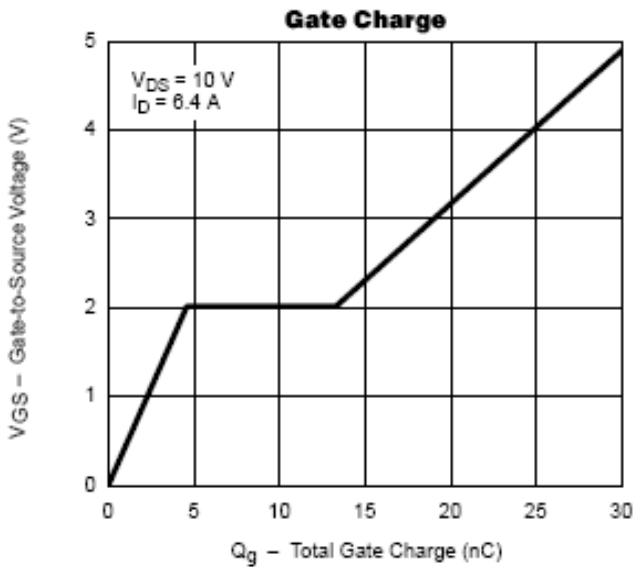
## TYPICAL CHARACTERISTICS





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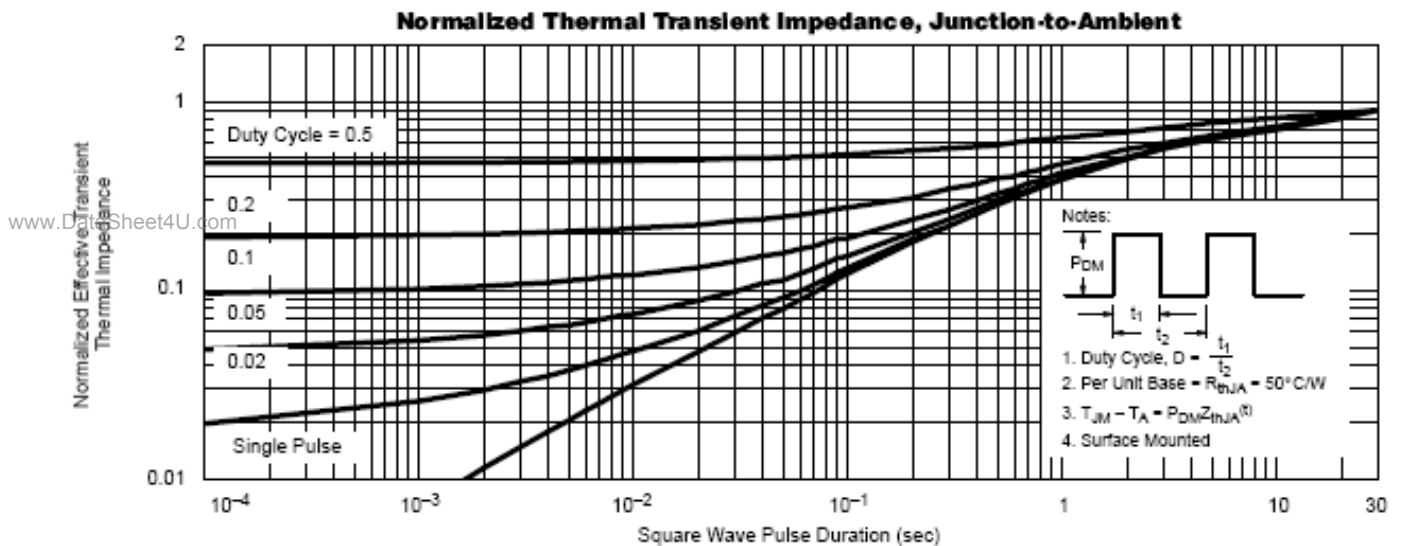
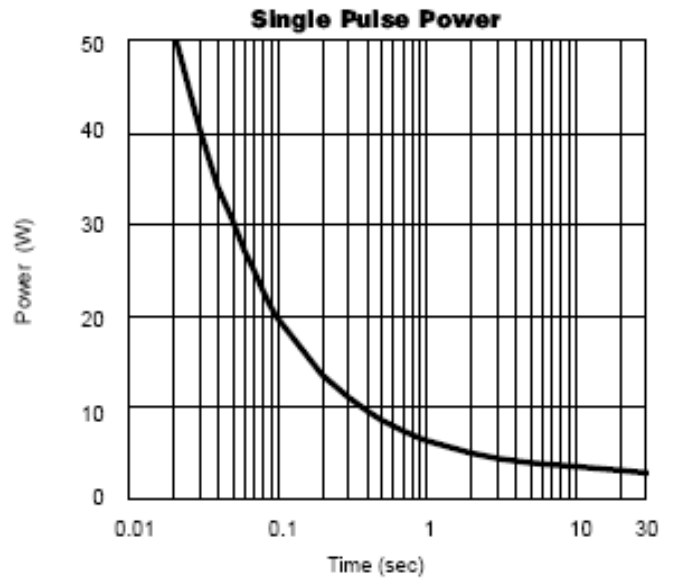
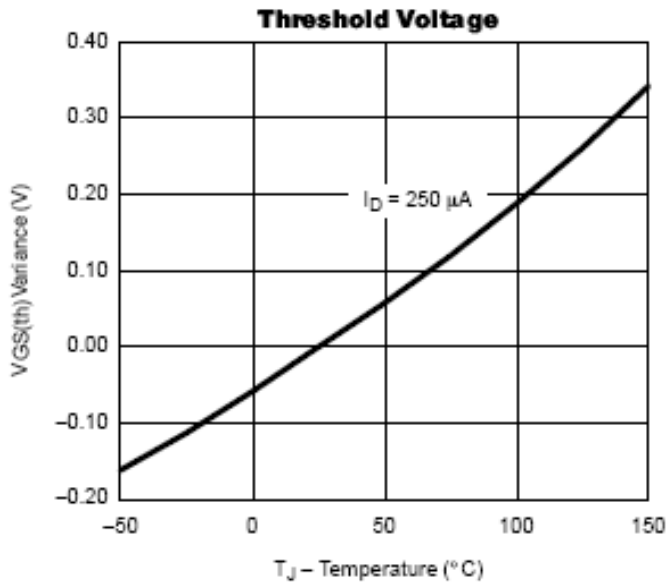
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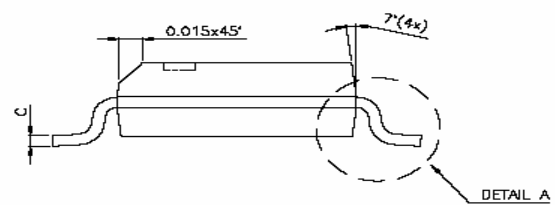
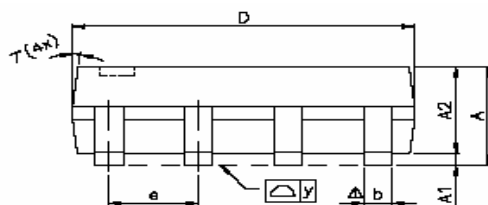
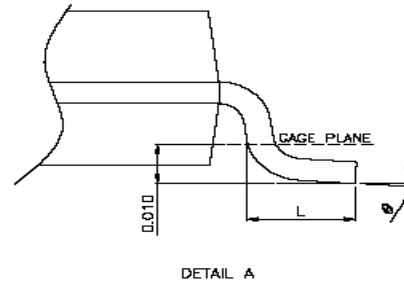
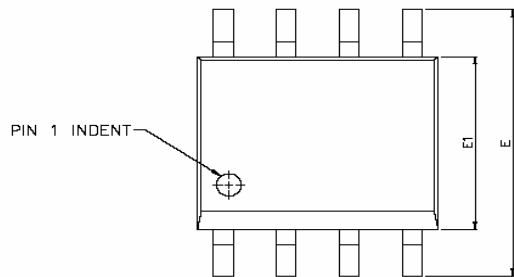




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## P-Channel Enhancement Mode MOSFET

### SOP- 8 PACKAGE OUTLINE



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	—	0.25	0.004	—	0.010
A2	—	1.45	—	—	0.057	—
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	—	1.27	—	—	0.050	—
L	0.38	0.71	1.27	0.015	0.028	0.050
$\Delta$ y	—	—	0.076	—	—	0.003
$\varnothing$	0°	—	8°	0°	—	8°



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